PROCESS CP307

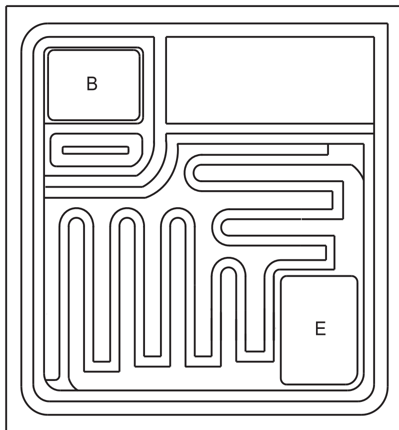
Small Signal Transistor

NPN - Silicon Darlington Transistor Chip

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	27 x 27 MILS
Die Thickness	9.0 MILS
Base Bonding Pad Area	5.3 x 3.8 MILS
Emitter Bonding Pad Area	5.3 x 6.5 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au - 18,000Å

GEOMETRY



R1

BACKSIDE COLLECTOR

GROSS DIE PER 4 INCH WAFER

15,165

PRINCIPAL DEVICE TYPES

2N6426
2N6427
CMPT6427
CMPTA13
CMPTA14
CXTA14
CZTA14
MPSA13
MPSA14
MPSA27

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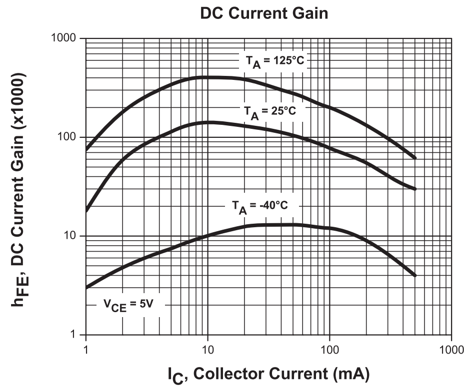
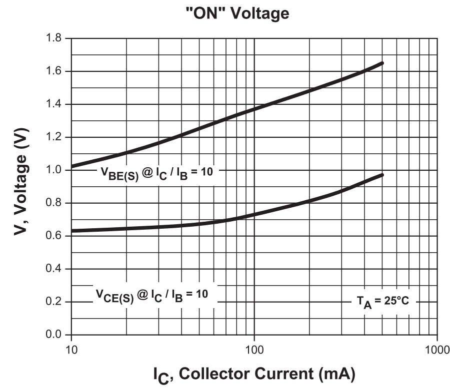
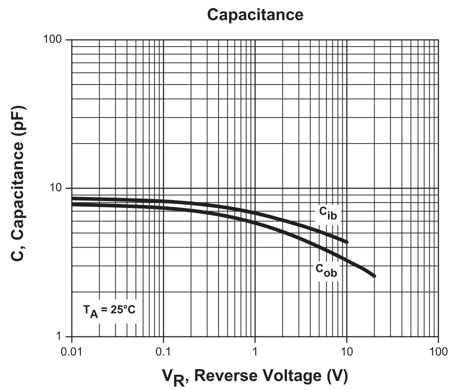
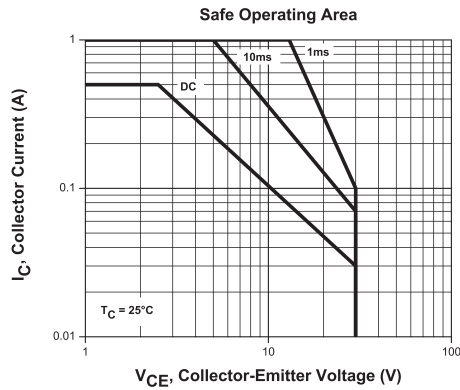
PROCESS CP307

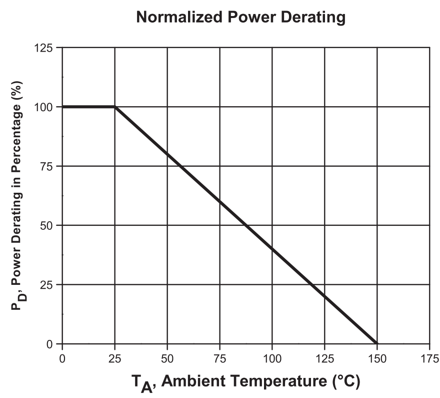
Typical Electrical Characteristics

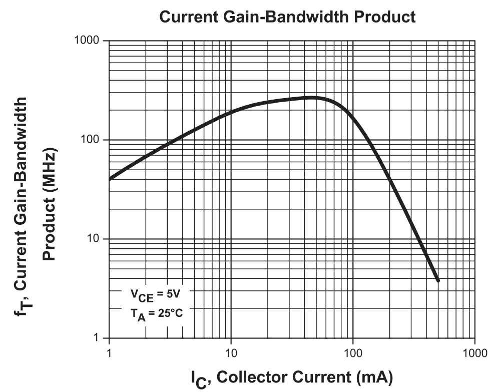












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