

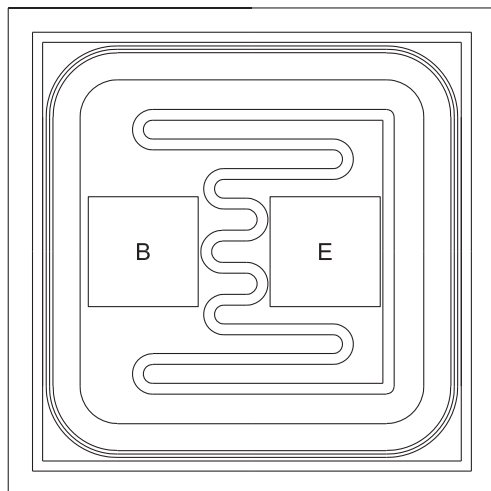
PROCESS CP336V
Small Signal Transistor
NPN - High Voltage Transistor Chip



PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	17.3 x 17.3 MILS
Die Thickness	7.1 MILS
Base Bonding Pad Area	3.9 x 3.9 MILS
Emitter Bonding Pad Area	3.9 x 3.9 MILS
Top Side Metalization	Al-Si - 30,000Å
Back Side Metalization	Au - 12,000Å

GEOMETRY



BACKSIDE COLLECTOR R0

GROSS DIE PER 5 INCH WAFER

57,735

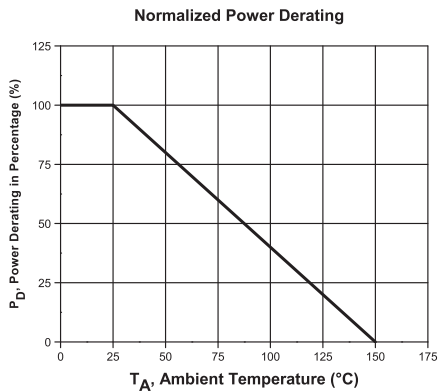
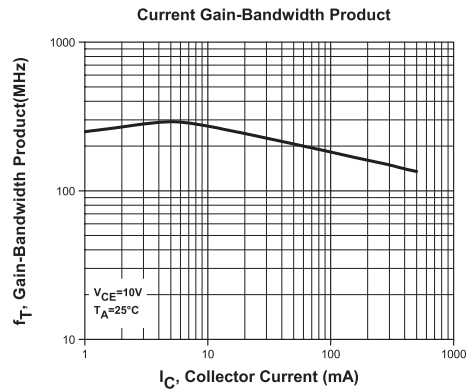
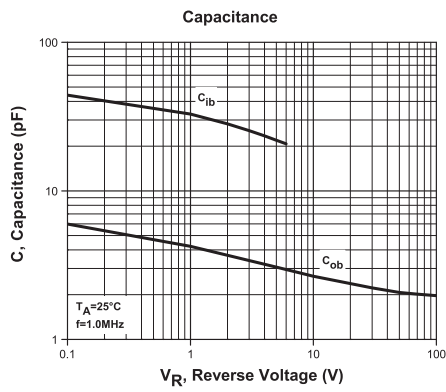
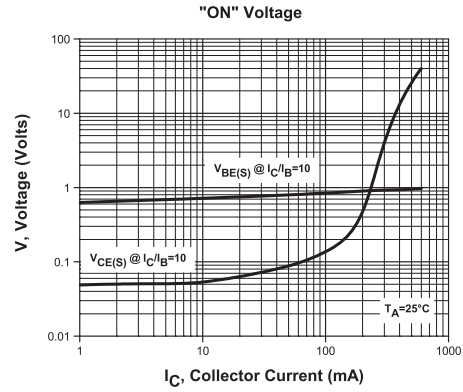
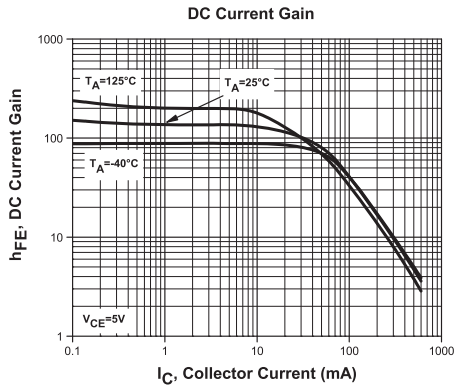
PRINCIPAL DEVICE TYPES

CMPT5551
CTLT5551-M832D
CXT5551
CZT5551
CZT5551E

R1 (26-October 2010)

PROCESS CP336V

Typical Electrical Characteristics



R1 (26-October 2010)