



Features

- Excellent common-mode rejection ratio (CMRR), >40 dB
- Supplied application circuits can meet isolation requirements of worldwide telephony standards
- Small 8-pin SOIC
- Worldwide telephone network compatibility
- Full-wave ringing level detector comparator with internal threshold, large hysteresis, and logic-level output
- 3.3 or 5.0 Volt operation
- High differential input impedance, very low common-mode input impedance
- Fixed gain
- Differential or single-ended linear output
- TTL logic input
- CMOS logic output (TTL compatible)
- Virtually non-detectable in voice monitoring applications

Description

The Clare CPC5710N is a CMOS special purpose fixed-gain amplifier with comparator for telephone line monitoring. The high (>40 dB) common-mode rejection ratio makes the CPC5710N an excellent choice for signal monitoring, discrete voice recording, and line condition monitoring applications. The CPC5710N is ideal for modem applications including embedded modem designs like set-top boxes, and voice recording applications.

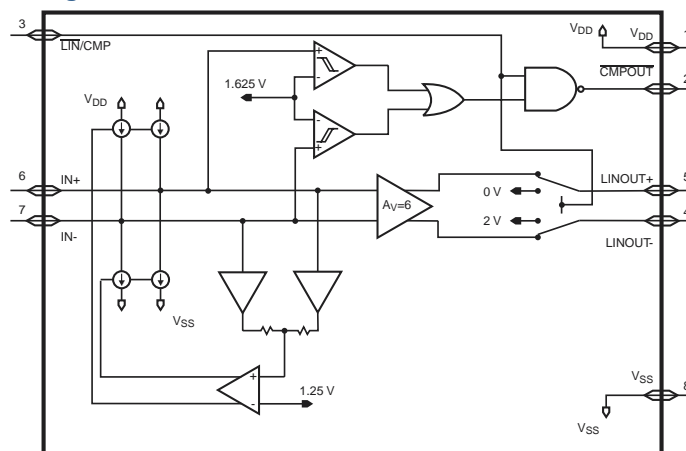
Ordering Information

Part Number	Description
CPC5710N	Phone line monitor IC, tubed
CPC5710NTR	Phone line monitor IC, tape and reel

Applications

- In signal monitoring applications, CPC5710N can be used for:
 - Display feature (caller ID) signal processing
 - Line-in-use detection (another-phone-off-hook)
 - Ringing signal level detection
 - Battery presence monitoring
 - Tip and ring lead voltage monitoring
- Line condition detection, including line polarity, tip and ring lead voltage, and battery presence

Figure 1. CPC5710N Block Diagram





CPC5710N

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1. Specifications

1.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
V_{DD}	-0.3	6	V
Storage temperature	-40	+125	°C
Total package power dissipation		300	mW
Logic input voltage	-0.3	$V_{DD} + 0.3$	V

Absolute maximum ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this data sheet is not implied. Exposure of the device to the absolute maximum ratings for an extended period may degrade the device and affect its reliability.

1.2 Electrical Characteristics

$V_{DD} = 5V$, temperature = 25 °C unless otherwise indicated.

Parameter	Conditions	Minimum	Typical	Maximum	Unit
DC Characteristics					
Supply voltage, V_{DD}		3.0	-	5.5	V
Supply current, I_{DD}		-	-	10	mA
AC Characteristics					
Input Impedance		10	-	-	MΩ
Input offset voltage, V_{IO}		-	-	40	mV
Input offset current, I_{IO}	No common-mode signal applied	-	-	35	nA
Input offset current, I_{IO}	With 12 μA of common-mode signal applied	-	-	125	nA
Output DC bias level	At LINOUT+ or LINOUT-, $I_O @ 0.5$ mA	0.9	1.0	1.1	V
Output Low Voltage Swing	$I_O = 0.5$ mA	-	-	50	mV
Gain, A_V	0 to 20 kHz	5.88	6	6.12	-
Common-mode rejection ratio, CMRR	Using supplied application circuits, with common-mode current ≤ 12 μA, 0 to 120 Hz	40	-	-	dB
Equivalent input noise voltage, V_N		-	-90	-	dBm/Hz

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Comparator Threshold Characteristics					
Comparator detection threshold voltage	$I_{CM} = 0$	675	750	850	mV
Comparator detection threshold voltage	$I_{CM} = \pm 12 \mu A$	488	750	1012	mV
Comparator hysteresis voltage	$I_{CM} = 0$	300	375	450	mV
LIN/CMP Input Characteristics					
Input low voltage	V_{IL}	-	-	0.8	V
Input high voltage	V_{IH}	2.0	-	-	V
Input high leakage current (I_{IH})	$V_{IH} = 2.4 V$	-	-	-120	μA
Input low leakage current (I_{IL})	$V_{IL} = 0.4 V$	-	-	-120	μA
<i>Unless otherwise specified, minimum and maximum values are production testing requirements. Typical values are characteristic of the device and are the result of engineering evaluations. Typical values are provided for information purposes only and are not part of the testing requirements.</i>					

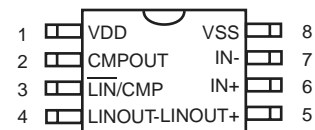
1.3 Environmental Characteristics

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Operating temperature		-40	-	+85	$^{\circ}C$
Operating humidity	non-condensing	5	-	95	%

1.4 Pinout

Pin	Name	Description
1	VDD	Power supply
2	\overline{CMPOUT}	Comparator output, active low
3	$\overline{LIN/CMP}$	Output select, low for linear output or high for comparator output
4	LINOUT-	Negative differential linear output
5	LINOUT+	Positive differential linear output
6	IN+	Positive differential input
7	IN-	Negative differential input
8	VSS	Ground

Figure 2. Package Pinout





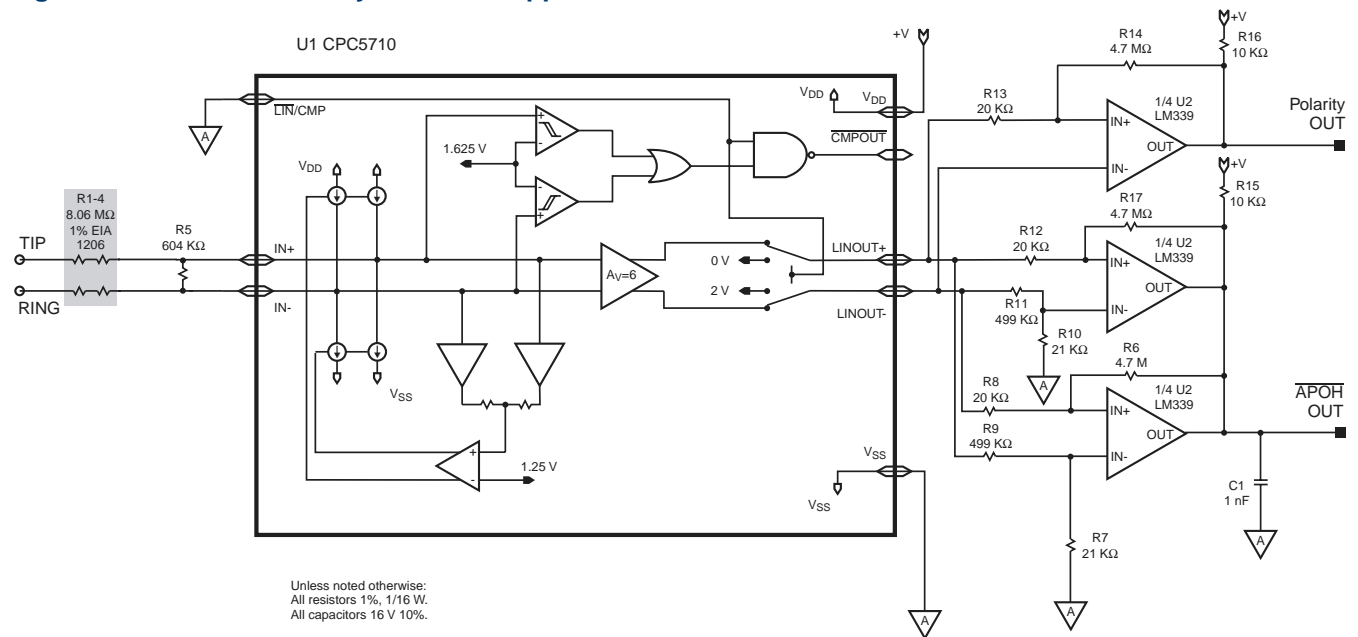
2. Applications

2.1 Another-Phone-Off-Hook (APOH) and Line Polarity Detector

This circuit performs two additional phone line interface functions, APOH and line polarity detection. The APOH output is logic low if another phone connected in parallel to the detector is off-hook, specifically, if the tip lead to ring lead voltage is less than approximately 18 V.

The polarity output indicates the polarity of the phone line. If tip is positive with respect to ring, polarity out will be high.

Figure 3. APOH and Polarity Detection Application Circuit



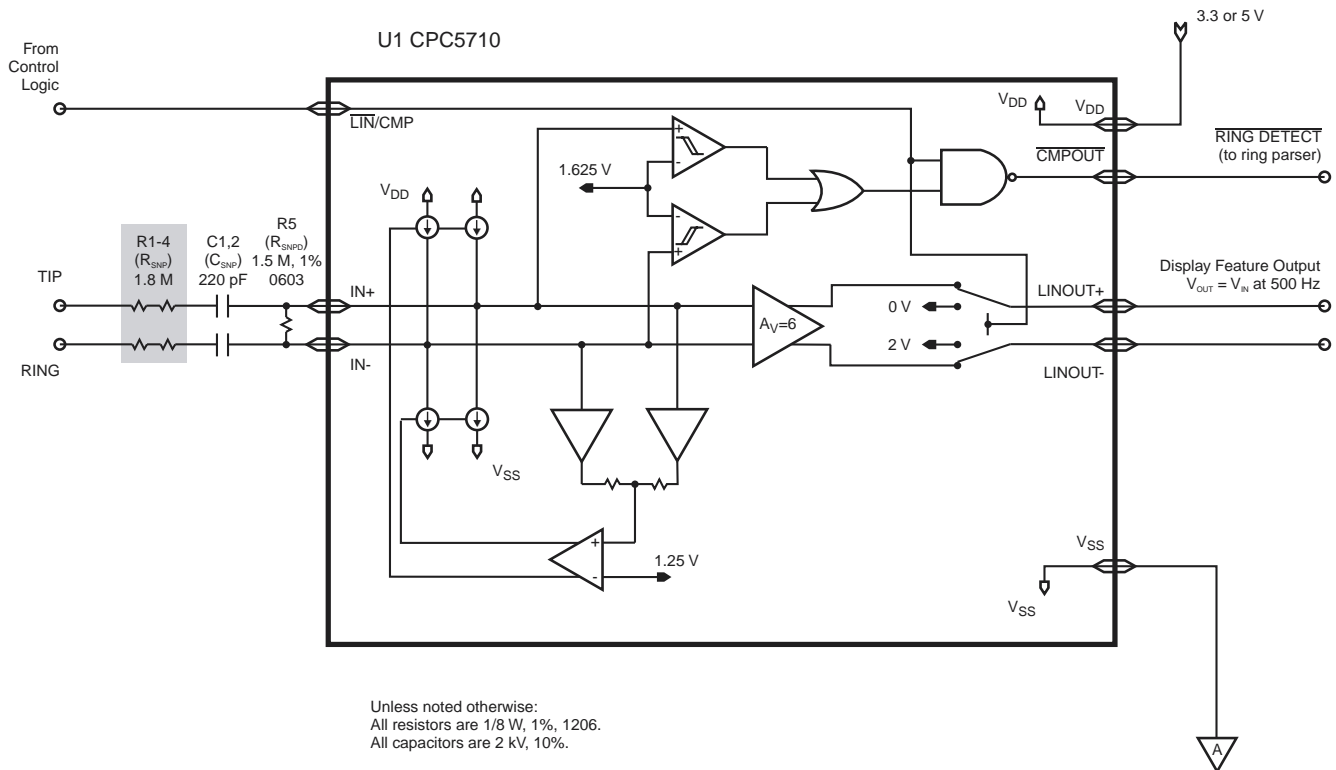
2.2 Non-Intrusive Line Monitoring, Display Feature (Caller ID) Signal Reception, and Ring Detection Application

This application uses the logic input $\overline{\text{LIN}}/\text{CMP}$ to select between detecting ringing or passing through display feature (caller-ID) and voice signals. Note the AC coupling of the tip and ring signals.

With this circuit, set $\overline{\text{LIN}}/\text{CMP}$ high to detect ringing. After a valid ring, set $\overline{\text{LIN}}/\text{CMP}$ low to couple the audio channel signal to the output pins.

Please see “Comparator Considerations” on page 7 for more information on ringing detection.

Figure 4. Non-Intrusive Line Monitoring, Display Feature (Caller ID) Signal Reception, and Ring Detection Application Circuit



2.2.1 Frequency Response

The blocking capacitors used in this application circuit affect the frequency response of the system. With the components shown, response rolls off 3 dB @ 166 Hz. Other values can be used for different response characteristics.

2.3 Regulatory Issues

Component sizing and value recommendations shown in the application circuits above will need to be reviewed with regard to the regulatory requirements of any particular application.



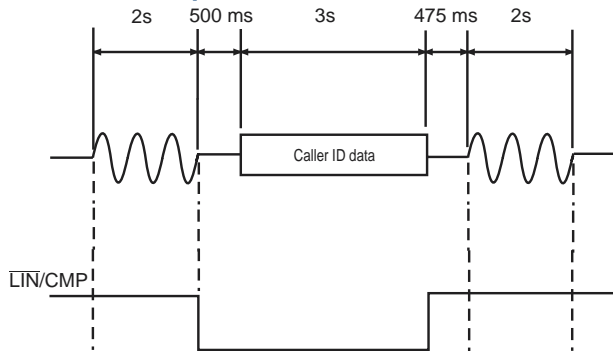
3. Using CPC5710N

3.1 $\overline{\text{LIN/CMP}}$ Input

The $\overline{\text{LIN/CMP}}$ input selects the active output, either the comparator output $\overline{\text{CMPOUT}}$ or the linear outputs, LINOUT- and LINOUT+ . Set $\overline{\text{LIN/CMP}}$ low for linear output and high for comparator output. Note that both outputs cannot be used at once.

With $\overline{\text{LIN/CMP}}$ at logic low ($\overline{\text{LIN/CMP}} = 0$), the amplifier outputs are biased at 1 Vdc and $\overline{\text{CMPOUT}}$ is held high. With $\overline{\text{LIN/CMP}}$ at logic high ($\overline{\text{LIN/CMP}} = 1$), LINOUT+ is 0 V and LINOUT- is 2 V.

Figure 5. $\overline{\text{LIN/CMP}}$ Timing for Caller-ID Signal Reception



Signal levels not to scale

3.2 Amplifier Design Considerations

Amplifier inputs are biased at 1.25 Vdc, the internal voltage references. The internal common-mode circuitry maintains the average of the inputs at 1.25 Vdc. For example, if one input reaches 1.3 V, the common-mode circuit drives the other input to 1.2 V.

3.2.1 Linear Amplifier Gain

Display feature information (caller ID) and voice signals are coupled through the linear amplifier. In North America, CID data signals are typically sent between the first and second ringing signal burst.

Referring to Figure 4, signal gain from tip and ring to LINOUT+ and LINOUT- is determined by:

$$GAIN_{CID}(dB) = 20 \log \left[\frac{6R_{SNPD}}{\sqrt{(4R_{SNP} + R_{SNPD})^2 + \frac{1}{(\pi f C_{SNP})^2}}} \right]$$

where f is the frequency of the signal.

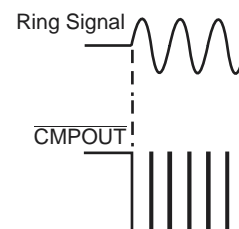
Clare Application Note AN-117 [Customize Caller ID Gain and Ring Detect Voltage Threshold](#) is a spreadsheet for trying different component values in this type of circuit.

3.3 Comparator Considerations

3.3.1 Ringing Signal Detection

The CPC5710N comparator is a full-wave configuration. Ringing signals will assert the output on positive and negative parts of the ringing waveform. Hysteresis is employed in the internal comparator circuit to provide noise immunity. The set-up of the comparator causes $\overline{\text{CMPOUT}}$ output pulses to remain low for most of the ringing signal positive and negative half-cycles. $\overline{\text{CMPOUT}}$ returns high when the ringing signal is near the zero-voltage crossing.

Figure 6. $\overline{\text{CMPOUT}}$ Relative to Ring Signal



3.3.2 Setting Ring Detection Threshold

The ring detection threshold depends on the component values of the input network. The values for these components shown in the typical application circuits are recommended for typical operation. Referring to Figure 4, the ring detection threshold can be changed according to the following formula:

$$V_{RINGPK} = \left(\frac{750mV}{R_{RSNPD}} \right) \sqrt{(4R_{SNP} + R_{SNPD})^2 + \frac{1}{(\pi f_{RING} C_{SNP})^2}}$$

With the application circuit in Figure 4, the series capacitors serve to reduce the magnitude of high-amplitude, low-frequency ring signals, making the ring detection threshold of the CPC5710N variable with the frequency of the ringing signal. With the circuit as given, $\overline{\text{CMPOUT}}$ will change states with a 15 Hz ringing signal at approximately $48 V_{\text{PEAK}}$. For a 68 Hz ring signal, $\overline{\text{CMPOUT}}$ will change states with a ringing signal amplitude of approximately $11.5 V_{\text{PEAK}}$.

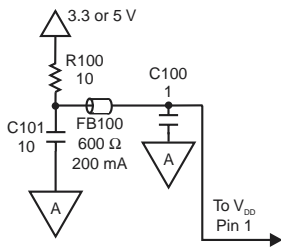
In applications where CPC5710N will be used only as a ring level detector, or if significant attenuation of the amplified signal can be tolerated, the frequency variability of the ring detection threshold can be reduced by increasing the value of the resistors and capacitors in series with the input.

Clare Application Note AN-117 [Customize Caller ID Gain and Ring Detect Voltage Threshold](#) is a spreadsheet for trying different component values in this circuit for LITELINK snoop circuit applications.

4. Power Quality

CPC5710N works best with a clean power supply. To clean up power supply noise, Clare, Inc., recommends using a pi network on the V_{DD} pin as shown in Figure 7, if needed.

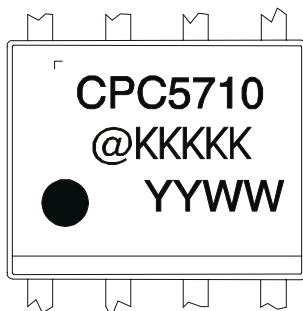
Figure 7. Optional Power Supply pi Network



Note: For lower-frequency noise, use a $220 \mu\text{H}$ inductor in series with R100.

5. Manufacturing Information

The CPC5710N branding (package imprinting) leaves off the last character of the part number due to package space limitations.



5.1 Package Dimensions

CPC5710N uses JEDEC standard 8-pin SOIC packaging. See [JEDEC Publication 95, MS-012](#) for 3.75 (0.150) small-outline package dimensions.

5.2 Soldering

5.2.1 Moisture Reflow Sensitivity

Clare has characterized the moisture reflow sensitivity of this product using IPC/JEDEC standard J-STD-020A and classifies it as MSL (Moisture Sensitivity Level) 1, not moisture sensitive.



5.2.2 Reflow Profile

The maximum ramp rates, dwell times, and temperatures of the assembly reflow profile should not exceed those specified in IPC/JEDEC standard J-STD-020A, which were used to determine the moisture sensitivity level of this component.

For additional information please visit www.clare.com

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