AUTOMOTIVE GRADE

CS8151

5V, 100mA Low Dropout Linear Regulator with WATCHDOG, $\overline{\text{RESET}}$, & WAKE UP

Description

The CS8151 is a precision 5V, 100mA micro-power voltage regulator with very low quiescent current (400μA typical at 200μA load). The 5V output is accurate within ±2% and supplies 100 mA of load current with a typical dropout voltage of 400mV. Microprocessor control logic includes Watchdog, Wake Up and $\overline{\text{RESET}}$. This unique combination of low quiescent current and full microprocessor control makes the CS8151 ideal for use in battery operated, microprocessor controlled equipment.

The CS8151 WAKE UP function brings the microprocessor out of Sleep mode. The microprocessor in turn, signals its WAKE UP status back to the CS8151 by issuing a WATCHDOG signal.

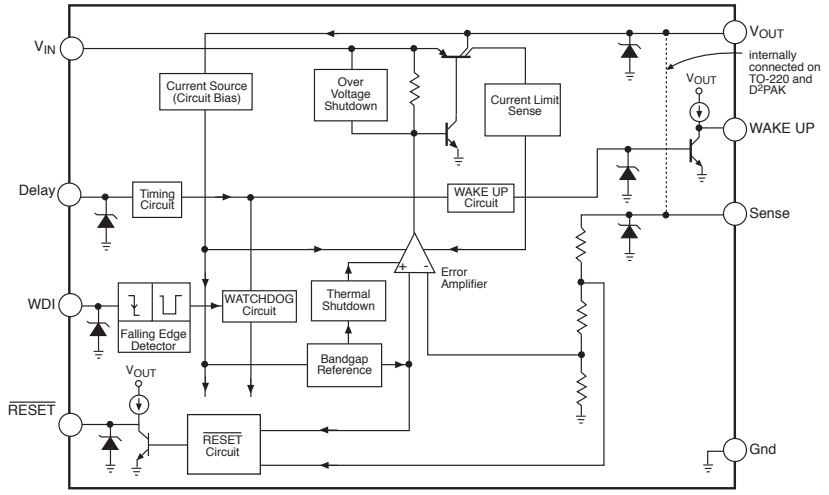
The WATCHDOG logic function monitors an input signal (WDI) from the microprocessor. The CS8151 responds to the falling edge of the WATCHDOG signal which it expects at least once during each wake-up period. When the correct WATCHDOG signal is received, a falling edge is issued on the wake-up signal line.

$\overline{\text{RESET}}$ is independent of V_{IN} and operates correctly to an output voltage as low as 1V. A $\overline{\text{RESET}}$ signal is issued in any of three situations. During power up the $\overline{\text{RESET}}$ is held low until the output voltage is in regulation. During operation if the output voltage shifts below the regulation limits, the $\overline{\text{RESET}}$ toggles low and remains low until proper output voltage regulation is restored. And finally, a $\overline{\text{RESET}}$ signal is issued if the regulator does not receive a WATCHDOG signal within the WAKE UP period.

The $\overline{\text{RESET}}$ pulse width, WAKE UP signal frequency, and WAKE UP delay time are all set by one external capacitor C_{Delay}.

The regulator is protected against short circuit, over voltage, and thermal runaway conditions. The device can withstand 74 volt load dump transients, making it suitable for use in automotive environments.

Block Diagram

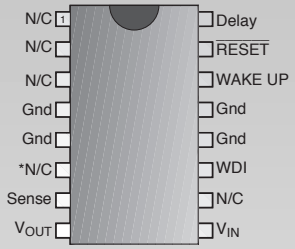


Features

- **5V ±2% / 100 mA Output Voltage**
- **Micropower Compatible Control Functions:**
  - **WAKE UP**
  - **WATCHDOG**
  - **$\overline{\text{RESET}}$**
- **Low Dropout Voltage: 400mV @ 100mA**
- **Low Sleep Mode Quiescent Current (400μA typ)**
- **Protection Features:**
  - **Thermal Shutdown**
  - **Short Circuit**
  - **74V Load Dump**
  - **Reverse Transient (-50V)**

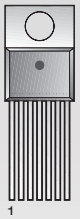
Package Options

16 Lead PDIP
16 Lead SOIC Wide*
(Internally Fused)

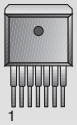


* For SO Wide package, pin # 6 is Gnd

7 Lead TO-220
Tab (Gnd)



7 Lead D²PAK
Tab (Gnd)



1. V_{OUT}
2. V_{IN}
3. WDI
4. Gnd
5. WAKE UP
6. $\overline{\text{RESET}}$
7. Delay

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Absolute Maximum Ratings

Power Dissipation ..... Internally Limited
Output Current (V_{OUT}, $\overline{RESET}$, WAKE UP) ..... Internally Limited
Reverse Battery ..... -15V
Maximum Load Dump Transient ..... +74V
Maximum Negative Transient (t<2ms) ..... -50V
ESD Susceptibility (Human Body Model) 2kV
ESD Susceptibility (Machine Model) 200V
Logic Inputs/Outputs ..... -0.3V to +6V
Storage Temperature Range ..... -55°C to +150°C
Lead Temperature Soldering
Wave Solder (through hole styles only) ..... 10 sec. max, 260°C peak
Reflow (SMD styles only) ..... 60 sec. max above 183°C, 230°C peak

Electrical Characteristics: T_A = -40°C to +125°C, -40°C ≤ T_J ≤ 150°C, 6V ≤ V_{IN} ≤ 26V, I_{OUT} = 100μA to 100mA, C_2 = 47μF (ESR < 8Ω), C_{Delay} = 0.1μF (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Output Section					
Output Voltage, V_{OUT}	9V < V_{IN} < 16V	4.90	5.00	5.10	V
	6V < V_{IN} < 26V, 0 < I_{OUT} < 100mA	4.85	5.00	5.15	V
Dropout Voltage (V_{IN} - V_{OUT})	I_{OUT} = 100mA		400	600	mV
	I_{OUT} = 100μA		100	150	mV
Load Regulation	V_{IN} = 14V, 100μA < I_{OUT} < 100mA		10	50	mV
Line Regulation	I_{OUT} = 1mA, 6V < V_{IN} < 26V		10	50	mV
Ripple Rejection	7V < V_{IN} < 17V @ f = 120Hz, I_{OUT} = 100mA	60	75		dB
Current Limit	V_{OUT} = 4.5V	100	250		mA
Thermal Shutdown		150	180	210	°C
Overvoltage Shutdown	V_{OUT} < 1V	50	56	62	V
Quiescent Current	I_{OUT} = 200μA (Sleep)		0.40	0.75	mA
	I_{OUT} = 50mA		4		mA
	I_{OUT} = 100mA (WAKE UP)		12	20	mA
Reverse Current	V_{OUT} = 5V, V_{IN} = 0V		1.0	1.5	mA
■ $\overline{RESET}$					
Threshold High (RTH)	RTH V_{OUT} Increasing	V_{OUT} - 0.3		V_{OUT} - 0.04	V
Threshold Low (RTL)	RTL V_{OUT} Decreasing	4.50	4.70	4.91	V
Hysteresis	RTH – RTL	150	200	250	mV
Output					
LOW	1V < V_{OUT} < RTL, I_{OUT} = 25μA		0.2	0.8	V
HIGH	I_{OUT} = 25μA, V_{OUT} > RTH	3.8	4.2	5.1	V
Current Limit	$\overline{RESET}$ = 0V, V_{OUT} > V_{RTH} (sourcing)	0.025	0.50	1.30	mA
	$\overline{RESET}$ = 5V, V_{OUT} > 1V (sinking)	0.1	12	80	mA
Delay Time	POR Mode	3	5	7	ms

Electrical Characteristics: continued

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ WATCHDOG Input					
Threshold					
HIGH			1.4	2.0	V
LOW		0.8	1.3		V
Hysteresis		25	100		mV
Input Current	0 < WDI < 6V	-10	0	+10	μA
Pulse Width	50% WDI falling edge to 50% WDI rising edge and 50% WDI rising edge to 50% WDI falling edge (see Figure 1)	5			μs
■ WAKE UP Output					
WAKE UP Period	see Figure 1a	30	40	50	ms
WAKE UP Duty Cycle nominal	see Figure 1c	40	50	60	%
$\overline{\text{RESET}}$ HIGH to WAKE UP Rising Delay Time	50% $\overline{\text{RESET}}$ rising edge to 50% WAKE UP edge (see Figure 1)	15	20	25	ms
WAKE UP Response to Watchdog Input	50% WDI falling edge to 50% WAKE UP falling edge		2	10	μs
WAKE UP Response to $\overline{\text{RESET}}$	50% $\overline{\text{RESET}}$ falling edge to 50% WAKE UP falling edge V_{OUT} = 5V→4.5V		2	10	μs
Output					
LOW	I_{OUT} = 25μA(sinking)		0.2	0.8	V
HIGH	I_{OUT} = 25μA(sourcing)	3.8	4.2	5.1	V
Current Limit	WAKE UP = 5V	0.025	1.00	7.00	mA
	WAKE UP = 0V	.05		3.50	mA

Package Lead Description

Package Lead #			Lead Symbol	Function
7L TO-220 & 7L D²PAK	**16 L PDIP** *(internally fused)*	**16L SOIC** *(internally fused)*		
2	9	9	V_{IN}	Supply voltage to the IC.
3	11	11	WDI	CMOS/TTL compatible input lead. The watchdog function monitors the falling edge of the incoming signal.
4	4,5,12,13	4,5,6,12,13	Gnd	Ground Connection
7	16	16	Delay	Input lead from timing capacitor for $\overline{\text{RESET}}$ and WAKE UP signal.
6	15	15	$\overline{\text{RESET}}$	CMOS/TTL compatible output lead $\overline{\text{RESET}}$ goes low whenever V_{OUT} drops by more than 6% from nominal, or during the absence of a correct watchdog signal.
5	14	14	WAKE UP	CMOS/TTL compatible output consisting of a continuously generated signal used to WAKE UP the microprocessor from sleep mode.
1	8	8	V_{OUT}	Regulated output voltage 5V ± 2%.
	7	7	Sense	Kelvin connection which allows remote sensing of the output voltage for improved regulation. If remote sensing is not required, connect to V_{OUT}.

Timing Diagrams

Figure 1a. Power Up, Sleep Mode and Normal Operation

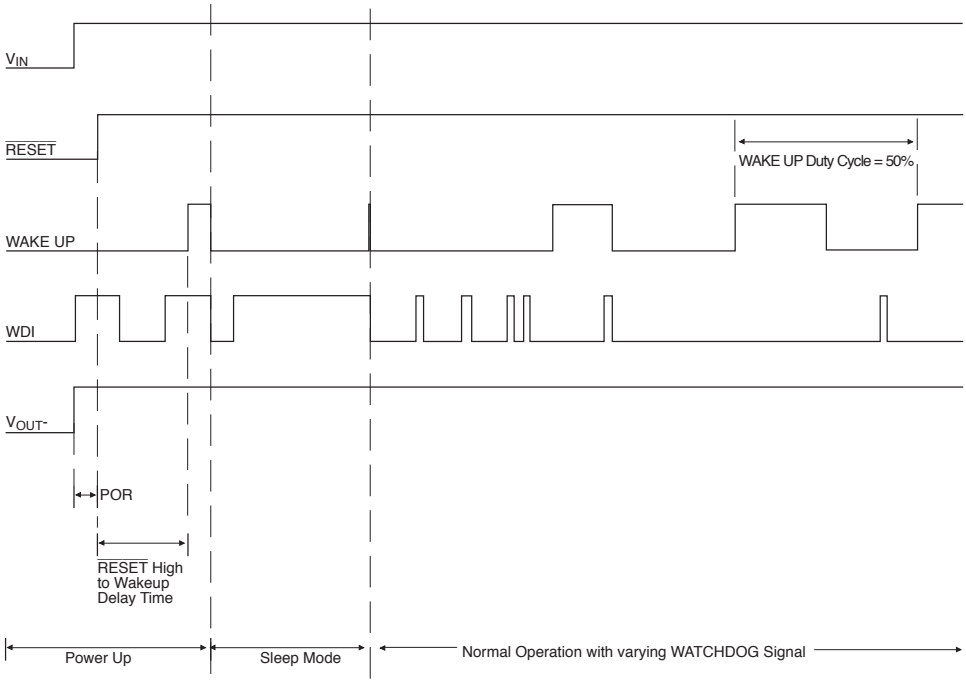


Figure 1b. Error Condition: Watchdog remains LOW and a $\overline{\text{RESET}}$ is issued

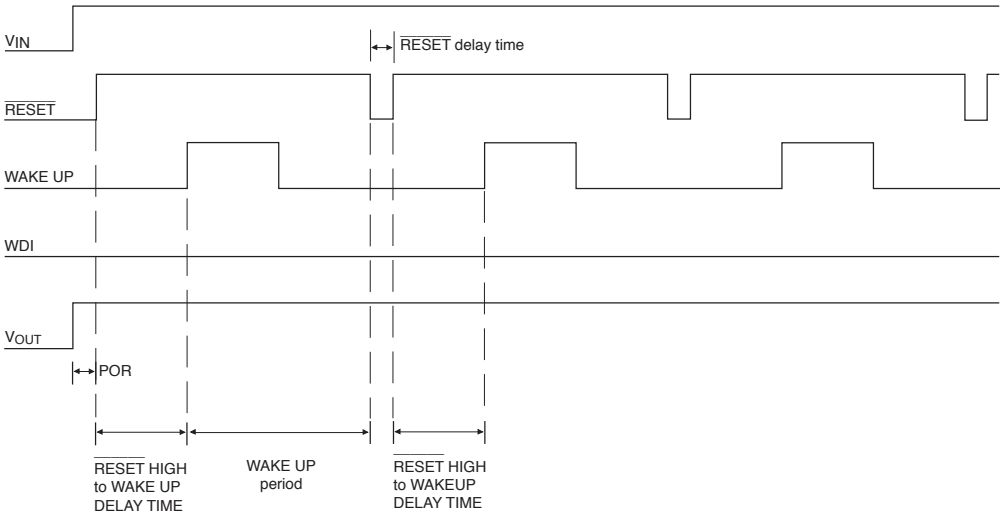
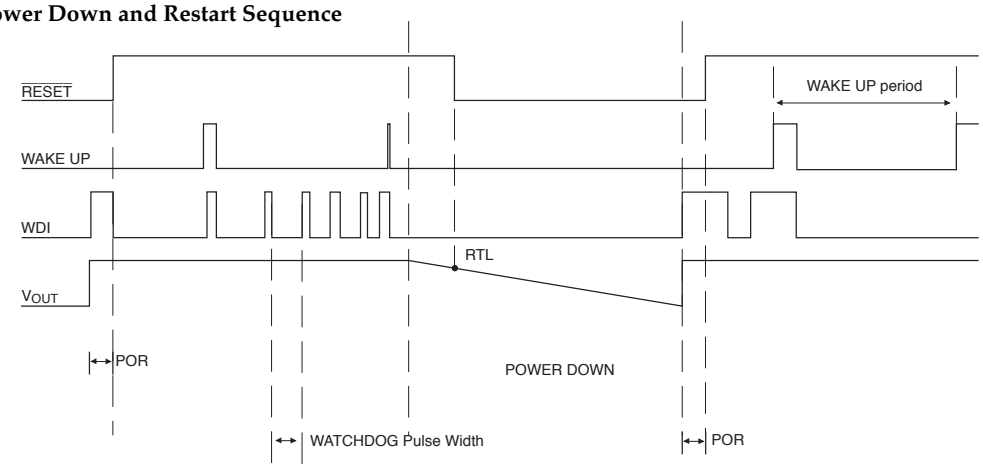


Figure 1c. Power Down and Restart Sequence



Definition of Terms

Dropout Voltage:
The input-output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100mV from the nominal value obtained at 14V input, dropout voltage is dependent upon load current and junction temperature.

Input Voltage:
The DC voltage applied to the input terminals with respect to ground.

Line Regulation:
The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation:
The change in output voltage for a change in load current at constant chip temperature.

Quiescent Current:
The part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

Ripple Rejection:
The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

Current Limit:
Peak current that can be delivered to the output.

Circuit Description

Functional Description

To reduce the drain on the battery a system can go into a low current consumption mode when ever its not performing a main routine. The WAKE UP signal is generated continuously and is used to interrupt a microcontroller that is in sleep mode. The nominal output is a 5 volt square wave with a duty cycle of 50% at a frequency that is determined by a timing capacitor, C_{Delay}.

When the microprocessor receives a rising edge from the WAKE UP output, it must issue a watchdog pulse and check its inputs to decide if it should resume normal operations or remain in the sleep mode.

The first falling edge of the watchdog signal causes the WAKE UP to go low within 2μs (typ) and remain low until the next WAKE UP cycle (see Figure 2). Other watchdog pulses received within the same cycle are ignored (Figure 1).

During power up, $\overline{\text{RESET}}$ is held low until the output voltage is in regulation. During operation, if the output voltage shifts below the regulation limits, the RESET toggles low and remains low until proper output voltage regulation is restored. After the $\overline{\text{RESET}}$ delay, $\overline{\text{RESET}}$ returns high.

The WATCHDOG circuitry continuously monitors the input watchdog signal (WDI) from the microprocessor. The absence of a falling edge on the WATCHDOG input during one WAKE UP cycle will cause a $\overline{\text{RESET}}$ pulse to occur at the end of the WAKE UP cycle. (see Figure 1b).

The WAKE UP output is pulled low during a $\overline{\text{RESET}}$ regardless of the cause of the $\overline{\text{RESET}}$. After the $\overline{\text{RESET}}$ returns high, the WAKE UP cycle begins again (see Figures 1b).

The $\overline{\text{RESET}}$ pulse width, WAKE UP signal frequency and $\overline{\text{RESET}}$ high to WAKE UP delay time are all set by one external capacitor C_{Delay}.

WAKE UP period=$(4x10^5)C_{Delay}$

$\overline{\text{RESET}}$ Delay Time=$(5x10^4)C_{Delay}$

$\overline{\text{RESET}}$ HIGH to WAKE UP Delay Time =$(2x10^5)C_{Delay}$

Capacitor temperature coefficient and tolerance as well as the tolerance of the CS8151 must be taken into account in order to get the correct system tolerance for each parameter.

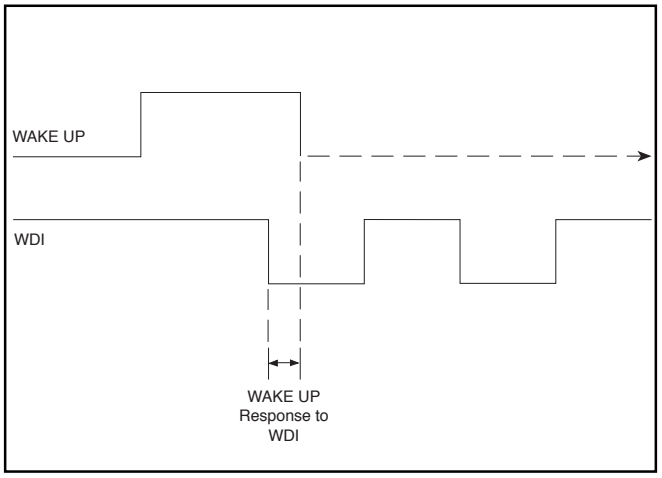


Figure 2. WAKE UP response to WDI

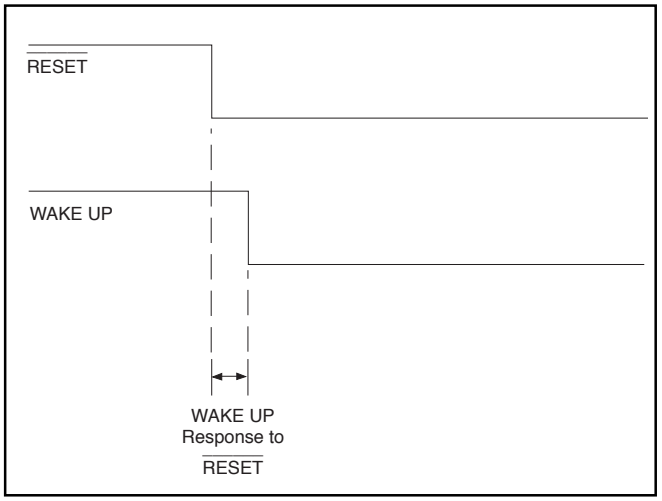


Figure 3. WAKE UP response to $\overline{\text{RESET}}$ (Low Voltage)

Application Notes

Output Stage Protection

The output stage is protected against overvoltage, short circuit and thermal runaway conditions (see Figure 4).

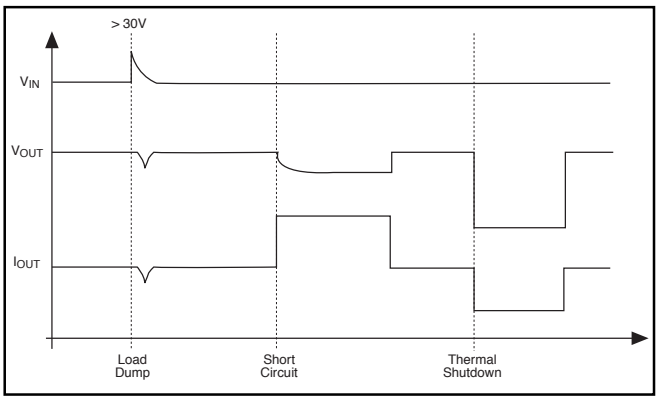


Figure 4: Typical Circuit Waveforms for Output Stage Protection.

If the input voltage rises above 56V (e.g. load dump), the output shuts down. This response protects the internal circuitry and enables the IC to survive unexpected voltage transients.

Should the junction temperature of the power device exceed 180˚C (typ) the power transistor is turned off. Thermal shutdown is an effective means to prevent die overheating since the power transistor is the principle heat source in the IC.

Stability Considerations

The output or compensation capacitor C_2 (see Figure 5) helps determine three main characteristics of a linear regulator: start-up delay, load transient response and loop stability.

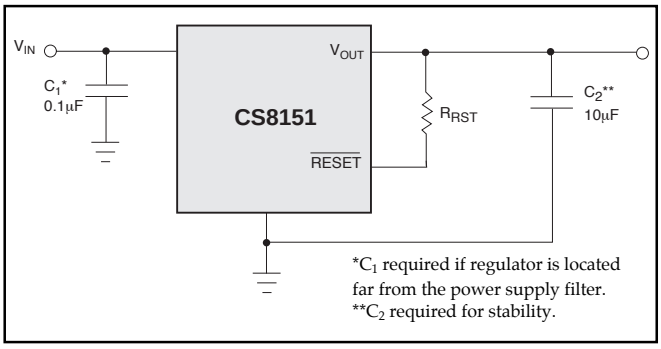


Figure 5. Test and application circuit showing output compensation.

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (-25°C to -40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provide this information.

The value for the output capacitor C_2 shown in the test and applications circuit should work for most applications, however it is not necessarily the optimized solution.

To determine an acceptable value for C_2 for a particular application, start with a tantalum capacitor of the recommended value and work towards a less expensive alternative part.

Step 1: Place the completed circuit with a tantalum capacitor of the recommended value in an environmental chamber at the lowest specified operating temperature and monitor the outputs with an oscilloscope. A decade box connected in series with the capacitor will simulate the higher ESR of an aluminum capacitor. Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible.

Step 2: With the input voltage at its maximum value, increase the load current slowly from zero to full load while observing the output for any oscillations. If no oscillations are observed, the capacitor is large enough to ensure a stable design under steady state conditions.

Step 3: Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause the greatest oscillation. This represents the worst case load conditions for the regulator at low temperature.

Step 4: Maintain the worst case load conditions set in step 3 and vary the input voltage until the oscillations increase. This point represents the worst case input voltage conditions.

Step 5: If the capacitor is adequate, repeat steps 3 and 4 with the next smaller valued capacitor. A smaller capacitor will usually cost less and occupy less board space. If the output oscillates within the range of expected operating conditions, repeat steps 3 and 4 with the next larger standard capacitor value.

Step 6: Test the load transient response by switching in various loads at several frequencies to simulate its real working environment. Vary the ESR to reduce ringing.

Step 7: Remove the unit from the environmental chamber and heat the IC with a heat gun. Vary the load current as instructed in step 5 to test for any oscillations.

Once the minimum capacitor value with the maximum ESR is found, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of ±20% so the minimum value found should be increased by at least 50% to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitor should be less than 50% of the maximum allowable ESR found in step 3 above.

Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 6) is:

$$P_{D(max)} = \{V_{IN(max)} - V_{OUT(min)}\}I_{OUT(max)} + V_{IN(max)}I_Q \qquad (1)$$

where:

$V_{IN(max)}$ is the maximum input voltage,

$V_{OUT(min)}$ is the minimum output voltage,

$I_{OUT(max)}$ is the maximum output current for the application, and

I_Q is the quiescent current the regulator consumes at $I_{OUT(max)}$.

Application Diagram

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\Theta JA}$ can be calculated:

$$R_{\Theta JA} = \frac{150°C - T_A}{P_D} \quad (2)$$

The value of $R_{\Theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\Theta JA}$'s less than the calculated value in equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

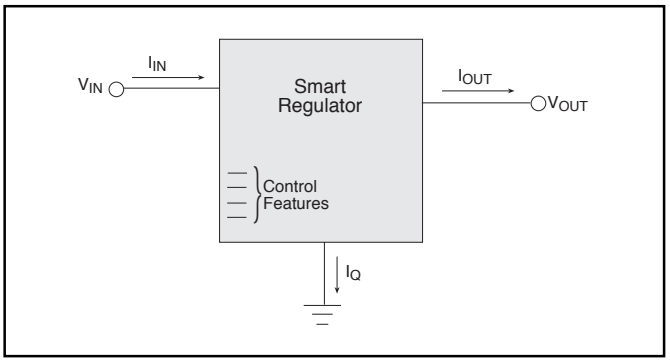


Figure 6. Single output regulator with key performance parameters labeled.

Heat Sinks

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\Theta JA}$:

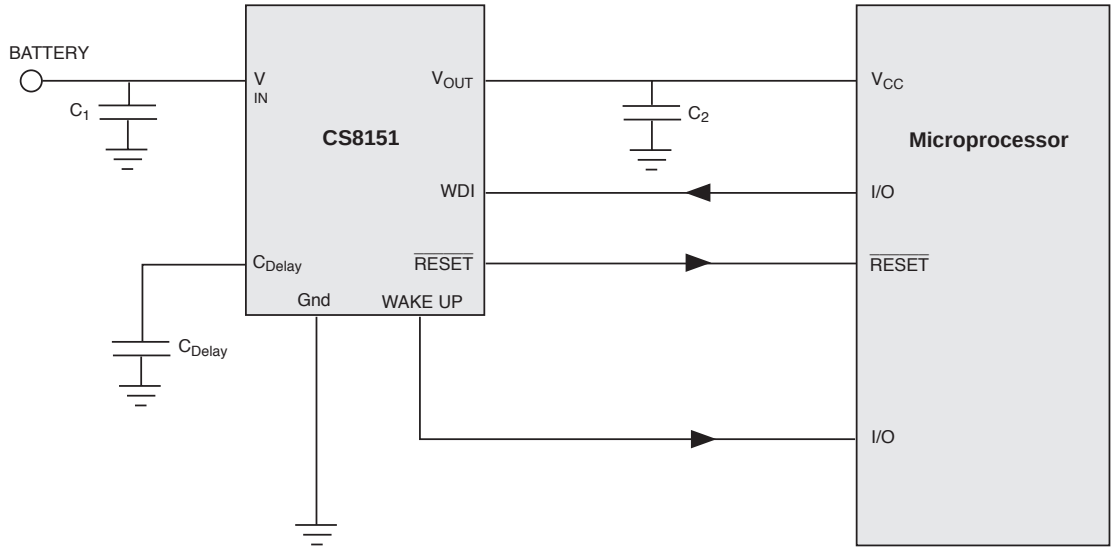
$$R_{\Theta JA} = R_{\Theta JC} + R_{\Theta CS} + R_{\Theta SA} \quad (3)$$

where:

$R_{\Theta JC}$ = the junction–to–case thermal resistance,
$R_{\Theta CS}$ = the case–to–heatsink thermal resistance, and
$R_{\Theta SA}$ = the heatsink–to–ambient thermal resistance.

$R_{\Theta JC}$ appears in the package section of the data sheet. Like $R_{\Theta JA}$, it too is a function of package type. $R_{\Theta CS}$ and $R_{\Theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

Application Diagram

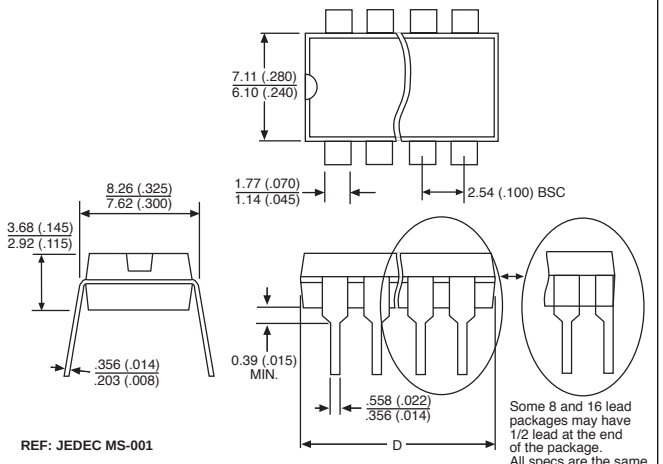


Package Specification

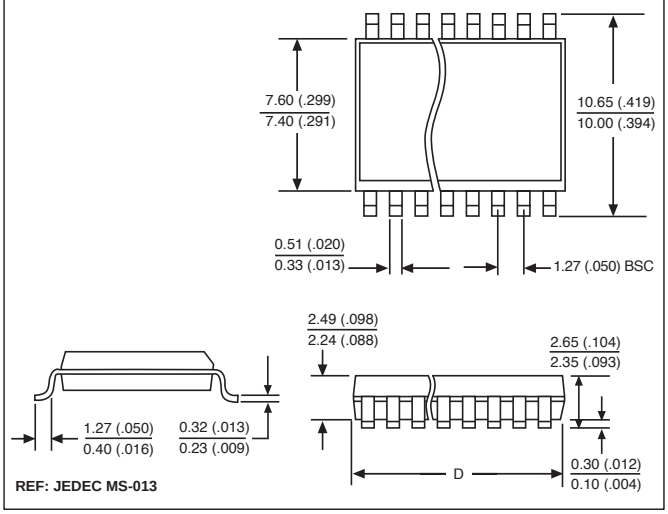
PACKAGE DIMENSIONS IN mm (INCHES)

Lead Count	D			
	Metric		English	
	Max	Min	Max	Min
16L PDIP *(Internally Fused Leads)*	19.69	18.67	.775	.735
16L SOIC Wide *(Internally Fused Leads)*	10.50	10.10	.413	.398

Plastic DIP (N); 300 mil wide



Surface Mount Wide Body (DW); 300 mil wide



Ordering Information

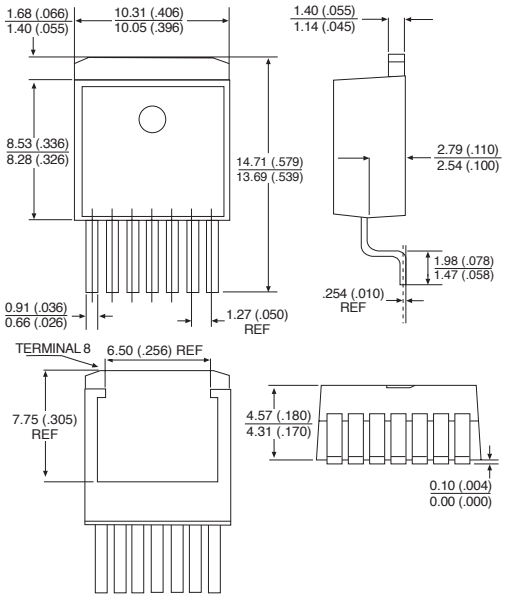
Part Number	Description
CS8151YT7	7 lead TO-220 Straight
CS8151YTVA7	7 lead TO-220 Vertical
CS8151YDPS7	7 lead D^{2}PAK Short-Leaded
CS8151YDPSR7	7 lead D^{2}PAK Short-Leaded *(tape & reel)*
CS8151YNF16	16 lead PDIP (*Internally Fused Leads)*
CS8151YDWF16	16 lead SOIC Wide (*Internally Fused Leads)*
CS8151YDWFR16	16 lead SOIC Wide (*Internally Fused Leads) (tape & reel)*

PACKAGE THERMAL DATA

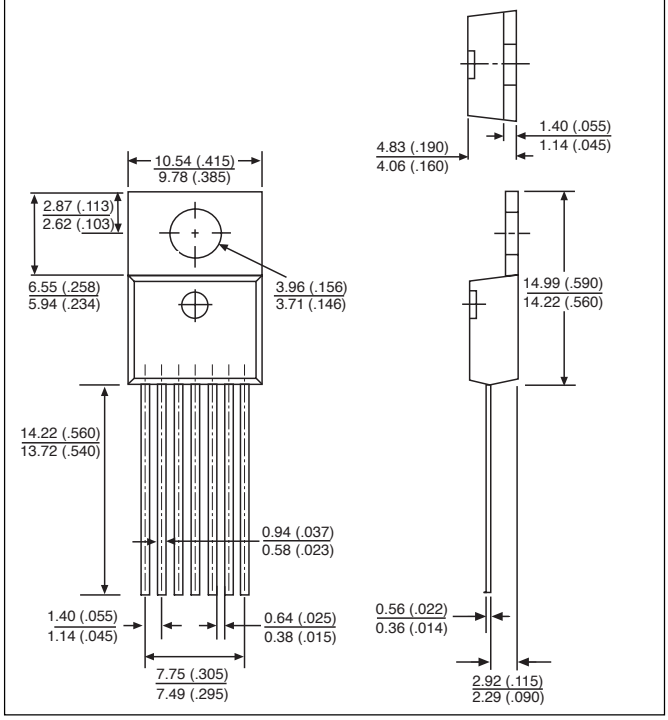
Thermal Data		7 Lead TO-220	7 Lead D^{2}PAK	16 Lead PDIP	16 Lead SOIC Wide	
$R_{\Theta JC}$	typ	1.8	1.8	15	18	°C/W
$R_{\Theta JA}$	typ	50	10-50*	50	75	°C/W

**Depending on thermal properties of substrate.* $R_{\Theta JA} = R_{\Theta JC} + R_{\Theta CA}$

7 Lead D^{2}PAK (DPS)* Short-Leaded



7 Lead TO-220 (T) Straight



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