

FEATURES

- Total of 33 single word instructions .
- The fast execution time may be 200ns for all single cycle instructions under 20MHz operating.
- Operating voltage range: 2.3V ~ 6.5V
- 8-bit data bus.
- 14-bit instruction word.
- Four-level stacks.
- On chip EPROM size : 512x14 bits for CTM8B54E/55E, 1Kx14 bits for CTM8B56E, 2Kx14 bits for CTM8B57E.
- Internal RAM size : 25 bytes for CTM8B54E/56E, 24 bytes for CTM8B55E, 72 bytes for CTM8B57E.
- Direct and indirect addressing modes for data accessing
- 8-bit real time clock/counter with 8-bit programmable prescaler.
- Internal power-on Reset.
- Device Reset Timer.
- Code protection.
- Sleep mode for power saving.
- On chip Watchdog Timer(WDT) based on internal RC oscillator.
- Three I/O ports PA, PB nad PC with independent direction control.

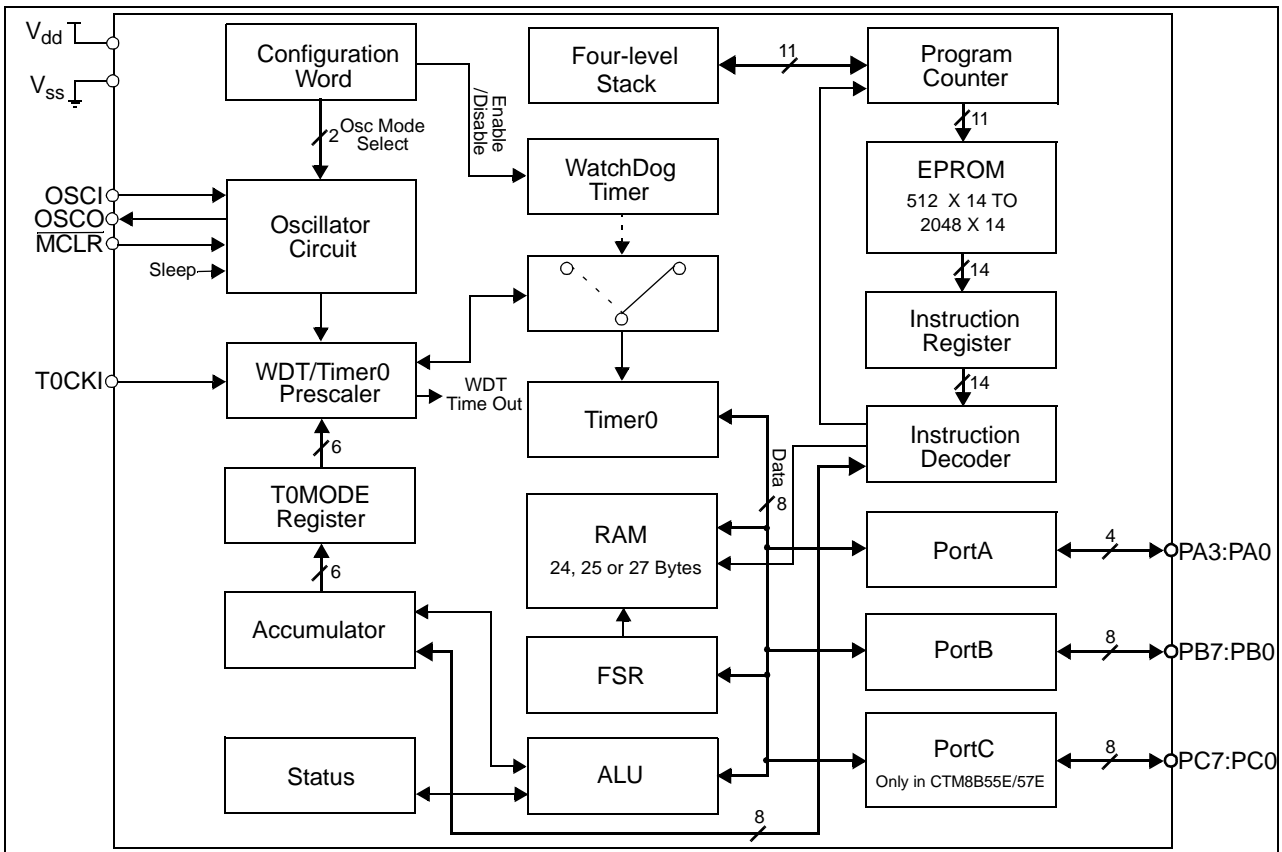
- 4 types of oscillator can be selected by code options:
 - RC : Low-cost RC oscillator
 - XTAL : Standard crystal oscillator
 - HFXTAL : High frequency crystal oscillator
 - LFXTAL : Low frequency crystal oscillator

GENERAL DESCRIPTION

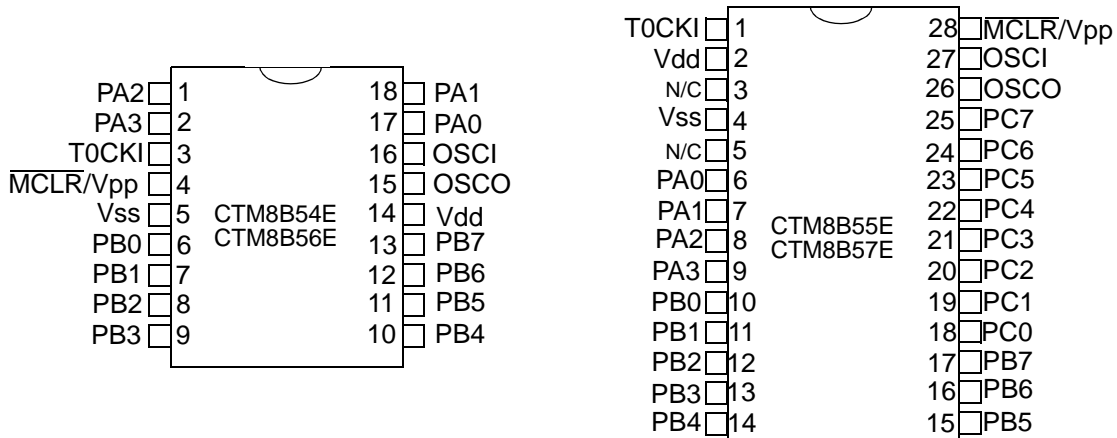
CTM8B5X series is an EPROM based 8-bit microcontroller which employs a full CMOS technology enhanced with low-cost, high speed and high noise immunity. Watchdog Timer, RAM, EPROM, tri-state I/O port, power down mode, and real time programmable clock/counter are integrated into this chip. CTM8B5X contains 33 instructions, all are single cycle except for program branches which take two cycles.

On chip memory is available with 512x14 bits of EPROM for CTM8B54E/55E, 1Kx14 bits of EPROM for CTM8B56E, 2Kx14 bits of EPROM for CTM8B57E and 24 to 72 bytes of static RAM.

BLOCK DIAGRAM



* All specs and applications shown above subject to change without prior notice.

1.0 PIN CONNECTION

2.0 PIN DESCRIPTIONS

Name	I/O	Descriptions
OSCI	I	RC type: Input pin of RC oscillator XTAL type: Input terminal of crystal oscillator
OSCO	O	RC type: OSCO outputs with 1/4 frequency of OSCI to denotes the cycle rate for instruction. XTAL type: Output terminal of crystal oscillator
T0CKI/SCL	I	Input pin of real time counter/clock. Must be tied to Vss or Vdd if not in use.
MCLR/Vpp	I	Input pin for device reset or high voltage programming input for EPROM. If this pin is low, the device is reset. In programming mode, this pin is connected to 12V. In normal operating mode, this pin must not exceed Vdd to avoid entering unintended programming mode.
PA0~PA3	I/O	PA0~PA3 as bi-directional I/O port
PB0~PB7	I/O	PB0~PB7 as bi-directional I/O port
PC0~PC7	I/O	PC0~PC7 as bi-directional I/O port
Vdd	-	Power supply
Vss	-	Ground

* All specs and applications shown above subject to change without prior notice.

3.0 FUNCTIONAL DESCRIPTIONS

3.1 REGISTER MAP

The register map of CTM8B5X is depicted as below:

The Register Map of CTM8B54E/56E

Address	Description
00h	Indirect Addressing Register
01h	Timer0
02h	PC
03h	STATUS
04h	FSR
05h	PORTA
06h	PORTB
07h-1Fh	General Purpose Register

The Register Map of CTM8B55E

Address	Description
00h	Indirect Addressing Register
01h	Timer0
02h	PC
03h	STATUS
04h	FSR
05h	PORTA
06h	PORTB
07h	PORTC
08h-1Fh	General Purpose Register

The Register Map of CTM8B57E

Address	Description			
	Bank 0 00	Bank 1 01	Bank 2 10	Bank 3 11
00h	Indirect Addressing Register	Map back to address in Bank 0		
01h	Timer0			
02h	PC			
03h	STATUS			
04h	FSR			
05h	PORTA			
06h	PORTB			
07h	PORTC			
08h~0Fh	General Purpose Register			
	10h~1Fh General Purpose Register	30h~3Fh General Purpose Register	50h~5Fh General Purpose Register	70h~7Fh General Purpose Register

* All specs and applications shown above subject to change without prior notice.

3.1.1 INAR(Indirect Address Register) : R0

R0 is not a physically implemented register. It is used as an indirect addressing pointer. Any instruction accessing this register can access data pointed by FSR(R4).

3.1.2 Timer0(8-bit real-time clock/timer) : R1

This register increases by an external signal edge applied to T0CKI pin, or by internal instruction cycle. It can be read or written as any other register.

3.1.3 PC(Program Counter) : R2

This register increases itself every instruction cycle, except the following condition shown in Figure 1:

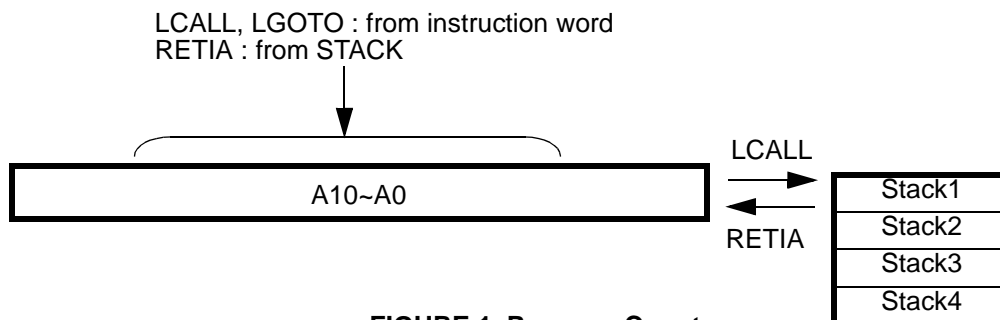


FIGURE 1. Program Counter

3.1.4 STATUS(Status Register): The content of R3 is listed in Table 1.

TABLE 1. STATUS Register

Bit	Symbol	Description
0	C	Carry/borrow bit ADDWF = 1, a carry occurred = 0, a carry did not occur SUBWF = 1, a borrow did not occur = 0, a borrow occurred
1	DC	Half carry/half borrow bit ADDWF = 1, a carry from the 4th low order bit of the result occurred = 0, a carry from the 4th low order bit of the result did not occur SUBWF = 1, a borrow from the 4th low order bit of the result did not occur = 0, a borrow from the 4th low order bit of the result occurred
2	Z	Zero bit: = 1, the result of a logic operation is zero = 0, the result of a logic operation is not zero
3	\overline{PD}	Power down flag bit: = 1, after power-up or by the CLRWDT instruction = 0, by the SLEEP instruction
4	\overline{TO}	Time overflow flag bit: = 1, after power-up or by the CLRWDT or SLEEP instruction = 0, a WDT time-overflow occurred
5, 6, 7	-	Unused

* All specs and applications shown above subject to change without prior notice.

3.1.5 FSR(File select register pointer): R4

Bit 0~4 are used to select up to 32 registers (address: 00h~1Fh) and Bit 5~6 are Bank Select (Bank0~3) in the indirect addressing mode shown in Figure 2.

3.1.6 PORT A: R5

PA3:PA0, bi-directional I/O Register

3.1.7 PORT B: R6

PB7:PB0, bi-directional I/O Register

3.1.8 PORT C: R7

PB7:PB0, bi-directional I/O Register, and for MTU8B55E/57E only

3.1.9 T0MODE REGISTER: T0MODE is a write-only register and the content is listed in Table 2.

3.1.10 IOST (Control Port I/O Mode Register)

The IOST register is "write-only"
 = 0, I/O pin in output mode;
 = 1, I/O pin in input mode.

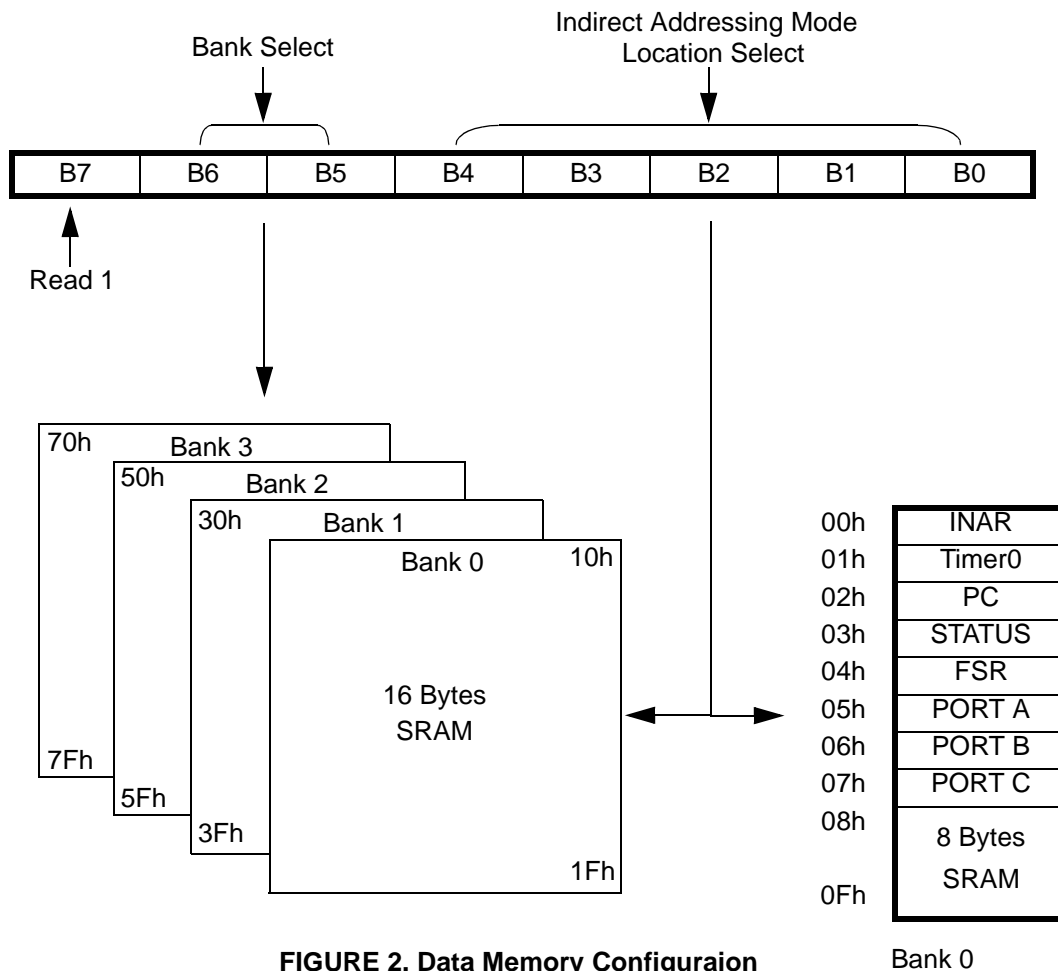


FIGURE 2. Data Memory Configuration

* All specs and applications shown above subject to change without prior notice.

TABLE 2. T0MODE Register

Bit	Symbol	Description		
		Bit Value	Timer Rate	WDT Rate
2-0	PS2:PS0	0 0 0	1:2	1:1
		0 0 1	1:4	1:2
		0 1 0	1:8	1:4
		0 1 1	1:16	1:8
		1 0 0	1:32	1:16
		1 0 1	1:64	1:32
		1 1 0	1:128	1:64
		1 1 1	1:256	1:128
3	PSC	Prescaler assign bit: = 0, Timer0 = 1, WDT		
4	TE	Timer0 source signal edge select bit: = 0, increment when low-to-high transition on T0CKI pin = 1, increment when high-to-low transition on T0CKI pin		
5	TS	Timer0 source signal select bit: = 0, internal instruction clock cycle = 1, transition on T0CKI pin		
6, 7	-	Unused		

* All specs and applications shown above subject to change without prior notice.

3.2 INSTRUCTION SET

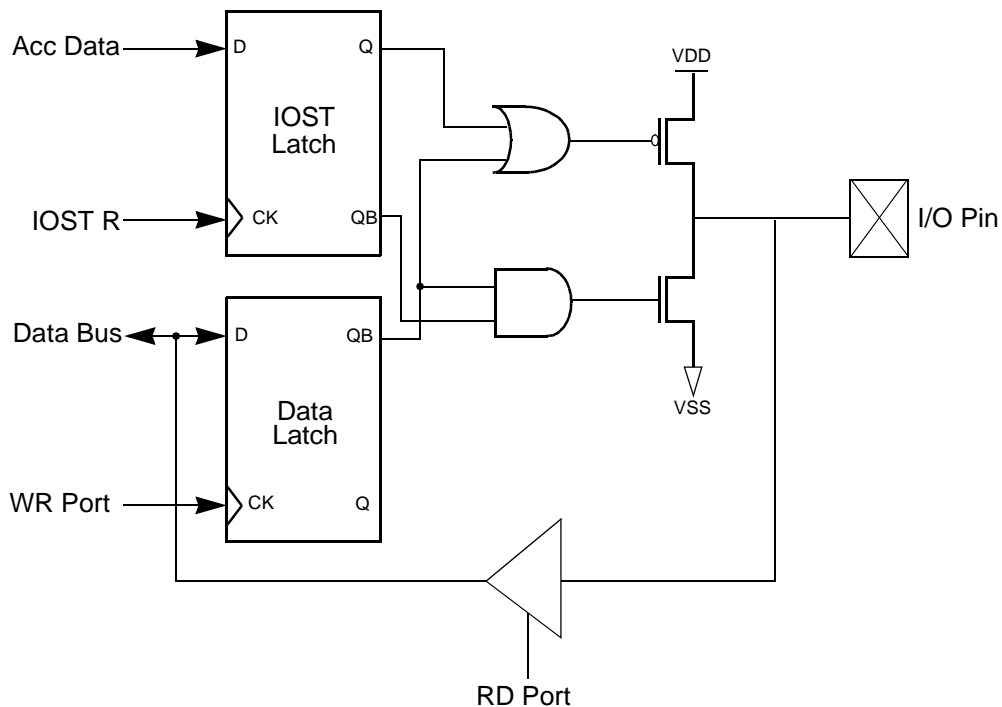
Mnemonic Operands	Description	Cycles	Instruction Code	Status Affected
BCR R, bit	Clear bit in R	1	11 11bb brrr rrrr	None
BSR R, bit	Set bit in R	1	11 10bb brrr rrrr	None
BTRSC R, bit	Test bit in R and skip if clear	1 or 2(skip)	11 01bb brrr rrrr	None
BTRSS R, bit	Test bit in R and skip if set	1 or 2(skip)	11 00bb brrr rrrr	None
CLRWDT	Clear Watchdog Timer	1	01 0000 0000 0001	\overline{TO} , \overline{PD}
T0MODE	Load T0MODE Register	1	01 0000 0000 0010	None
SLEEP	Go into standby mode	1	01 0000 0000 0011	\overline{TO} , \overline{PD}
IOST R	Load IOST Register	1	01 0000 0000 0rrr	None
ANDIA I	AND immediate with Acc	1	00 1001 iiiii iiiii	Z
XORIA I	Exclusive OR immediate with Acc	1	00 1000 iiiii iiiii	Z
MOVIA I	Move immediate to Acc	1	00 0001 iiiii iiiii	None
IORIA I	Inclusive OR immediate with Acc	1	00 0011 iiiii iiiii	Z
RETIA I	Return, place immediate in A	2	00 1100 iiiii iiiii	None
LCALL I	Call subroutine	2	10 0iii iiiii iiiii	None
LGOTO I	Unconditional branch	2	10 1iii iiiii iiiii	None
NOP	No operation	1	01 0000 0000 0000	None
MOVAR R	Move Acc to R	1	01 0000 lrrr rrrr	None
COMR R, d	Complement R	1	01 0010 drrr rrrr	Z
MOVR R	Move R	1	01 0011 drrr rrrr	Z
RRR R, d	Rotate right R	1	01 1110 drrr rrrr	C
RLR R, d	Rotate left R	1	01 1100 drrr rrrr	C
SWAPR R, d	Swap halves R	1	01 1101 drrr rrrr	None
CLRA	Clear Acc	1	01 0001 0000 0000	Z
CLRR R	Clear R	1	01 0001 lrrr rrrr	Z
INCR R, d	Increment R	1	01 1000 drrr rrrr	Z
INCRSZ R, d	Increment R, Skip if 0	1 or 2(skip)	01 1001 drrr rrrr	None

* All specs and applications shown above subject to change without prior notice.

Mnemonic Operands	Description	Cycles	Instruction Code	Status Affected
DECR R, d	Decrement R	1	01 0110 drrr rrrr	Z
DECRSZ R, d	Decrement R, Skip if 0	1 or 2(skip)	01 0111 drrr rrrr	None
SUBAR R, d	Subtract Acc from R	1	01 1010 drrr rrrr	C, DC, Z
XORAR R, d	Exclusive OR Acc with R	1	01 1011 drrr rrrr	Z
ANDAR R, d	AND Acc with R	1	01 0100 drrr rrrr	Z
ADDAR R, d	Add Acc and R	1	01 0101 drrr rrrr	C, DC, Z
IORAR R, d	Inclusive OR Acc with R	1	01 1111 drrr rrrr	Z

Note: b : Bit position WDT : Watchdog Timer R : Register address
i : Immediate data Acc : Accumulator TOMODE : TOMODE register
PD : Power down flag TO : Time overflow bit IOST : I/O port status register
Z : Zero flag C : Carry flag DC : Digital carry flag
I : (i₇i₆i₅i₄i₃i₂i₁i₀) R : (r₆r₅r₄r₃r₂r₁r₀)
d ∈ [0, 1]: Destination
If d is "0", the result is stored in the Acc register.
If d is "1", the result is stored back in register R.

3.3 I/O PORTS EQUIVALENT CIRCUIT



Note : 1. The IOST registers are "write-only" and set upon RESET.
2. If the IOST latch is "0", the corresponding I/O pin is in output mode;
if the IOST latch is "1", the corresponding I/O pin is in input mode.

* All specs and applications shown above subject to change without prior notice.

3.4 RESET

This device may be reset by one of the following ways:

- (1) Power-on Reset : At power-up, this device will be kept in a RESET condition for a period of 18ms after the voltage on MCLR/V_{pp} pin has reached a logic high level.
- (2) MCLR reset (normal operation).
- (3) WDT reset (normal operation).
- (4) MCLR wake-up (from sleep mode).
- (5) WDT wake-up (from sleep mode) : Executing the SLEEP instruction can force this device entering into sleep mode (power saving mode). While in sleep mode, the WDT is cleared but keeps running. This device can be awakened by WDT time-out or reset input on MCLR pin.

The contents of registers after reset are listed below:

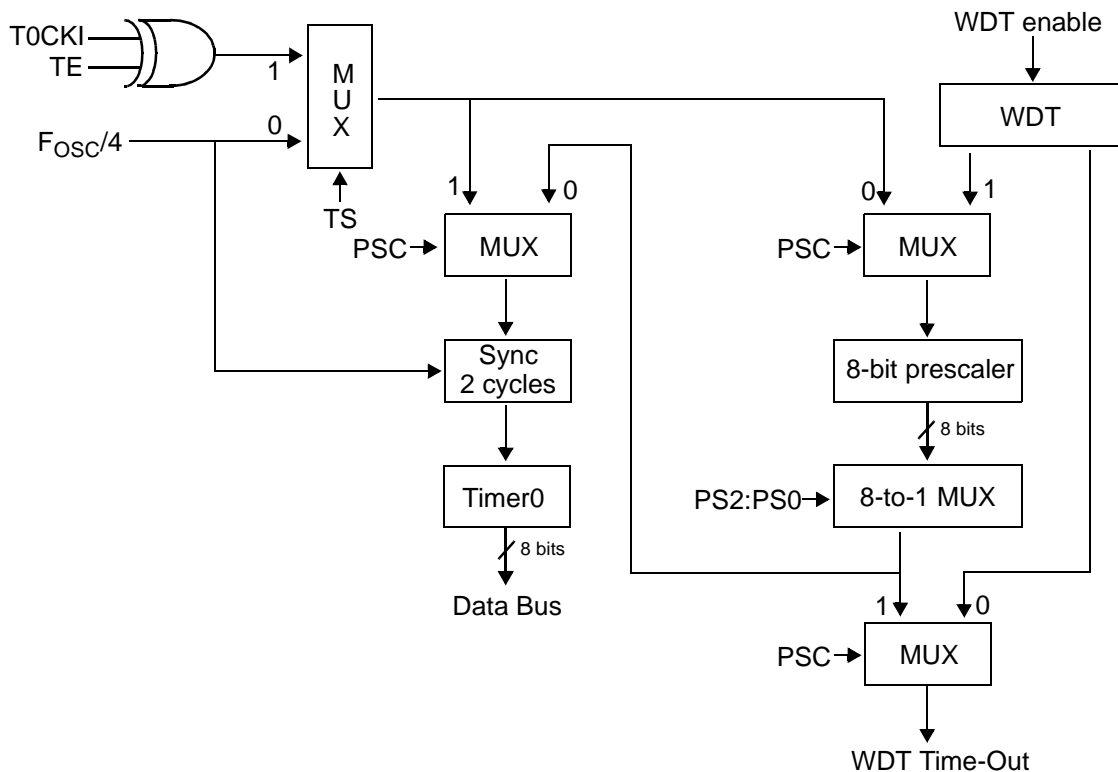
Address	Register	Power-On Reset	/MCLR or WDT Reset
00h	INAR	xxxx xxxx	uuuu uuuu
01h	Timer0	xxxx xxxx	uuuu uuuu
02h	PC	1111 1111	1111 1111
03h	STATUS	0001 1xxx	000# #uuu
04h	FSR	1xxx xxxx	1uuu uuuu
05h	PORTA	---- xxxx	---- uuuu
06h	PORTB	xxxx xxxx	uuuu uuuu
07h	PORTC	xxxx xxxx	uuuu uuuu
07h-1Fh	General Purpose Register	xxxx xxxx	uuuu uuuu
N/A	Acc	xxxx xxxx	uuuu uuuu
N/A	IOST	1111 1111	1111 1111
N/A	T0MODE	--11 1111	--11 1111

Note: x = unknown, u = unchanged, - = unimplemented, read as "0",
 # = refer to the following table

Condition	Status:bit 4	Status:bit 3
/MCLR Reset (not during SLEEP)	u	u
/MCLR Reset during SLEEP	1	0
WDT Reset (not during SLEEP)	0	1
WDT Reset during SLEEP	0	0

* All specs and applications shown above subject to change without prior notice.

3.5 REAL TIME CLOCK (TIMER0) AND WATCHDOG TIMER



3.5.1 Timer0

Timer0 is an 8-bit timer/counter. The clock source of Timer0 can come from the internal clock or by an external clock source presented at the T0CKI pin.

To select the internal clock source, bit 5 of the T0MODE register should be reset. In this mode, Timer0 will increase by 1 in every instruction cycle (without prescaler).

To select the external clock source, bit 5 of the T0MODE register should be set. In this mode, Timer0 will increase by 1 on every falling or rising edge of T0CKI pin is controlled by bit 4 of T0MODE register.

3.5.2 Watchdog Timer(WDT)

The Watchdog Timer is a free running on-chip RC oscillator. This RC oscillator is separated from the RC oscillator of the OSCI pin. That means the WDT will keep running even when the oscillator driver is turned off, such as in sleep mode. During normal operation or in sleep mode, a WDT time-out will cause the device reset and the TO bit (bit 4 of STATUS register) will be cleared.

Without prescaler, the WDT time-out period is 18ms. This period can be increased by using the prescaler. The division ratio of prescaler is up to 1:128. Thus, the longest time-out period is approximately 2.3s.

3.5.3 Prescaler

The 8-bit prescaler may be assigned to either the Timer0 or the WDT through the PSC bit (bit 3 of the T0MODE register). Setting this bit assigns the prescaler to the WDT. Resetting this bit assigns the prescaler to the Timer0. The PS2:PS0 bits determine the prescale ratio. When assigned to Timer0, the prescaler will be cleared by instructions which write to Timer0 Register. A CLRWDT instruction will clear the WDT and prescaler when assigned to WDT. The prescaler can not be assigned to both the Timer0 and WDT simultaneously.

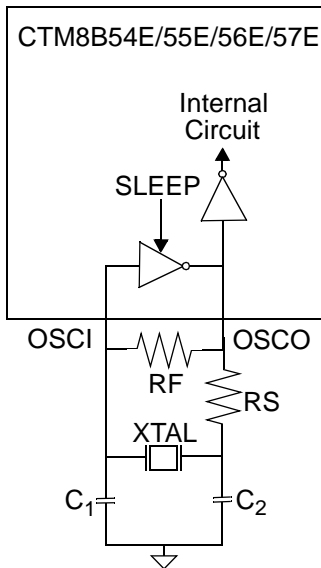
* All specs and applications shown above subject to change without prior notice.

3.6 OSCILLATOR CONFIGURATION

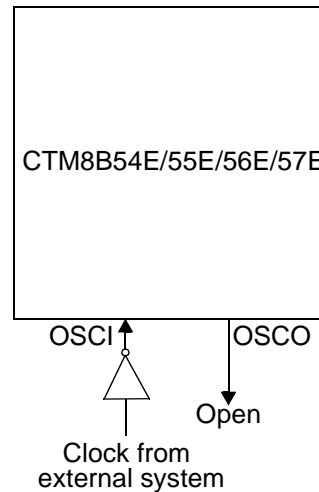
This device supports four oscillator modes. Users can program two configuration bits to select the appropriate mode. These oscillator modes offered as:

- RC: Low-cost crystal
- XTAL: Standard crystal oscillator
- HFXTAL: High frequency crystal oscillator
- LFXTAL: Low frequency crystal oscillator

3.6.1 XTAL, HFXTAL or LFXTAL modes

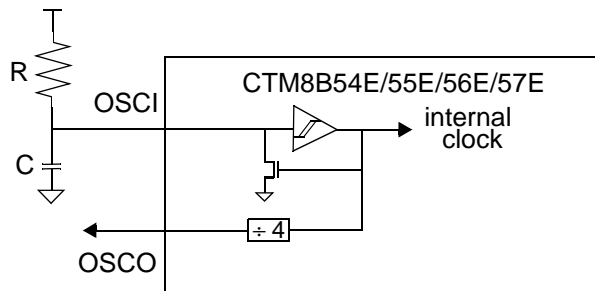


(a) Crystal Operation (or Ceramic Resonator)



(b) External Clock Input Operation

3.6.2 RC Oscillator Mode



3.7 CONFIGURATION WORD

Bit 3	Bit2	Bit1	Bit0	Function	Remark
Code Protect	WDT Enable	Oscillator Type	Oscillator Type		
1	x	x	x	EPROM unprotected	Default
0	x	x	x	EPROM protected	
x	1	x	x	Watchdog Timer enable	Default
x	0	x	x	Watchdog Timer disable	
x	x	1	1	RC	Default
x	x	1	0	HFXTAL	
x	x	0	1	XTAL	
x	x	0	0	LFXTAL	

* All specs and applications shown above subject to change without prior notice.

4.0 ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	-55°C to +125°C
Store Temperature	-65°C to +150°C
DC Supply Voltage (V_{dd})	0V to +7.5V
Voltage with respect to Ground (V_{ss})	0.6V to ($V_{dd} + 0.6$)V
Voltage on MCLR (V_{pp}) with respect to Ground (V_{ss})	0V to +12V

5.0 OPERATING CONDITIONS

DC Supply Voltage	+2.3V to +6.5V
Operating Temperature	-40°C to +85°C

6.0 ELECTRICAL CHARACTERISTICS (Under Operating Conditions)

6.1 ELECTRICAL CHARACTERISTICS of CTM8B54E/56E

Parameter	Sym	Min.	Typ.	Max.	Units	Conditions
Input High Voltage	V_{IH}		2.2		V	I/O ports, $V_{dd}=5V$
			4.2		V	MCLR, $V_{dd}=5V$
Input Low Voltage	V_{IL}		1.1		V	I/O ports, $V_{dd}=5V$
			1.0		V	MCLR, $V_{dd}=5V$
Output Voltage	V_{OH}	3.8			V	I/O Ports, $V_{dd}=4.5V$, $I_{oh}=-5.4mA$,
	V_{OL}			0.6	V	$I_{ol}=8.7mA$ in RC mode
Sleep Current	I_{PD}		3.0		μA	WDT Enable, $V_{dd}=3.0V$
	I_{PD}		<1		μA	WDT Disable, $V_{dd}=3.0V$
Operating Current	I_{DD}					HFXTAL: 24MHz, WDT Disable
			8.07		mA	$V_{dd}=6.4V$
			5.16		mA	$V_{dd}=5.0V$
			3.98		mA	$V_{dd}=4.0V$
			2.05		mA	$V_{dd}=3.0V$
	I_{DD}					LFXTAL: 32kHz, WDT Disable
			2.8		mA	$V_{dd}=6.4V$
			1.77		mA	$V_{dd}=5.0V$
			1.31		mA	$V_{dd}=4.0V$
			604		μA	$V_{dd}=3.0V$
			224		μA	$V_{dd}=2.4V$
	I_{DD}		88		μA	$V_{dd}=2.1V$ **
						XTAL: 12MHz, WDT Disable
			6.21		mA	$V_{dd}=6.4V$
			3.91		mA	$V_{dd}=5.0V$
		2.71		mA	$V_{dd}=4.0V$	
	1.39		mA	$V_{dd}=3.0V$		
	685		μA	$V_{dd}=2.4V$		

* All specs and applications shown above subject to change without prior notice.

Parameter	Sym	Min.	Typ.	Typ.	Units	Conditions			
Operating Current	I _{DD}		5.01		mA	XTAL: 4MHz, WDT Disable			
			3.03		mA	V _{dd} =6.4V			
			2.05		mA	V _{dd} =5.0V			
			916		uA	V _{dd} =4.0V			
			391		uA	V _{dd} =3.0V			
			195		uA	V _{dd} =2.1V **			
						V _{dd} =5V, RC mode, WDT Disable, These values include current through Rext			
			6.32		mA	C=3P	R=900Ohm	F=7.80MHz	
			3.11		mA		R=4.7kOhm	F=4.10MHz	
			2.46		mA		R=10kOhm	F=2.38MHz	
			1.88		mA		R=47kOhm	F=617kHz	
			1.80		mA		R=100kOhm	F=311kHz	
			1.73		mA		R=300kOhm	F=103Hz	
		I _{DD}		6.18		mA	C=20P	R=900Ohm	F=6.76MHz
				2.91		mA		R=4.7kOhm	F=2.98MHz
				2.31		mA		R=10kOhm	F=1.67MHz
				1.84		mA		R=47kOhm	F=403kHz
				1.77		mA		R=100kOhm	F=202kHz
				1.72		mA		R=300kOhm	F=65.8kHz
				5.72		mA	C=101P	R=900Ohm	F=4.17MHz
				2.60		mA		R=4.7kOhm	F=1.33MHz
				2.13		mA		R=10kOhm	F=676kHz
				1.79		mA		R=47kOhm	F=154kHz
				1.75		mA		R=100kOhm	F=75.8kHz
				1.71		mA		R=300kOhm	F=24.5kHz
			5.32		mA	C=301P	R=900Ohm	F=2.34MHz	
			2.45		mA		R=4.7kOhm	F=617kHz	
			2.06		mA		R=10kOhm	F=313kHz	
			1.78		mA		R=47kOhm	F=64.9kHz	
			1.74		mA		R=100kOhm	F=32.5kHz	
		1.71		mA	R=300kOhm		F=10.4kHz		

** Operating at V_{dd}=2.1V is for reference only.

* All specs and applications shown above subject to change without prior notice.

6.2 ELECTRICAL CHARACTERISTICS of CTM8B55E/57E

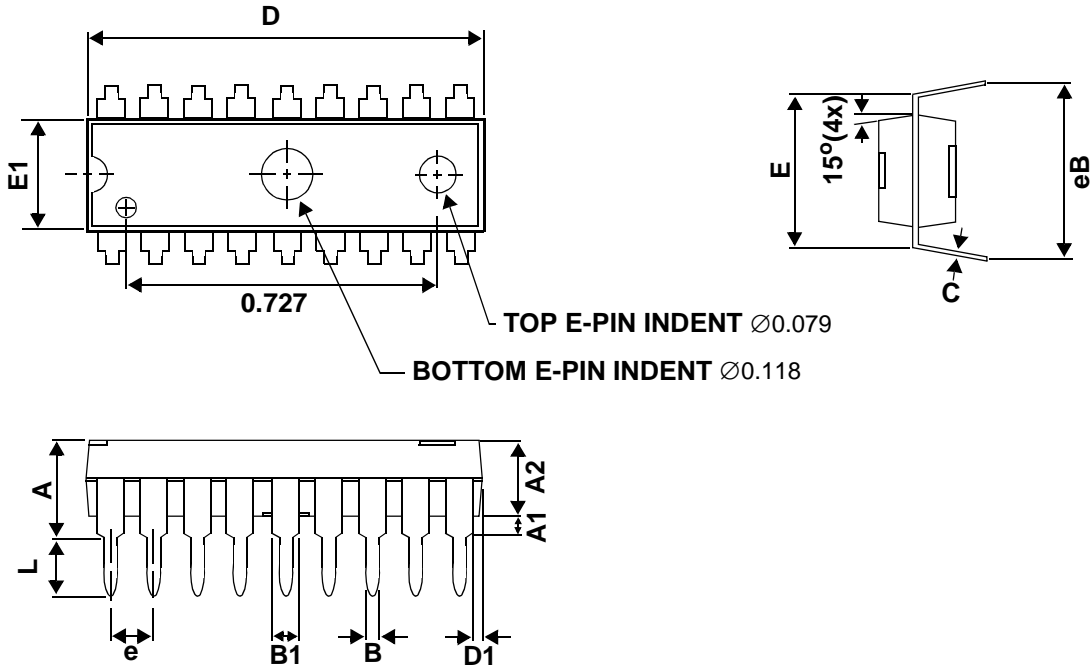
Parameter	Sym	Min.	Typ.	Max.	Units	Conditions	
Input High Voltage	V_{IH}		2.2		V	I/O ports, $V_{dd}=5V$	
			4.2		V	MCLR, $V_{dd}=5V$	
Input Low Voltage	V_{IL}		1.1		V	I/O ports, $V_{dd}=5V$	
			1.0		V	MCLR, $V_{dd}=5V$	
Output Voltage	V_{OH}	3.8			V	I/O Ports, $V_{dd}=4.5V$, $I_{oh}=-5.4mA$, $I_{ol}=8.7mA$ in RC mode	
	V_{OL}			0.6	V		
Sleep Current	I_{PD}		3.0		μA	WDT Enable, $V_{dd}=3.0V$	
	I_{PD}		<1		μA	WDT Disable, $V_{dd}=3.0V$	
Operating Current	I_{DD}					HFX TAL: 24MHz, WDT Disable	
			8.87		mA	$V_{dd}=6.4V$	
			5.84		mA	$V_{dd}=5.0V$	
			4.09		mA	$V_{dd}=4.0V$	
			1.88		mA	$V_{dd}=3.0V$	
	I_{DD}						LFXTAL: 32kHz, WDT Disable
			2.83		mA	$V_{dd}=6.4V$	
			1.96		mA	$V_{dd}=5.0V$	
			1.42		mA	$V_{dd}=4.0V$	
			675		μA	$V_{dd}=3.0V$	
			279		μA	$V_{dd}=2.4V$	
			116		μA	$V_{dd}=2.1V^{**}$	
	I_{DD}						XTAL: 12MHz, WDT Disable
			6.70		mA	$V_{dd}=6.4V$	
			4.39		mA	$V_{dd}=5.0V$	
			3.12		mA	$V_{dd}=4.0V$	
			1.76		mA	$V_{dd}=3.0V$	
			908		μA	$V_{dd}=2.4V$	
					mA	XTAL: 4MHz, WDT Disable	
			3.11		mA	$V_{dd}=6.4V$	
			2.22		mA	$V_{dd}=5.0V$	
			1.17		mA	$V_{dd}=4.0V$	
			578		μA	$V_{dd}=3.0V$	
			377		μA	$V_{dd}=2.1V^{**}$	

* All specs and applications shown above subject to change without prior notice.

Parameter	Sym	Min.	Typ.	Typ.	Units	Conditions		
Operating Current	I _{DD}					V _{dd} =5V, RC mode, WDT Disable, These values include current through Rext		
			6.58		mA	C=3P	R=900Ohm	F=9.12MHz
			3.18		mA		R=4.7kOhm	F=3.85MHz
			2.55		mA		R=10kOhm	F=2.10MHz
			2.05		mA		R=47kOhm	F=500kHz
			1.98		mA		R=100kOhm	F=250kHz
			1.93		mA		R=300kOhm	F=82.8Hz
			6.40		mA	C=20P	R=900Ohm	F=7.72MHz
			3.03		mA		R=4.7kOhm	F=2.86MHz
			2.46		mA		R=10kOhm	F=1.52MHz
			2.04		mA		R=47kOhm	F=352kHz
			1.97		mA		R=100kOhm	F=176kHz
			1.93		mA		R=300kOhm	F=56.8kHz
			5.90		mA	C=101P	R=900Ohm	F=4.61MHz
			2.79		mA		R=4.7kOhm	F=1.33MHz
			2.34		mA		R=10kOhm	F=676kHz
			2.02		mA		R=47kOhm	F=147kHz
			1.97		mA		R=100kOhm	F=73.1kHz
			1.93		mA		R=300kOhm	F=23.6kHz
			5.48		mA	C=301P	R=900Ohm	F=2.46MHz
			2.60		mA		R=4.7kOhm	F=638kHz
			2.28		mA		R=10kOhm	F=311kHz
			2.02		mA		R=47kOhm	F=66.8kHz
			1.98		mA		R=100kOhm	F=32.7kHz
	1.93		mA	R=300kOhm	F=10.5kHz			

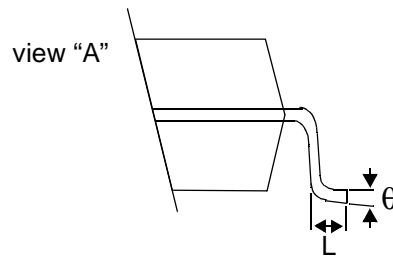
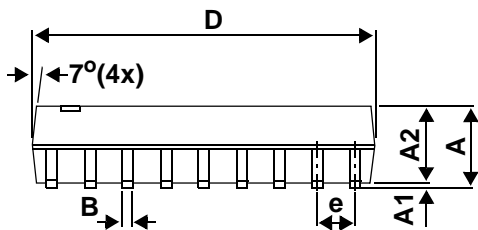
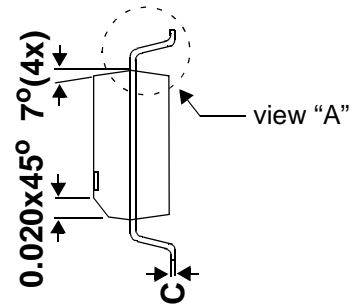
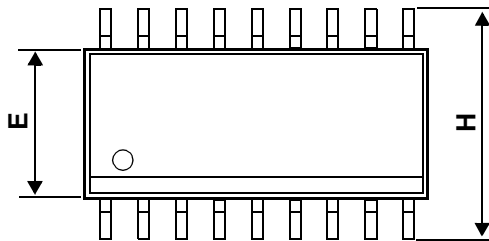
** Operating at V_{dd}=2.1V is for reference only.

* All specs and applications shown above subject to change without prior notice.

7.0 PACKAGE DIMENSION
7.1 18 Pin PDIP 300mil for CTM8B54EN and CTM8B56EN


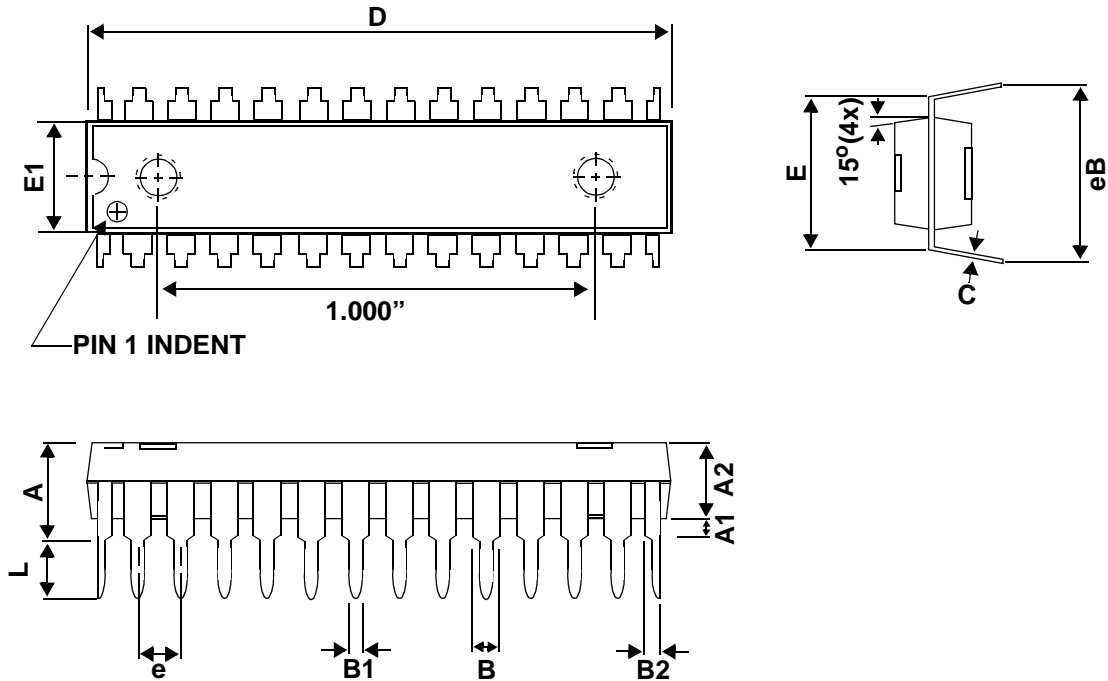
Symbols	Dimension In Millemeters			Dimension In Inches		
	Min	Nom	Max	Min	Nom	Max
A	-	-	4.57	-	-	0.180
A1	0.13	-	-	0.005	-	-
A2	-	3.30	3.56	-	0.130	0.140
B	0.36	0.46	0.56	0.014	0.018	0.022
B1	1.27	1.52	1.78	0.050	0.060	0.070
C	0.20	0.25	0.33	0.008	0.010	0.013
D	22.71	22.96	23.11	0.894	0.904	0.910
D1	0.43	0.56	0.69	0.017	0.022	0.027
E	7.62	-	8.26	0.300	-	0.325
E1	6.40	6.50	6.65	0.252	0.256	0.262
e	-	2.54	-	-	0.100	-
L	3.18	-	-	0.125	-	-
eB	8.38	-	9.65	0.330	-	0.380

* All specs and applications shown above subject to change without prior notice.

7.2 18 Pin SOP for CTM8B54EP and CTM8B56EP


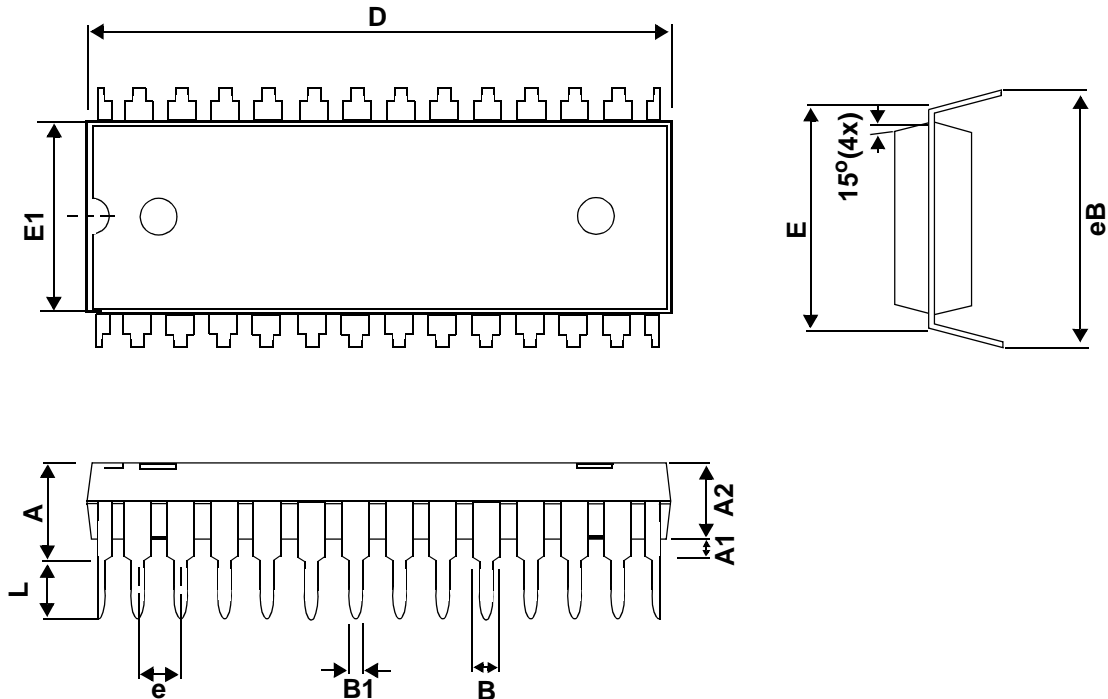
Symbols	Dimension In Millimeters			Dimension In Inches		
	Min	Nom	Max	Min	Nom	Max
A	2.36	2.49	2.64	0.093	0.098	0.104
A1	0.10	-	0.30	0.04	-	0.012
A2	-	2.31	-	-	0.091	-
B	0.33	0.41	0.51	0.013	0.016	0.020
C	0.18	0.23	0.28	0.007	0.009	0.011
D	11.35	-	11.76	0.447	-	0.463
E	7.39	7.49	7.59	0.291	0.295	0.299
e	-	1.27	-	-	0.050	-
H	10.01	10.31	10.64	0.394	0.406	0.419
L	0.38	0.81	1.27	0.015	0.032	0.050
θ	0°	-	8°	0°	-	8°

* All specs and applications shown above subject to change without prior notice.

7.3 28 Pin PDIP 300mil for CTM8B55EM and CTM8B57EM


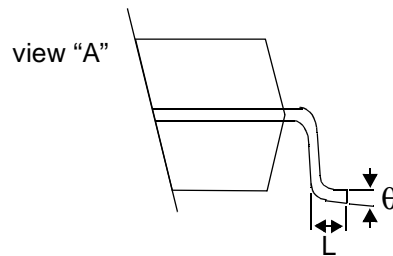
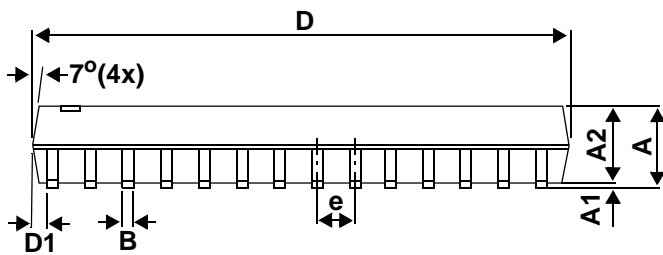
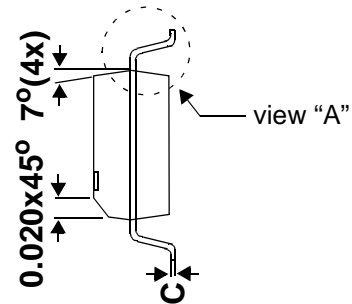
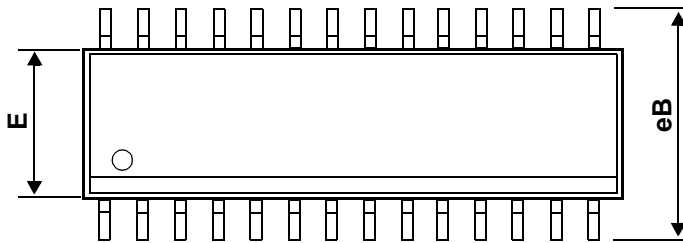
Symbols	Dimension In Millimeters			Dimension In Inches		
	Min	Nom	Max	Min	Nom	Max
A	-	-	4.57	-	-	0.180
A1	0.38	-	-	0.015	-	-
A2	-	3.30	3.56	-	0.130	0.140
B	1.02	-	1.65	0.0040	-	0.065
B1	0.41	-	0.58	0.016	-	0.023
B2	0.71	-	1.12	0.028	-	0.044
C	0.20	0.25	0.33	0.008	0.010	0.013
D	35.13	35.18	35.43	1.383	1.385	1.395
E	7.87	8.31	8.38	0.310	0.327	0.330
E1	7.26	7.32	7.52	0.284	0.288	0.296
e	-	2.54	-	-	0.100	-
L	3.18	-	-	0.125	-	-
eB	8.64	-	9.65	0.340	-	0.380

* All specs and applications shown above subject to change without prior notice.

7.4 28 Pin PDIP 600mil for CTM8B55EN and CTM8B57EN


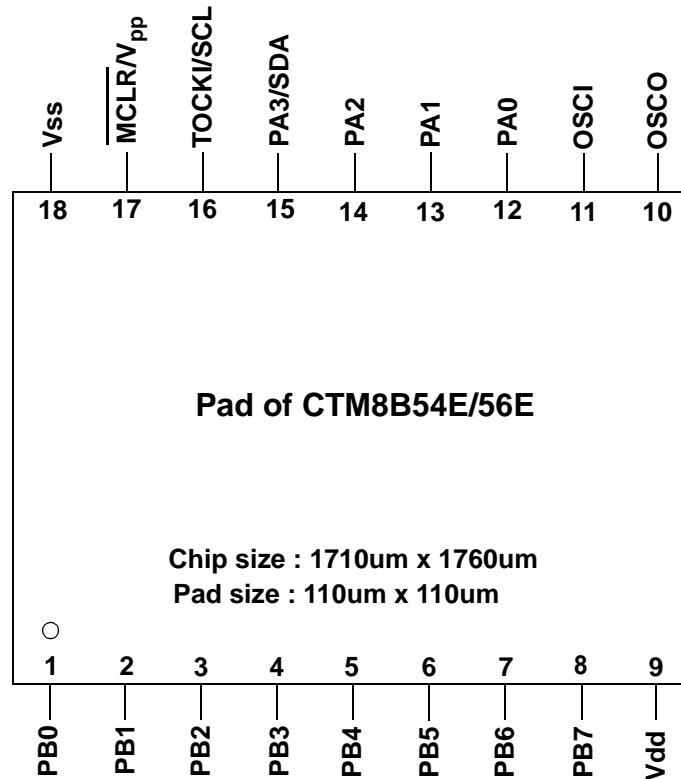
Symbols	Dimension In Millimeters			Dimension In Inches		
	Min	Nom	Max	Min	Nom	Max
A	-	-	5.59	-	-	0.220
A1	0.38	-	-	0.015	-	-
A2	3.81	3.94	4.06	0.150	0.155	0.160
B	-	1.52	-	-	0.06	-
B1	-	0.46	-	-	0.018	-
D	36.96	37.08	37.34	1.455	1.460	1.470
E	-	15.24	-	-	0.600	-
E1	13.72	13.84	13.97	0.540	0.545	0.550
e	-	2.54	-	-	0.100	-
L	3.18	-	-	0.125	-	-
eB	16.00	16.51	17.02	0.630	0.650	0.670

* All specs and applications shown above subject to change without prior notice.

7.5 28 Pin SOP for CTM8B55EP and CTM8B57EP


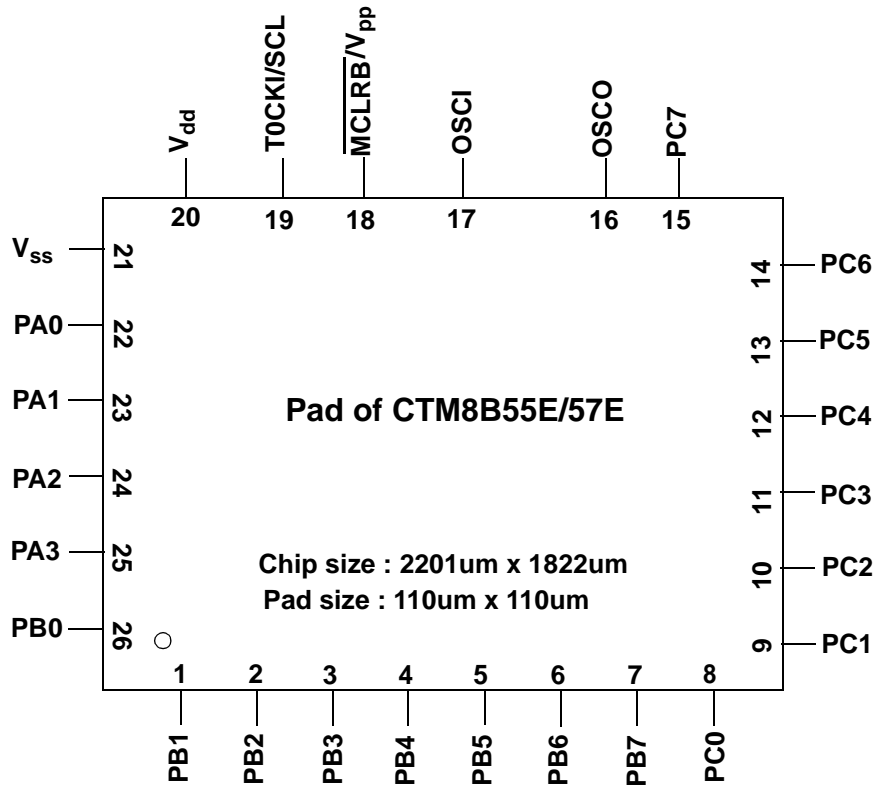
Symbols	Dimension In Millimeters			Dimension In Inches		
	Min	Nom	Max	Min	Nom	Max
A	-	2.488	2.743	-	0.098	0.108
A1	0.152	-	-	0.006	-	-
A2	2.21	2.336	2.464	0.087	0.091	0.097
B	0.305	0.406	0.508	0.012	0.016	0.020
C	0.204	0.254	0.304	0.008	0.010	0.012
D	17.78	17.91	18.42	0.700	0.705	0.725
E	7.366	7.493	7.62	0.290	0.295	0.300
e	1.219	1.270	1.321	0.048	0.050	0.052
eB	10.26	10.42	10.57	0.404	0.410	0.416
L	0.635	-	-	0.025	-	-
θ	0°	4°	8°	0°	4°	8°
D1	0.356	0.508	-	0.014	0.020	-

* All specs and applications shown above subject to change without prior notice.

8.0 PAD ASSIGNMENT
8.1 Pad Assignment for CTM8B54E and CTM8B56E


Pad No.	Pad	X	Y	Pad No.	Pad	X	Y
1	PB0	145.45	153.05	10	OSCO	1598.95	1606.95
2	PB1	320.95	153.05	11	OSCI	1264.95	1606.95
3	PB2	496.45	153.05	12	PA0	1098.45	1606.95
4	PB3	671.95	153.05	13	PA1	922.95	1606.95
5	PB4	847.45	153.05	14	PA2	747.45	1606.95
6	PB5	1022.95	153.05	15	PA3/SDA	571.95	1606.95
7	PB6	1198.45	153.05	16	TOCKI/SCL	424.90	1606.95
8	PB7	1373.95	153.05	17	MCLR/V _{pp}	249.20	1606.95
9	V _{dd}	1557.45	153.05	18	V _{ss}	124.20	1606.95

* All specs and applications shown above subject to change without prior notice.

8.2 Pad Assignment for CTM8B55E and CTM8B57E


Pad No.	Pad	X	Y	Pad No.	Pad	X	Y
1	PB1	217.01	93.20	14	PC6	2117.01	1627.80
2	PB2	476.09	93.20	15	PC7	1830.89	1738.75
3	PB3	720.67	93.20	16	OSCO	1595.29	1733.20
4	PB4	979.75	93.20	17	OSCI	1210.68	1733.20
5	PB5	1224.33	93.20	18	MCLR/V _{pp}	863.95	1738.79
6	PB6	1483.41	93.20	19	TOCKI/SCL	603.04	1738.75
7	PB7	1727.99	93.20	20	V _{dd}	344.41	1738.75
8	PC0	1987.07	93.20	21	V _{ss}	101.98	1644.97
9	PC1	2117.01	361.40	22	PA0	93.21	1372.18
10	PC2	2117.01	620.48	23	PA1	93.21	1127.60
11	PC3	2117.01	865.06	24	PA2	93.21	868.52
12	PC4	2117.01	1124.14	25	PA3/SDA	93.21	623.94
13	PC5	2117.01	1386.72	26	PB0	93.21	364.86

* All specs and applications shown above subject to change without prior notice.

9.0 Order Information

Type	300mil PDIP	600mil PDIP	300mil SOP	Die Form
18pins	CTM8B54EN	-	CTM8B54EP	CTM8B54E
28pins	CTM8B55EM	CTM8B55EN	CTM8B55EP	CTM8B55E
18pins	CTM8B56EN	-	CTM8B56EP	CTM8B56E
28pins	CTM8B57EM	CTM8B57EN	CTM8B57EP	CTM8B57E

* All specs and applications shown above subject to change without prior notice.