SONY

CXA2161R

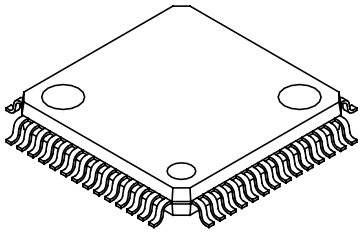
I²C Bus Compatible Audio Video (AV) Switch & Electronic Volume Control

Description

The Sony CXA2161R is an Audio/Video switch designed primarily for application in Digital Set Top Boxes. It provides video and audio routing from the digital encoder source to the TV and VCR scart (peri-television) connectors. In addition, the TV audio output has a programmable volume control. The chip is programmed by means of an I²C interface and can operate from a single or dual power supply.

Target specifications: Canal+, BSkyB, TPS, NorDig, and ECCA Euro-Box

56 pin LQFP (Plastic)



Features

Supply

- Single: 0V, +5V, +12V
- Dual: 0V, –5V, +5V and +12V
  (Low number of external parts required)

Video

- 2 scart switching (VCR, TV)
- VCR input supports RGB mode
- Integrated 75Ω drivers for direct video connection
- Y/C mixer with trap for RF modulators
- Switchable clamps on inputs
- Adjustable gain on RGB outputs
- Video output shutdown for low power modes
- Fast blanking switch
- Slow blanking switch for TV and VCR output
- SVHS switch on VCR output
- Y/C auxiliary input

Audio

- Four stereo audio inputs
- Volume control (–56dB to +6dB in 2dB steps)
- Additional switchable gain on audio DAC inputs
- Audio overlay facility
- Volume bypass for TV and Phono outputs
- Mono switching on TV, VCR outputs
- High drive capability (600Ω loads possible)
- Switchable audio limiter function
- Switchable Mono output for RF modulators
- Audio output disable

I²C and Logic

- Fast mode compatible I²C bus
- Function monitor with loop through
- Interrupt output for function monitor
- Logic output pin
- Sync detector for Y/CVBS inputs

Applications

- Digital Set Top Box
- Integrated digital television

Structure

Bipolar silicon monolithic IC

Absolute Maximum Ratings (Ta = 25°C) unless stated

• Supply voltage	V_{CC}	14	V
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	1.1	W
(when mounted on the board)			

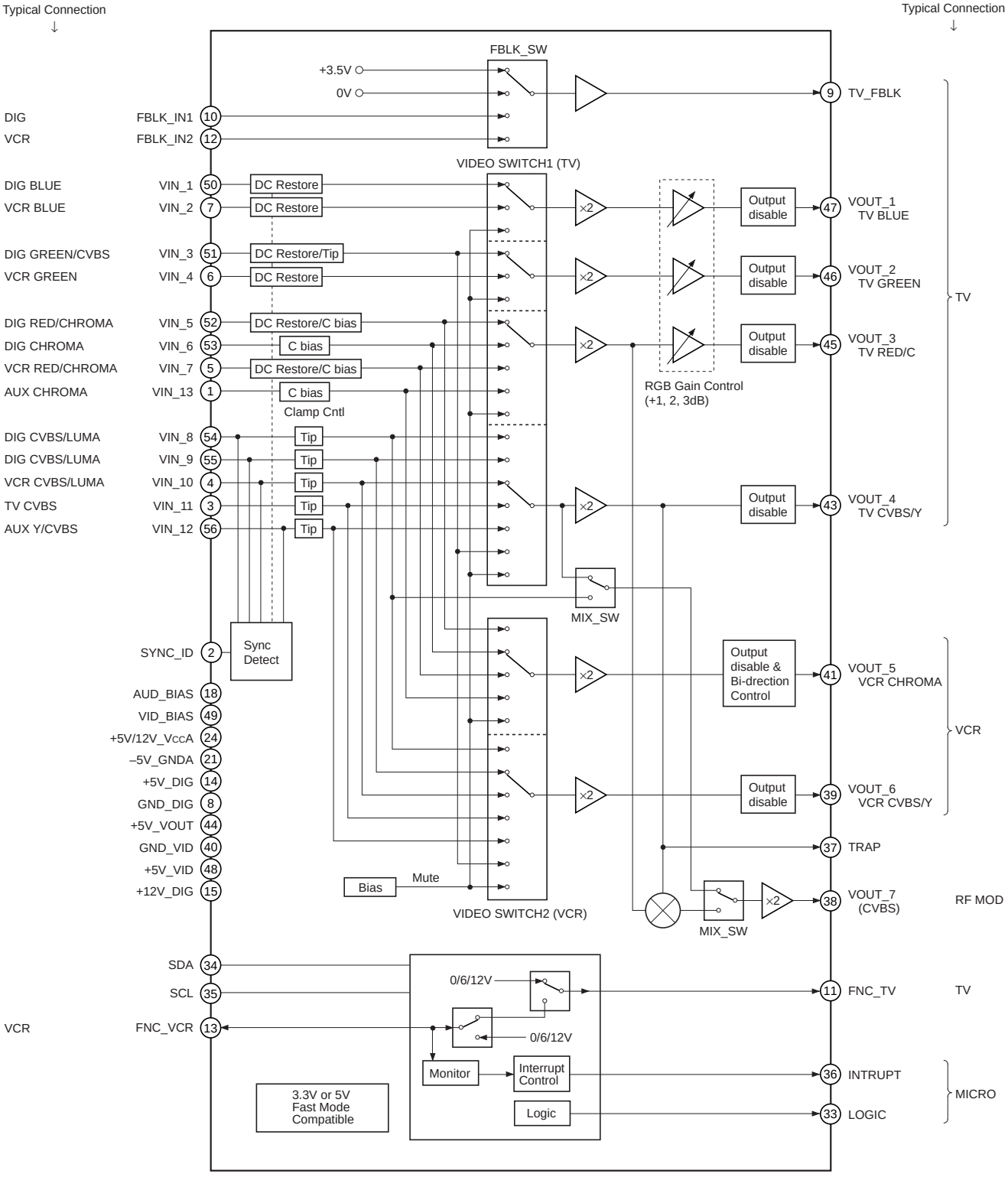
Operating Conditions

• Single supply		12 ± 0.6	V
		5 ± 0.25	V
• Dual supply		–5 ± 0.25	V
		5 ± 0.25	V
		12 ± 0.6	V
• Operating temperature	Topr	–20 to +75	°C

E00202-PS

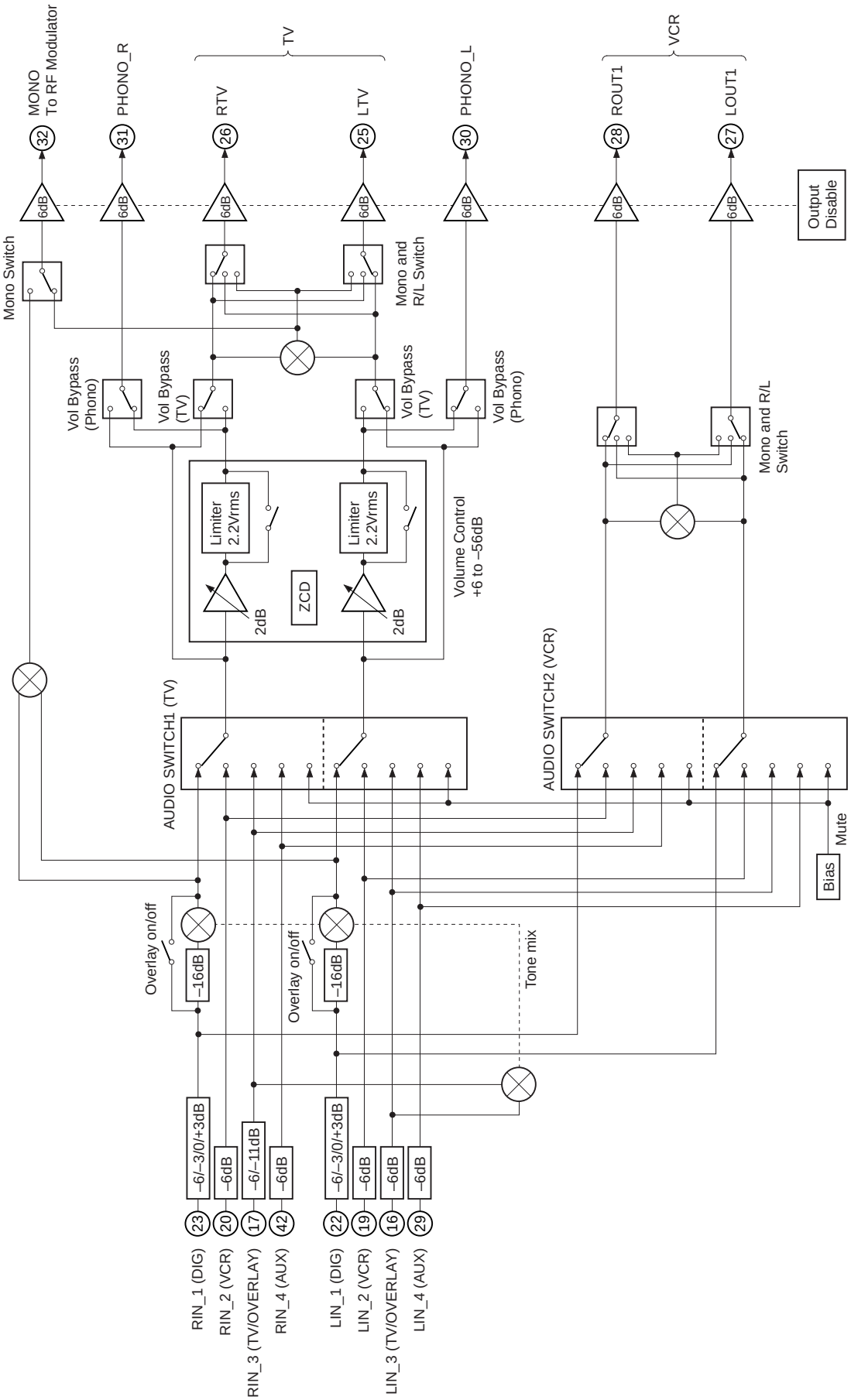
Block Diagram

(1) Video and Digital Section

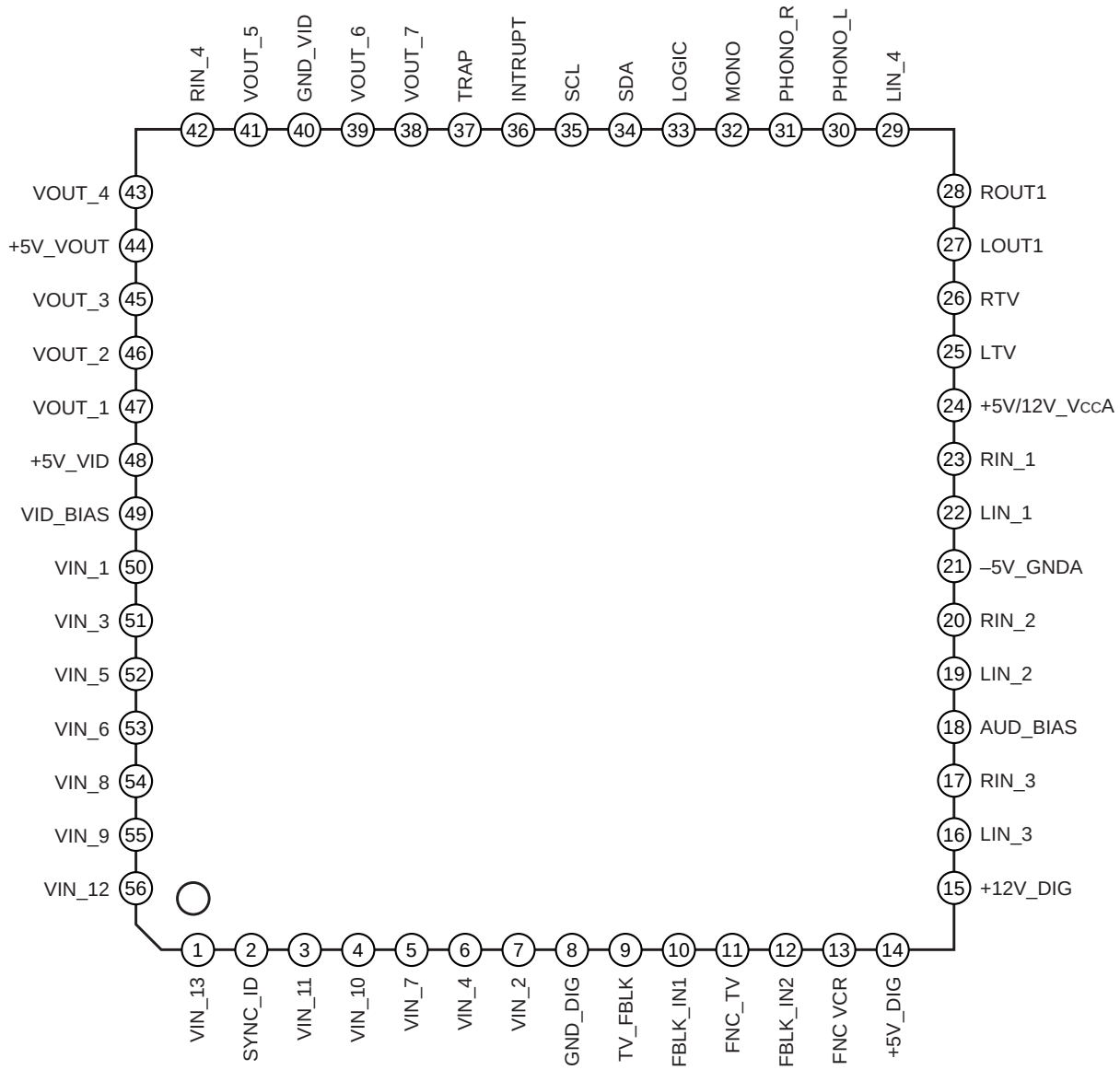


Note) All video outputs contain 75Ω drivers, except VOUT_7 (Pin 38).

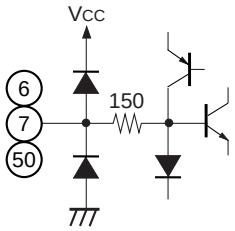
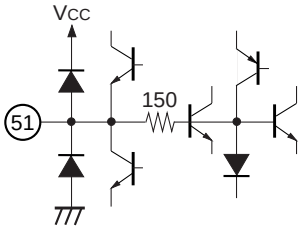
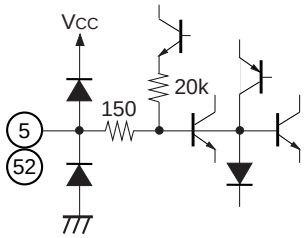
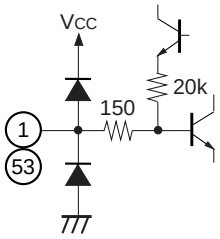
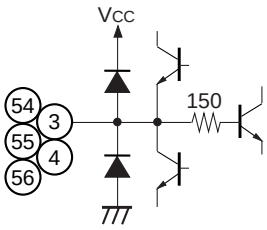
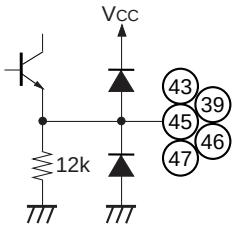
(2) Audio section

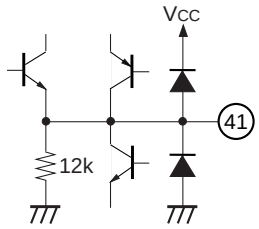
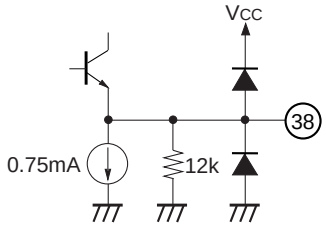
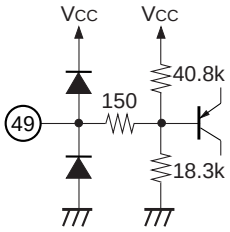
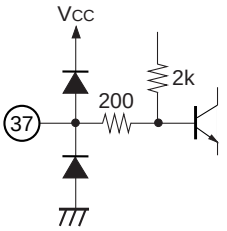
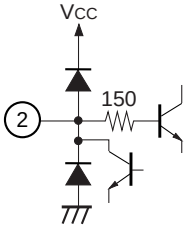
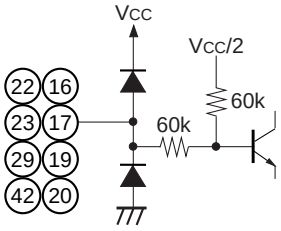


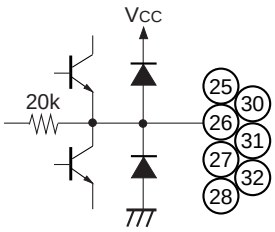
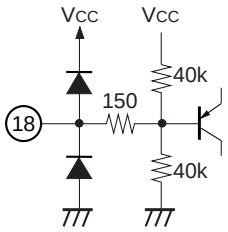
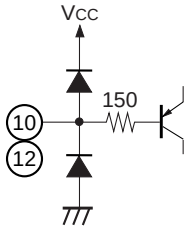
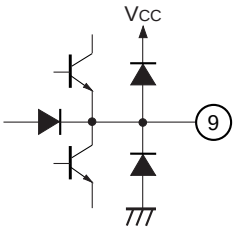
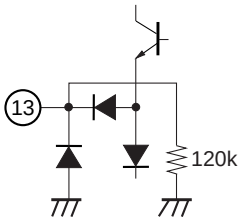
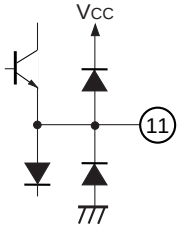
Pin Configuration

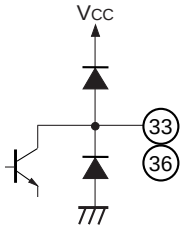
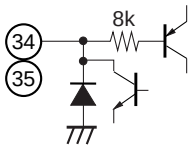


Pin Description

Pin No.	Symbol	Pin voltage [V]	Equivalent circuit	Description
50 7 6	VIN_1 VIN_2 VIN_4	2.4		RGB signal inputs
51	VIN_3	2.4 2.35		RGB signal input or CVBS/Luminance signal input
52 5	VIN_5 VIN_7	2.4 3.0		RGB signal inputs or Chrominance signal inputs
53 1	VIN_6 VIN_13	3.0		Chrominance signal inputs
54 55 4 3 56	VIN_8 VIN_9 VIN_10 VIN_11 VIN_12	2.35		CVBS/Luminance signal inputs
47 46 45 43 39	VOUT_1 VOUT_2 VOUT_3 VOUT_4 VOUT_6	—		RGB/CVBS signal outputs (See description of operation for pin voltages)

Pin No.	Symbol	Pin voltage [V]	Equivalent circuit	Description
41	VOUT_5	1.8		Chrominance signal output
38	VOUT_7	0.4		Typically RF modulator signal output Minimum load resistance = 20kΩ
49	VID_BIAS	0.9		Internal reference bias for video circuits. A capacitor is connected from this pin to GND. Typically 100nF
37	TRAP	2.3		Connects trap circuit for subcarrier
2	SYNC_ID	2.5		Sync detect circuit time constant, resistor and capacitor connection pin
22 23 19 20 16 17 29 42	LIN_1 RIN_1 LIN_2 RIN_2 LIN_3 RIN_3 LIN_4 RIN_4	6.0 (Single) 0.0 (Dual)		Audio signal inputs

Pin No.	Symbol	Pin voltage [V]	Equivalent circuit	Description	
25 26 27 28 30 31 32	LTV RTV LOUT1 ROUT1 PHONO_L PHONO_R MONO	6.0 (Single) 0.0 (Dual)		Audio signal outputs	
18	AUD_BIAS	6.0 (Single) 0.0 (Dual)		Internal reference bias for audio circuits.	Capacitor connected to GND. (Typically 22µF) Connected directly to GND.
10 12	FBLK_IN1 FBLK_IN2	—		Fast blanking signal inputs	
9	TV_FBLK	—		Fast blanking signal output	
13	FNC_VCR	—		SCART function pin 8 input/output to VCR	
11	FNC_TV	—		SCART function pin 8 output to TV	

Pin No.	Symbol	Pin voltage [V]	Equivalent circuit	Description
33 36	LOGIC INTRUPT	—		Open collector logic outputs Typically connect to +5V through 10kΩ resistor.
35	SCL	—		I^2C bus clock line
34	SDA	—		I^2C bus data line
14	+5V_DIG	5.0		Digital supply
44	+5V_VOUT			Video output supply
48	+5V_VID			Video supply
15	+12V_DIG	12.0		Digital supply
21	–5V_GNDA	–5.0 (Dual) 0.0 (Single)		Audio supply or Audio ground
24	+5V/+12V_VccA	5.0 (Dual) 12.0 (Single)		Audio supply
8	GND_DIG	0.0		Digital ground
40	GND_VID	0.0		Video ground

Electrical Characteristics

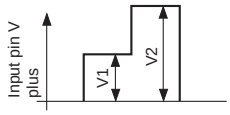
Nominal conditions (Ta = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption (Single ended supply)	I_{CC1}	+12 supply, no signal, no load	—	22	45	mA
	I_{CC2}	+5 supply, no signal, no load	—	50	80	mA
Current consumption (Dual supply)	I_{CC3}	+12 supply, no signal, no load	—	2	6	mA
	I_{CC4}	+5 supply, no signal, no load	—	70	115	mA
	I_{CC5}	–5 supply, no signal, no load	—	20	45	mA

Video System

Nominal conditions single supply (Ta = 25°C, +5V/12V_V_{CC}A = +12V, –5V_GNDA = 0V, +5V_VID = +5V, +5V_VOUT = +5V, +5V_DIG = +5V, GND_VID = 0V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Sync tip clamp voltage at input	Vclmp1	Vin3, Vin8, Vin9, Vin10, Vin11, Vin12 inputs. (Vin3 set to CVBS mode) (Fig. 1)	—	2.4	—	V
Chrominance bias input voltage	Cbias1	Vin5, Vin7 inputs. Clamps set to Chrominance bias mode. (Fig. 1)	—	3	—	V
	Cbias2	Vin6, Vin13 inputs. (Fig. 1)	—	2.35	—	V
RGB dc restore input voltage	RGB1	Vin1, Vin2, Vin3, Vin4, Vin5, Vin7 inputs. (Vin3 & Vin5 set to RGB mode) (Fig. 1)	—	2.4	—	V
Sync tip clamp voltage at output	Vclmp2	Vout4, Vout6 outputs (Fig. 1)	—	0.3	—	V
Chrominance bias output voltage	Cbias3	Vout3, Vout5 outputs (Fig. 1)	—	1.8	—	V
RGB dc restore output voltage	RGB2	Vout1, Vout2, Vout3 outputs (Fig. 1)	—	0.6	—	V
Gain (Vout1 to 6)	GVv	f = 200kHz, 0.3Vp-p input , RGB Gain = 0dB (Fig. 2)	5.5	6.0	6.5	dB
Gain (Vout1, 2, 3)	GV_{RGB1}	f = 200kHz, 0.3Vp-p input , RGB Gain = +1dB (Fig. 2)	6.5	7.0	7.5	dB
	GV_{RGB2}	f = 200kHz, 0.3Vp-p input , RGB Gain = +2dB (Fig. 2)	7.5	8.0	8.5	dB
	GV_{RGB3}	f = 200kHz, 0.3Vp-p input , RGB Gain = +3dB (Fig. 2)	8.5	9.0	9.5	dB
Gain (Vout7) Mixer off	GV_{YC}	f = 200kHz, 0.3Vp-p input (Fig. 2)	5.5	6.0	6.5	dB
Gain (Vout7) Mixer on	GV_{YC}	f = 200kHz, 0.3Vp-p input (Fig. 2)	5.5	5.75	6.5	dB
Bandwidth (Vout1 to 6)	f_{V3dB}	0.3Vp-p input, frequency where output level is –3dB with 200kHz serving as 0dB (Fig. 2)	15	22	—	MHz
Bandwidth (Vout7) Mixer on – No trap components	f_{V3dB}	0.3Vp-p input, frequency where output level is –3dB with 200kHz serving as 0dB (Fig. 2)	8	18	—	MHz
Input dynamic range	V_{DRVI}	200kHz input applied to any video (Fig. 2)	1.4	—	—	Vp-p
Output dynamic range	V_{DRVO}	200kHz input applied to any video (Fig. 2)	2.8	—	—	Vp-p

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Cross talk	Vctv	f = 4.43MHz, 1Vp-p input (Fig. 2)	—	—	–50	dB
S/N ratio	S/N_V	Ratio of 0.7Vp-p white video signal to black line noise. Weighted using CCIR 567. HPF@5kHz, LPF@5MHz. (Fig. 2)	—	74	—	dB
Non-linearity	Lin	 V1 = Pin voltage + 0.5V, V2 = Pin voltage + 1V At output, non-linearity = $\left(\frac{V2}{V1 \times 2} - 1\right) \times 100$ (Fig. 2)	–3	0	3	%
Differential gain	DG	1.7Vp-p 5-step modulated staircase. (Chrominance & Burst are 150mVp-p, 4.43MHz) (Fig. 2)	–3	0	3	%
Differential phase	DP	As above.	–3	0	3	deg

Audio System

Unless otherwise stated: input coupling capacitor 1µF; output coupling capacitor 10µF; load 10kΩ.

Nominal conditions single supply (Ta = 25°C, +5V/12V_V_{CC}A = +12V, –5V_GNDA = 0V, +5V_VID = +5V, +5V_VOUT = +5V, +5V_DIG = +5V, GND_VID = 0V)

Nominal conditions dual supply (Ta = 25°C, +5V/12V_V_{CC}A = +5V, –5V_GNDA = –5V, +5V_VID = +5V, +5V_VOUT = +5V, +5V_DIG = +5V, GND_VID = 0V)

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Input/output pin voltage (Single supply)		V_{APIN1}	No signal, no load (Fig. 3)	—	6	—	V
Input/output pin voltage (Dual supply)		V_{APIN2}	No signal, no load (Fig. 3)	—	0	—	V
Output pin voltage when disabled (Dual supply)		V_{APIN3}	No signal, no load (Fig. 3)	—	0	—	V
Gain							
Input	Output						
Rin1 or Lin1	TV or Phono	GV_{A1}	f = 1kHz, 0.5Vrms input. TV volume set to 0dB, RIN_1/LIN_1 amplifier = –6dB (Fig. 4)	–0.5	0	0.5	dB
Rin1 or Lin1	TV or Phono	GV_{A2}	f = 1kHz, 0.5Vrms input. TV volume set to 0dB, RIN_1/LIN_1 amplifier = –3dB (Fig. 4)	2.5	3	3.5	dB
Rin1 or Lin1	TV or Phono	GV_{A3}	f = 1kHz, 0.5Vrms input. TV volume set to 0dB, RIN_1/LIN_1 amplifier = 0dB (Fig. 4)	5.5	6	6.5	dB
Rin1 or Lin1	TV or Phono	GV_{A4}	f = 1kHz, 0.5Vrms input. TV volume set to 0dB, RIN_1/LIN_1 amplifier = +3dB (Fig. 4)	8.5	9	9.5	dB
Rin1 or Lin1	VCR	GV_{A5}	f = 1kHz, 1Vrms input. TV volume set to 0dB, RIN_1/LIN_1 amplifier = –6dB (Fig .4)	–0.5	0	0.5	dB

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Rin1 + Lin1	TV (mono mix)	GV_{A6}	f = 1kHz, 0.5Vrms stereo input. TV volume set to 0dB, RIN_1/LIN_1 amplifier = –6dB. TV mono switch on. (Fig. 4)	–0.5	0	0.5	dB
Rin1 + Lin1	MONO	GV_{A7}	f = 1kHz, 1Vrms stereo input. TV volume set to 0dB, RIN_1/LIN_1 amplifier = –6dB. **(Note 1)** (Fig. 4)	–0.5	0	0.5	dB
Rin2, 3, 4 or Lin2, 3, 4	TV or Phono	GV_{A9}	f = 1kHz, 1Vrms input, TV volume set to 0dB (Fig. 4)	–0.5	0	0.5	dB
Rin1 + Lin1	VCR (mono mix)	GV_{A8}	f = 1kHz, 1Vrms stereo input. RIN_1/LIN_1 amplifier = –6dB. VCR mono switch on. (Fig 4)	–0.5	0	0.5	dB
Rin2 + Lin2 Rin3 + Lin3 Rin4 + Lin4	MONO	GV_{A10}	f = 1kHz, 1Vrms stereo input. TV volume set to 0dB **(Note 2)** (Fig 4)	–0.5	0	0.5	dB
Rin2, 3, 4 Lin2, 3, 4	VCR	GV_{A11}	f = 1kHz, 1Vrms input (Fig 4)	–0.5	0	0.5	dB
Rin2 + Lin2 Rin3 + Lin3 Rin4 + Lin4	VCR (mono mix)	GV_{A12}	f = 1kHz, 1Vrms stereo input. VCR mono switch on. (Fig 4)	–0.5	0	0.5	dB
Rin3	RTV, ROUT1, Phono_R	GV_{A13}	f = 1kHz, 1Vrms input, Lin3 has no signal Audio overlay enabled with –11dB attenuation at input RIN_3 (Fig 4)	–5.5	–5	–4.5	dB
Lin3	LTV, LOUT1, Phono_L	GV_{A14}	f = 1kHz, 1Vrms input Audio overlay enabled. (Fig 4)	–0.5	0	0.5	dB
Audio frequency response		F_{AF}	0.3Vp-p input. Output/input gain at 30kHz with 1kHz serving as 0dB (Fig 4)	–0.3	0	0.3	dB
Frequency bandwidth		F_{BWA1}	0.3Vp-p input; frequency where output level is –3dB with 1kHz serving as 0dB. No load attached (Fig 4)	—	1	—	MHz
Distortion		THD	f = 1kHz, 0.5Vrms, unweighted response; LPF@400Hz, HPF@80kHz (Fig 4)	—	0.005	0.2	%
Input dynamic range Rin1, 2, 3, 4/Lin1, 2, 3, 4		Vd_{A1}	f = 1kHz, RIN_1/LIN_1 input amplifier set to –6dB. Dual supply mode used. (Fig 4)	2.5	2.9	—	Vrms
Cross talk (Channel separation)		Vct_A	f = 1kHz, 1Vrms input on one input, measure on any other audio output (Fig 4)	—	—	–76	dB
DC offset		Voff	Offset voltage between input and output	–30	0	30	mV
Input impedance Rin1, 2, 3, 4/Lin1, 2, 3, 4		Zin1	(excluding any external series resistor)	—	120	—	kΩ
Output impedance		Zout	(excluding any external series resistor)	—	10	—	Ω
Phase difference		Vpda	f = 1kHz, 1Vrms input to two channels. Phase difference of stereo output measured	—	0.05	—	deg
S/N ratio		S/N_A	f = 1kHz, 1Vrms input (at 0dB volume). HPF@20Hz, LPF@20kHz. (Fig 4)	80	93	—	dB

Note 1) Mono switch set to mix of Rin1 & Lin1 inputs.

Note 2) Mono switch set to mix of RTV & LTV after volume control.

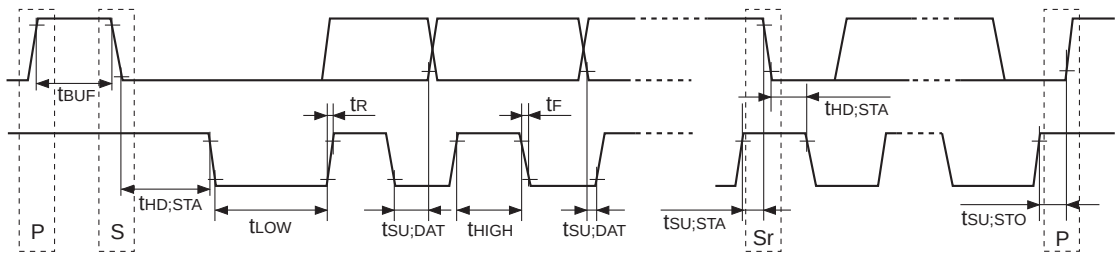
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Electronic Volume Control						
Volume attenuation step	A_{EVC}	f = 1kHz, 0.5Vrms input. Set by I²C (Fig 4)	1.6	2	2.4	dB
Mute TV I/P MUTE or VCR I/P MUTE	Amute	f = 1kHz, 1Vrms input (Fig 4)	—	–90	–76	dB
Audio limiter level	Alimit	f = 1kHz, 2.5Vrms input. Measure TVp-p output with limiter switched on. (Fig 4)	—	6.5	—	Vp-p

Digital Characteristics

I²C Interface

The I²C interface is compliant with Philips I²C Fast Mode specification (date April 1995). The interface is also capable of interfacing to +3.3V or +5V logic levels.

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage	V_{IH}		2.3	—	5.5	V
Low level input voltage	V_{IL}		0	—	1.5	V
Low level output voltage	V_{OL}	With SDA, 3mA current supplied	0	—	0.4	V
		With SDA, 6mA current supplied	0	—	0.6	
Hysteresis of schmitt trigger input	V_{HYST}	$V_{IH} - V_{IL}$	—	0.5	—	V
Spike suppression	t_{SP}		—	—	50	ns
Fall time for SDA line	t_F	400pF bus load	—	—	300	ns
SCL clock frequency	t_{SCL}	I²C Bus line requirement	0	—	400	kHz
Bus free time between a stop and start	t_{BUF}	I²C Bus line requirement	1.3	—	—	µs
Hold time (repeated start condition)	$t_{HD;STA}$	I²C Bus line requirement	0.6	—	—	µs
Low period of SCL clock	t_{LOW}	I²C Bus line requirement	1.3	—	—	µs
High period of SCL clock	t_{HIGH}	I²C Bus line requirement	0.6	—	—	µs
Setup time for a repeated start condition	$t_{SU;SDA}$	I²C Bus line requirement	0.6	—	—	µs
Data hold time	$t_{HD;DAT}$	I²C Bus line requirement	0	—	0.9	µs
Data setup time	$t_{SU;DAT}$	I²C Bus line requirement	100	—	—	ns
Setup time for stop condition	$t_{SU;STO}$	I²C Bus line requirement	0.6	—	—	µs



Logic/Interrupt Output

These outputs are open collector type and normally connected to +5V through a 10kΩ resistor.

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output low voltage	DIG_{VOUTL}	I_{OL} = 1mA	—	0.15	0.4	V

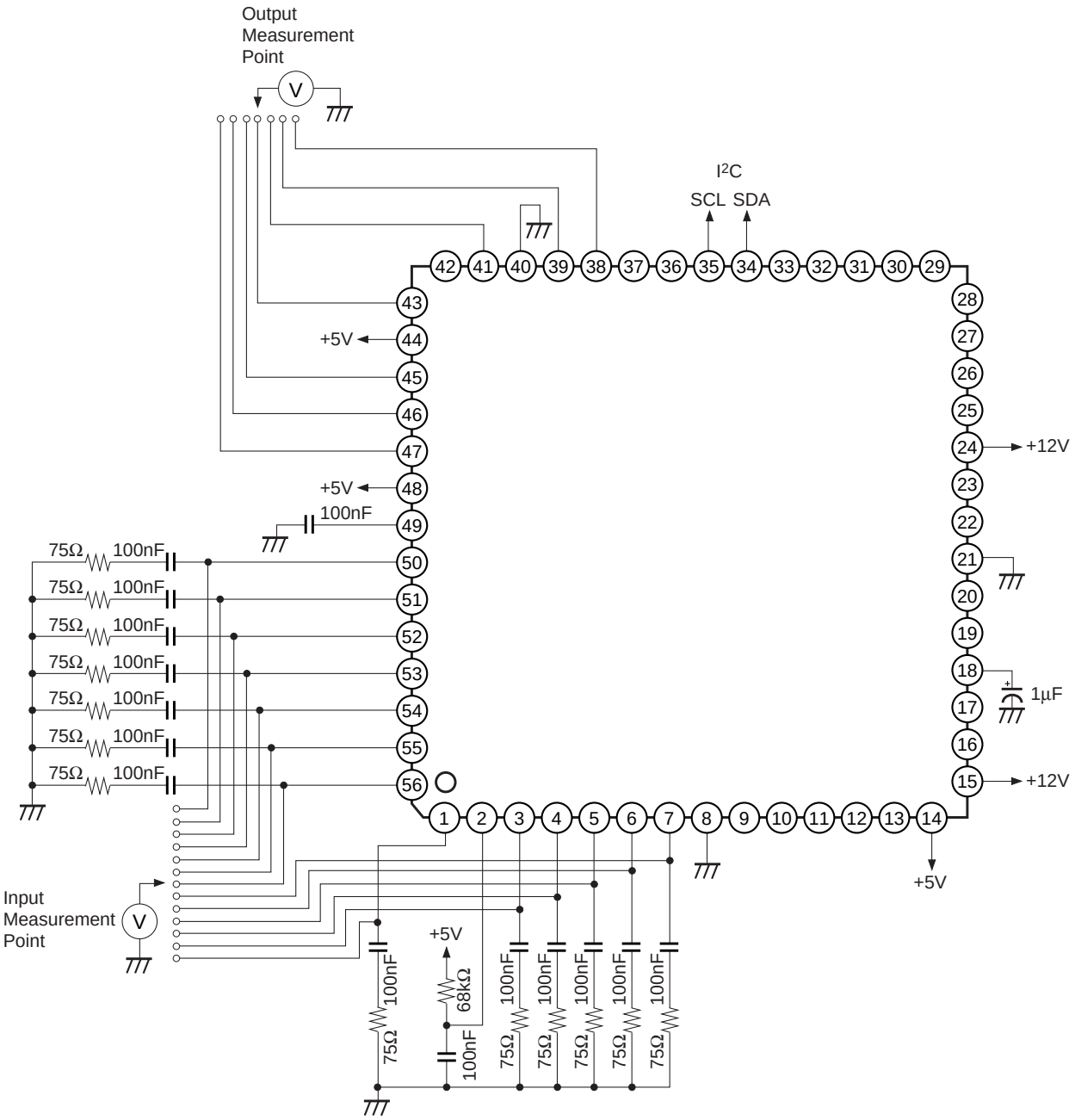


Fig. 1. Video System (DC Test)

DC measured from Pins 1, 3, 4, 5, 6, 7, 38, 39, 41, 43, 45, 46, 47, 50, 51, 52, 53, 54, 55, 56

Notes) 1. All supplies de-coupled close to supply pins 14, 15, 24, 44, 48 with 10nF and 10µF capacitors.
2. All video outputs are unloaded during tests.

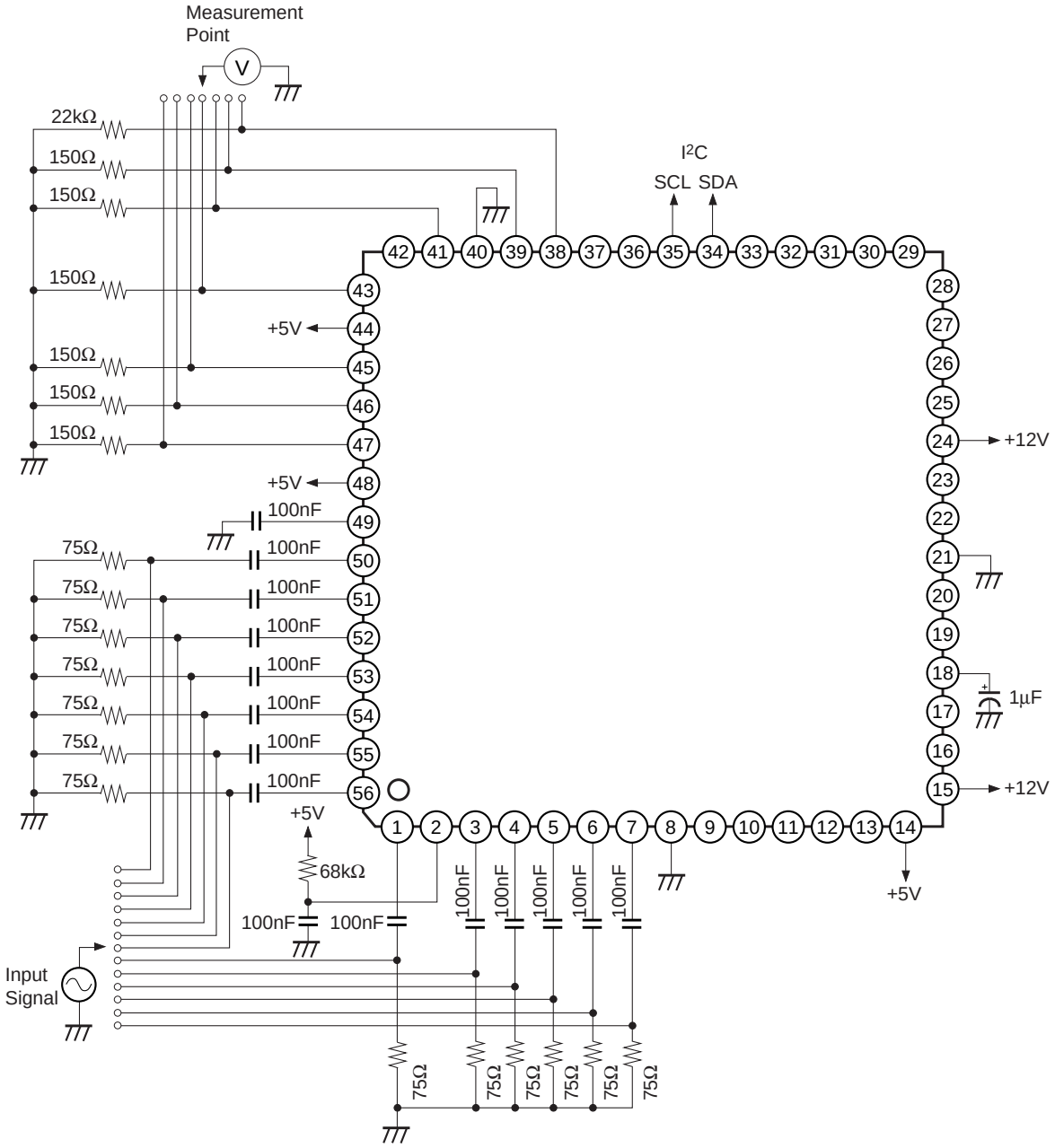


Fig. 2. Video System
(Gain, Dynamic Range, Bandwidth, Differential Gain, Differential Phase, Crosstalk, Linearity, Sync Detection)

Signal applied to Pins 1, 3, 4, 5, 6, 7, 50, 51, 52, 53, 54, 55, 56
Output signal measured from Pins 38, 39, 41, 43, 45, 46, 47

Notes) 1. All supplies de-coupled close to supply pins 14, 15, 24, 44, 48 with 10nF and 10µF capacitors.
2. For tests requiring video measuring equipment with 75Ω input impedance, an external video line driver or buffer is used.
3. For video crosstalk tests all video inputs are terminated with 37.5Ω

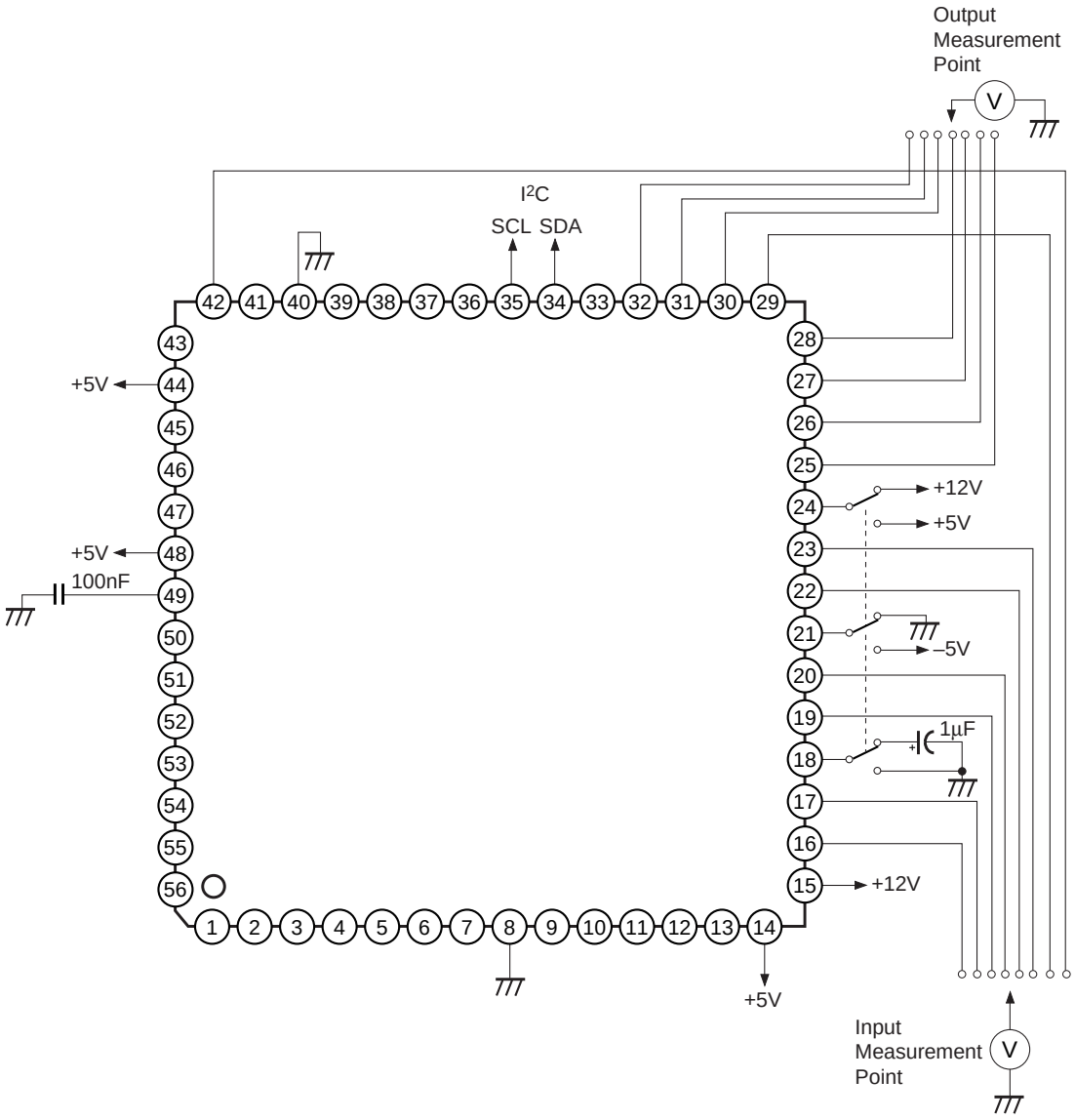


Fig. 3. Audio System (DC Tests)

DC measured from Pins 16, 17, 19, 20, 22, 23, 25, 26, 27, 28, 29, 30, 31, 32, 42

Notes) 1. Single audio supply configuration shown. Operate switches for dual supply configuration.
2. All supplies de-coupled close to supply pins 14, 15, 21, 24, 44, 48 with 10nF and 10µF capacitors.

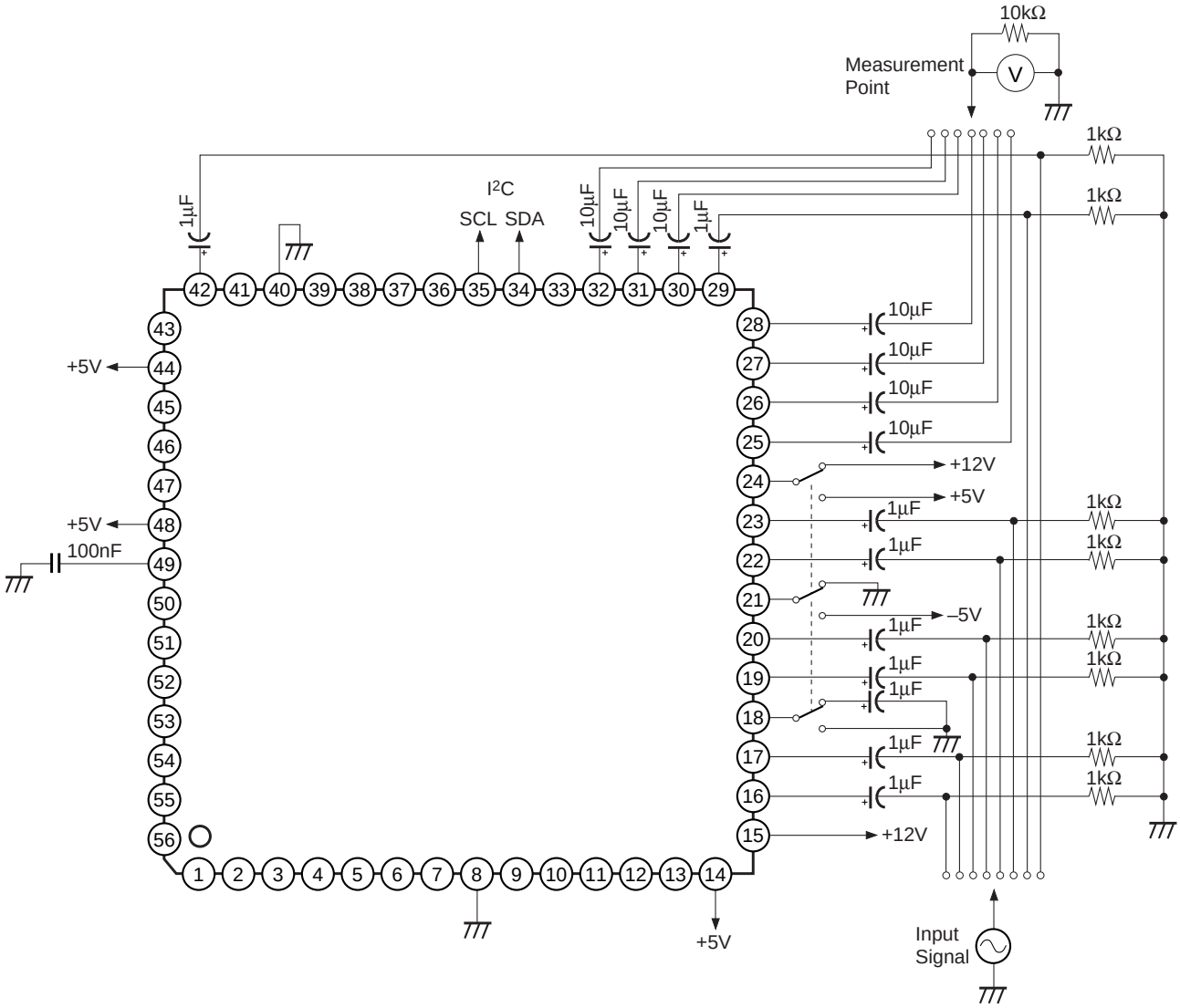


Fig. 4. Audio System

(Single Supply — Gain, Bandwidth, Signal to Noise, Electronic Volume, Zero Cross Detection, Limiter)
(Dual Supply — Distortion, Dynamic Range, Crosstalk)

Signal applied to Pins 16, 17, 19, 20, 22, 23, 29, 42
Output signal measured from Pins 25, 26, 27, 28, 30, 31, 32

Notes) 1. Single audio supply configuration shown. Operate switches for dual supply configuration.
2. All supplies de-coupled close to supply pins 14, 15, 21, 24, 44, 48 with 10nF and 10µF capacitors.

I²C Control Data Format

S	Slave address	A	DATA1	A	DATA2	A	DATA3	A	DATA4	A	DATAn	A	P

S: Start condition A: Acknowledge P: Stop condition

Address = 90H

I²C Data Structure (write mode)

	b7	b6	b5	b4	b3	b2	b1	b0
Address	1	0	0	1	0	0	0	0 = Write
Data1	RIN1/LIN1 GAIN CONTROL		VOLUME CONTROL					TV AUD MUTE
Data2	MONO SWITCH	TV VOL BYPASS	TV MONO SWITCH			TV AUDIO SELECT		PHONO BYPASS
Data3	TV AUD MUTE	OUTPUT LIMIT	VCR MONO SWITCH			VCR AUDIO SELECT		OVERLAY ENABLE
Data4	TV INPUT MUTE	LOGIC LEVEL	FNC LEVEL		FNC FOLLOW	FNC DIR	FAST BLANK	
Data5	VCR VIDEO SWITCH			RGB GAIN		TV VIDEO SWITCH		
Data6	VCR INPUT MUTE	SYNC SEL		VIN5 CLAMP	VIN7 CLAMP	VIN3 CLAMP	MIXER CONTROL	
Data7	ZCD	VOUT5 0V	ENABLE VOUT6	ENABLE VOUT5	ENABLE VOUT4	ENABLE VOUT3	ENABLE VOUT2	ENABLE VOUT1

I²C Data Structure (read mode)

	b7	b6	b5	b4	b3	b2	b1	b0
Address	1	0	0	1	0	0	0	1 = Read
Data	NOT USED	NOT USED	ZERO CROSS STATUS	P.O.D.	NOT USED	SYNC DETECT	FNC_VCR	

Note) ZCD = Zero Cross Detect
P.O.D. = Power on Detect

Video I²C Write Structure

Video Switch 1: TV Output [Data 5 Bits 0, 1, 2]

Switch setting	Blue Vout1	Green Vout2	R/C Vout3	CVBS/Y Vout4	Comment
0 xxxxx000	Encoder Blue VIN1	Encoder Green VIN3	Encoder Red VIN5	Encoder CVBS VIN8	Digital encoder RGB or CVBS
1 xxxxx001	Bias	Bias	Encoder Chrominance VIN6	Encoder Luminance VIN9	Digital encoder Y/C
2 xxxxx010	VCR Blue VIN2	VCR Green VIN4	VCR Chrominance/Red VIN7	VCR CVBS/Y VIN10	VCR Y/C or RGB
3 xxxxx011	Bias	Bias	Bias	TV CVBS VIN11	TV
4 xxxxx100	Bias	Bias	Encoder Chrominance VIN5	Encoder Luminance VIN3	Digital encoder Y/C
5 xxxxx101	Encoder Blue VIN1	Encoder Green VIN3	Encoder Red VIN5	Aux CVBS VIN12	Encoder RGB and Aux CVBS
6 xxxxx110	Bias	Bias	Aux Chrominance VIN13	Aux CVBS/Y VIN12	Aux Y/C or CVBS
7 xxxxx111	Bias	Bias	Bias	Bias	Video mute (Power on default)

After power on all TV outputs are off (high impedance output) and muted.

TV RGB GAIN Control [Data 5 Bits 3, 4]

I²C setting RGB GAIN	Extra gain/dB
0 xxx00xxx	0 (Power on default)
1 xxx01xxx	+1
2 xxx10xxx	+2
3 xxx11xxx	+3

Video Switch 2: VCR Output [Data 5 Bits 5, 6, 7]

Switch setting		Chrominance Vout5	CVBS/Y Vout6	Comment
0	000xxxxx	Encoder Chrominance VIN5	Encoder CVBS/Y VIN8	Digital encoder Y/C
1	001xxxxx	Encoder Chrominance VIN6	Encoder CVBS/Y VIN9	Digital encoder Y/C or CVBS
2	010xxxxx	VCR Chrominance VIN7	VCR CVBS/Y VIN10	VCR Y/C
3	011xxxxx	Bias	TV CVBS VIN11	TV CVBS
4	100xxxxx	Encoder Chrominance VIN5	Encoder Luminance VIN3	Encoder Y/C
5	101xxxxx	Bias	Aux CVBS VIN12	Aux CVBS
6	110xxxxx	Aux Chrominance VIN13	Aux CVBS/Y VIN12	Aux Y/C or CVBS
7	111xxxxx	Bias	Bias	Video mute (Power on default)

After power on VCR outputs are off (high impedance) and muted.

MIXER CONTROL [Data 6 Bits 0, 1]

I^2C setting		Mixer Output Vout7
0	xxxxxx00	No mix, Vout7 = Vout4 (CVBS)
1	xxxxxx01	Mix of Vout4 (Y) + Vout3 (C)
2	xxxxxx10	No mix, Vout7 = Vin8 (CVBS)
3	xxxxxx11	No mix, Vout7 = Vout4 (CVBS) (Power on default)

Input Clamp Control VIN3 Clamp [Data 6 Bit 2]

xxxxx0xx = GREEN input on VIN3. DC restore clamp active. (Power on default.)

xxxxx1xx = CVBS input on VIN3. Sync tip clamp active.

Input Clamp Control VIN7 Clamp [Data 6 Bit 3]

xxxx0xxx = CHROMINANCE input on VIN7. Chrominance bias applied. (Power on default.)

xxxx1xxx = RED input on VIN7. DC restore clamp applied.

Input Clamp Control VIN5 Clamp [Data 6 Bit 4]

xxx0xxxx = RED input on VIN5. DC restore clamp applied. (Power on default.)

xxx1xxxx = CHROMINANCE input on VIN5. Chrominance bias applied.

Sync Select Control for RGB DC Restore Circuits SYNC_SEL [Data 6 Bits 5, 6]

When the TV output is set to RGB + Y/CVBS mode. Then it is necessary to select the input that contains the sync information for the RGB signal. This will normally be the digital encoder CVBS or VCR CVBS input.

I^2C setting SYNC SEL		Input with sync
0	x00xxxxx	VIN8 (Power on default)
1	x01xxxxx	VIN9
2	x10xxxxx	VIN10
3	x11xxxxx	VIN12

Standby Mode Control [Data 7 Bits 0, 1, 2, 3, 4, 5]

The video outputs VOUT1, 2, 3, 4, 5, 6 can be individually turned off using data byte 7.

0 = Video output off. (Power on default)

1 = Video output on.

Note) When switched off, the video outputs are in a high impedance state. With a normal 150Ω load, the outputs will be pulled to 0V.

Bi-directional Line Control on VCR Scart. Vout5_0V [Data 7 Bit 6]

x0xxxxxx = Vout5 active. Connected to input specified in VCR switch table.

x1xxxxxx = Vout5 set to 0V (Power on default)

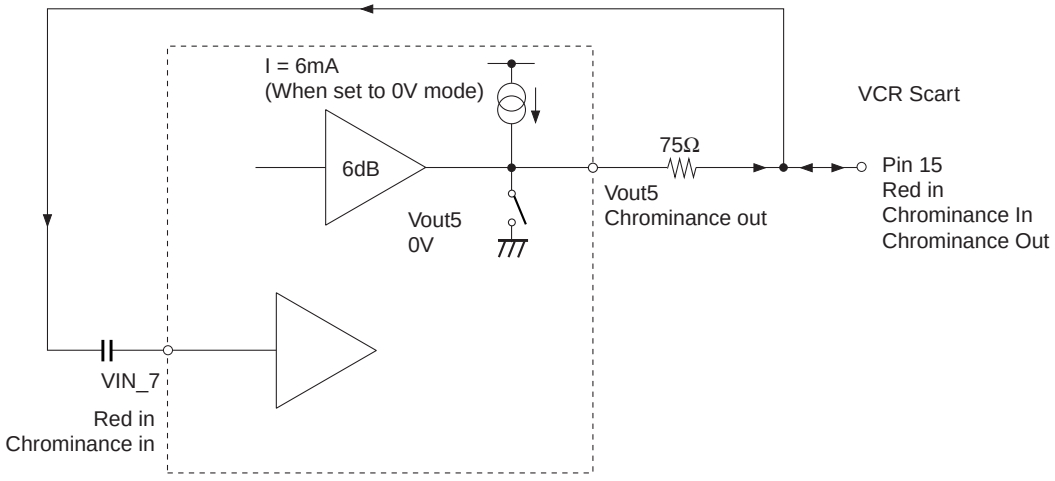


Fig 5. Bi-directional Line to VCR

As Pin 15 on the VCR scart can be bi-directional, either chrominance output or red/chrominance input, it is necessary for output Vout5 to be individually controlled. When the VCR inputs red/chrominance signals, the output Vout5 is set to 0V giving the required line impedance of 75Ω.

I²C Audio Signal Control

Channel Select TV (Phono), VCR [Data 2, 3 Bits 1, 2]

Switch setting		RTV, Phono_R, ROUT1	LTV, Phono_L, LOUT1
0	xxxxx00x	Rin1	Lin1
1	xxxxx01x	Rin2	Lin2
2	xxxxx10x	Rin3	Lin3
3	xxxxx11x	Rin4	Lin4

After power on Rin4/Lin4 are selected.

Mono Switch TV [Data 2 Bits 3, 4, 5]

Switch setting		Connection to R channel output	Connection to L channel output	Comment
0	xx000xxx	R	L	Normal
1	xx001xxx	(R + L mix)	(R + L mix)	Mono mix
2	xx010xxx	L	R	Channel swap
3	xx011xxx	R	R	Right channel only
4	xx100xxx	L	L	Left channel only
5	xx101xxx	R	L	Normal
6	xx110xxx	R	L	Normal
7	xx111xxx	R	L	Normal (power on default)

Mono Switch VCR [Data 3 Bits 3, 4, 5]

Switch setting		Connection to R channel output	Connection to L channel output	Comment
0	xx000xxx	R	L	Normal
1	xx001xxx	(R + L mix)	(R + L mix)	Mono mix
2	xx010xxx	L	R	Channel swap
3	xx011xxx	R	R	Right channel only
4	xx100xxx	L	L	Left channel only
5	xx101xxx	R	L	Normal
6	xx110xxx	R	L	Normal
7	xx111xxx	X	X	All audio outputs disabled (RTV, LTV, PHONO_R, PHONO_L, MONO, ROUT1, LOUT1) (power on default)

PHONO BYPASS [Data 2 Bit 0]

xxxxxxx0 = Phono outputs connected after volume control block. (Power on default)

xxxxxxx1 = Phono outputs connected before volume control block.

TV VOL BYPASS [Data 2 Bit 6]

x0xxxxxx = TV outputs connected after volume control block. (Power on default)

x1xxxxxx = TV outputs connected before volume control block.

MONO SWITCH [Data 2 Bit 7]

0xxxxxxx = Mono output connected to mix of TV R + L channels. (Power on default)

1xxxxxxx = Mono output connected to mix of RIN1 + LIN1 inputs.

VOLUME CONTROL [Data 1 Bits 1, 2, 3, 4, 5]

Setting		Volume gain
0	xx00000x	+6dB
1	xx00001x	+4dB
2	xx00010x	+2dB
3	xx00011x	0dB (power on default)
4	xx00100x	–2dB
5	xx00101x	–4dB
6	xx00110x	–6dB
7	xx00111x	–8dB
8	xx01000x	–10dB
9	xx01001x	–12dB
10	xx01010x	–14dB
11	xx01011x	–16dB
:		:
31	xx11111x	–56dB

AUDIO RIN1/LIN1 GAIN [Data 1 Bits 6, 7]

Setting		Input attenuation
0	00xxxxxx	–6dB (Power on default) **(Note 1)**
1	01xxxxxx	–3dB
2	10xxxxxx	+0dB
3	11xxxxxx	+3dB

Note 1) The power on default is –6dB. As the output amplifiers have a nominal +6dB gain the overall input to output gain is 0dB.

OVERLAY ENABLE [Data3 Bit 0]

xxxxxxx0 = Overlay off (Power on default)

xxxxxxx1 = Overlay on: Rin3 and Lin3 are mixed and added to Rin1, Lin1 channels. Rin1 and Lin1 are attenuated by 16dB before mixing with the tone.

TV Mute and Zero Cross Operation

When the zero cross is switched on (ZCD = 1), volume control changes are only implemented when the audio signal passes though the zero cross point. Similarly, when a mute instruction is sent, the TV outputs are only muted when the signal passes the zero cross point. This eliminates any click noise.

There are two TV audio mute control bits in the bus map. By having two bits it allows the TV outputs to be muted, the TV channel changed and then un-muted all in one I^2C write operation. The normal structure for a click free audio channel change is as follows:

Data 1: Mute the TV audio output with the ZCD switched on.

Data 2: Change the TV audio source.

Data 3: Un-mute the TV audio output again with the ZCD switched on.

Operation of the Mute circuit

TV Aud Mute [Data 1 Bit 0] [Data 3 Bit 7]	ZCD [Data 7 Bit 7]	TV, Phono and Mono output
0	0	Un-mute immediately
0	1	Un-mute on next zero cross
1	0	Mute immediately
1	1	Mute on next zero cross

After power on TV Audio Mute = 1 and ZCD are set to 1.

TV INPUT MUTE [Data 4 Bit 7]

0xxxxxxx = The input to the TV switch is not muted.

1xxxxxxx = The input to the TV switch is muted. (power on default)

VCR INPUT MUTE [Data 6 Bit 7]

0xxxxxxx = The input to the VCR switch is not muted.

1xxxxxxx = The input to the VCR switch is muted. (power on default)

OUTPUT LIMIT [Data 3 Bit 6]

This will limit the output level of the volume control block to 2.2Vrms maximum.

0xxxxxxx = The volume control outputs are not limited. (power on default)

1xxxxxxx = The volume control outputs are limited to 2.2Vrms.

Fast Blanking Operation (Pin 16 on SCART), FBLK

The fast blanking signal instructs the TV to select either the external CVBS information or the external RGB information. This is used to superimpose an on screen display (OSD) presentation (normally RGB) upon a CVBS background. Fast blanking information has the same nominal phase as the RGB and CVBS signal, and is defined as follows,

Fast blanking output at scart,

1. CVBS mode: Scart pin voltage = 0 to 0.4V
2. RGB mode: Scart pin voltage = 1 to 3.0V

The threshold voltage is approximately 0.75V at the scart input.

Fast Blanking I²C Control

In the CXA2161R, there are two fast blanking inputs, one associated with the digital encoder input (FBLK_IN1) and another associated with the VCR RGB/CVBS input (FBLK_IN2). These can be selected and switched to the output using an I²C instruction. In addition, the fast blank output pin can be set to a constant 0V or +3.5V by means of the I²C control. Hence there are four possible states. These are set according to the following table.

FAST_BLANK [Data 4 Bits 0, 1]

I²C setting BLANK_LEVEL	Fast blank output pin voltage
0 xxxxxx00	0V (Power on default)
1 xxxxxx01	Same level as Fast Blank in 1 (0/+3.5V)
2 xxxxxx10	Same level as Fast Blank in 2 (0/+3.5V)
3 xxxxxx11	+3.5V

Fast Blank Output Interface

The Fast Blanking output pin is connected to the scart via a 75Ω resistor.

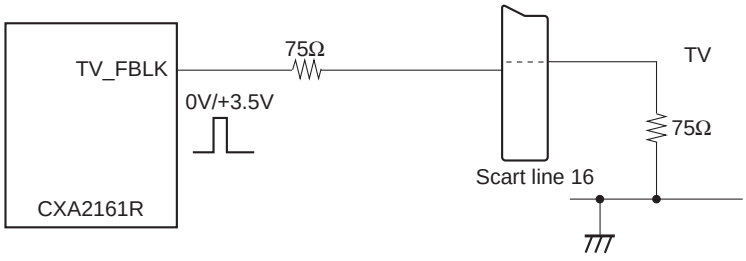


Fig. 6. Fast Blanking Output Interface

Function Switching Operation (Pin 8 on scart)

The function switch facility is designed to read the status of the SCART function Pin 8 from the VCR scart connector and store this in the status register. Both, VCR and TV function lines can be set to outputs and controlled by I^2C. The TV function line has two modes, the first being control via I^2C and secondly the follow mode where the output will follow the same state as the VCR input.

Setting the Direction for the Function Lines

The input and control for the function lines is set by the FNC_DIR and FNC_FOLLOW bits.

FNC_FOLLOW [Data 4 Bit 3]	FNC_DIR [Data 4 Bit 2]	VCR Pin 8	TV Pin 8
0	0	Input (Level stored in read register)	Output Controlled by FNC_LEVEL
0	1	Output Controlled by FNC_LEVEL	Output Holds previous level
1	0	Input (Level stored in read register)	Output Follows same level as VCR input
1	1	Output (Both set to same voltage controlled by FNC_LEVEL)	

FNC_LEVEL [Data 4 Bits 4, 5]

These bits set the voltage at the (TV_FNC or VCR_FNC) outputs. The output is determined by the table above.

I^2C control FNC_LEVEL	Voltage at output	Mode
0 xx00xxxx	< 2V	Internal TV
1 xx01xxxx	> 4.5V, < 7V	External scart input 16:9 mode
2 xx10xxxx	< 2V	Internal TV
3 xx11xxxx	> 9.5V	External scart input 4:3 mode

Note) After power on the output is internal TV mode ie. 0V at the pin.

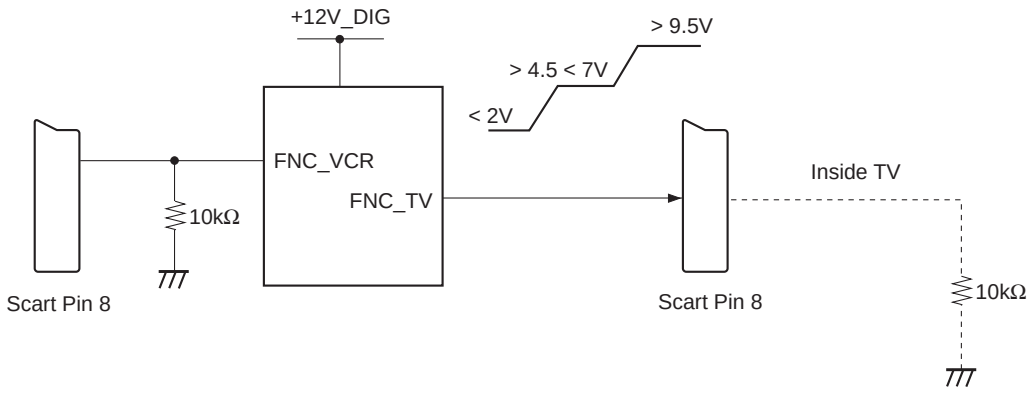


Fig. 7. TV Function Switch Output

Logic and Interrupt Output

These open collector output pins can be used for an interrupt line to a microprocessor or as a general purpose logic output.

Interrupt Output

The INTRUPT pin will become a current sink for approximately 2µs when the VCR input function line changes from:

a) 0 to 6V, 6 to 0V b) 0 to 12V, 12 to 0V c) 6 to 12V, 12 to 6V

This pin will normally be connected to +5V through a 10kΩ resistor.

Logic Output

The logic output level can be changed using the logic output bit in the I^2C register, LOGIC_LEVEL.

LOGIC LEVEL [Data 4 Bit 6]

x0xxxxxx = Current sink mode resulting in < 0.4V saturation voltage on logic pin. (Power on default)

x1xxxxxx = Open collector/high output impedance on logic pin.

Imax during current sink = 1mA

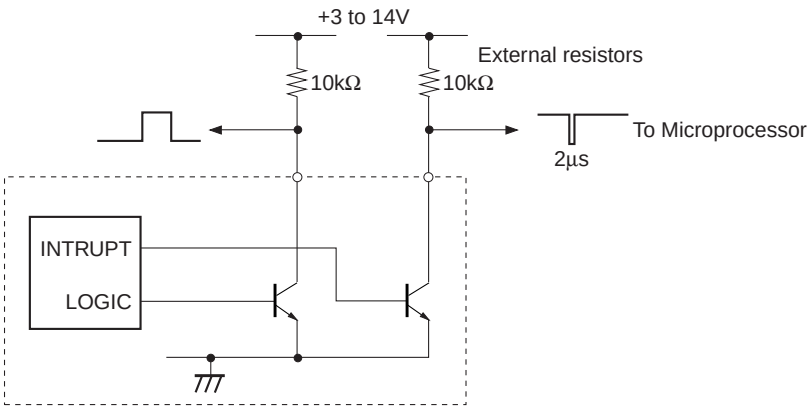


Fig. 8. INTRUPT and Logic Line Interface

Read Mode Status Register

The following information can be read from the status register:

FNC VCR [Bits 0, 1]

The status register bits 0, 1 hold the level of the input function line

Input pin voltage FNC_VCR	SCART mode	Data 8	
		b1	b0
0 to +2V (default)	(Internal)	0	0
+4.5 to +7V	(16:9 External)	0	1
+9.5 to +12V	(4:3 External)	1	1

SYNC DETECT [Bit 2]

Once a valid sync signal is detected on the input selected by SYNC_SELECT this bit is set to 1. The bit is reset to 0 every time the SYNC_SELECT is changed. It is assumed that when a video input is in-active then the input level will be 0V with minimum noise.

POD (Power on Detect) [Bit 4]

This bit is set to 1 after power on. It is then changed to 0 after the first I^2C read. It is used to detect if the supply has been corrupted. If the POR bit is read as 1 at any time then the IC should be re-initialized to the correct I^2C settings.

Zero Cross Status [Bit 5]

This audio function is used to determine if an input audio signal has passed the zero cross point. For dual supply operation the zero cross point is 0V. For Single supply, the zero cross point is approximately 6V.

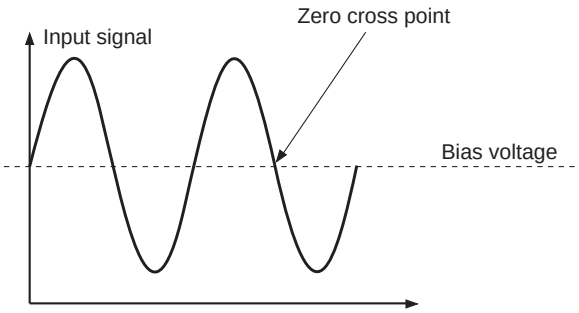


Fig. 9. Zero Cross Point

0 = No zero cross detected

1 = Signal has passed through zero cross point.

Description of Operation

Video Section

Inputs and Outputs

The video section comprises of thirteen (13) high impedance inputs switched through to seven (7) video outputs. An internal +6dB amplifier is connected to each output. The amplifier is required to compensate for the 6dB attenuation that occurs at the 75Ω series output resistor. The outputs VOUT_1 to VOUT_6 are capable of driving 150Ω loads. Output VOUT_7 is designed to interface to an RF Modulator but requires an external buffer to drive a 75Ω load.

Composite/Luminance Inputs

The 4 composite (or luminance) inputs are ac coupled to the input pins. The signals are first sync tip clamped to a set level. These clamps are permanently active, therefore these inputs should only be used for signals with a sync.

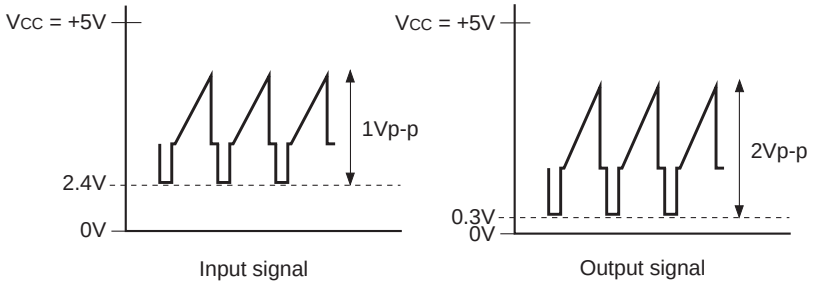


Fig. 10. CVBS/Y Waveforms

RGB Inputs

The RGB inputs are ac coupled to the input pins. The inputs have a dc restore circuit, which is used to set the blanking level to a fixed voltage. The clamps are controlled by the timing signal provided by the sync detect circuit. It is necessary to select the correct luma or CVBS signal associated with the RGB inputs for the sync select circuit. It is assumed that a sync signal will not be present on any of the RGB input signals. For inputs that can be either red or chrominance then the clamp can be switched between the dc restore mode (for red input) and average level bias (for chrominance). The RGB signals are fed through additional amplifiers that are controlled via I^2C. These allow the nominal 0.7Vp-p signal to be increased to 0.8Vp-p, 0.9Vp-p or 1Vp-p. When the TV output is in Y/C mode, the RGB gain should be set to 0dB to prevent over amplification of the chrominance output.

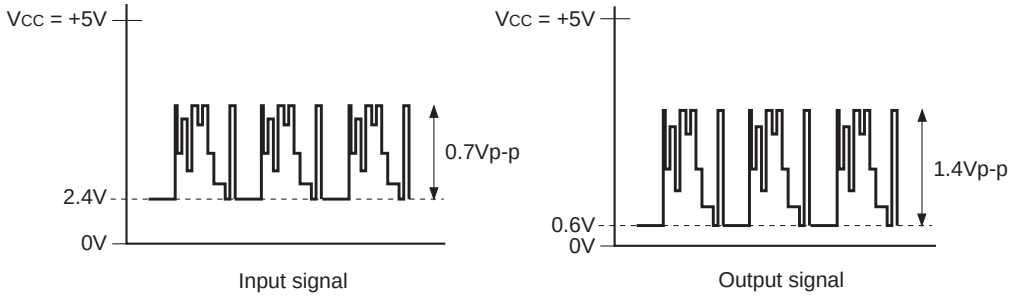


Fig. 11. RGB Waveforms

Sync Detection Circuit

The clamp signals, used to restore the RGB level, are generated from the sync detect circuit. By using the SYNC_SELECT control bits, the 4 different CVBS/Y inputs may be selected. Once selected, the clamped signal is compared with a threshold voltage 65mV above the tip level. If the signal is less than this threshold it is not passed to the next block. If greater than the threshold, it is passed to the discrimination circuit that checks that the duty cycle is greater than 91%. The discrimination block also contains a time constant which, when a sync is detected, holds the status line high for at least 11 video lines. If a valid sync signal is detected the SYNC_DETECT bit in the read register is set to 1.

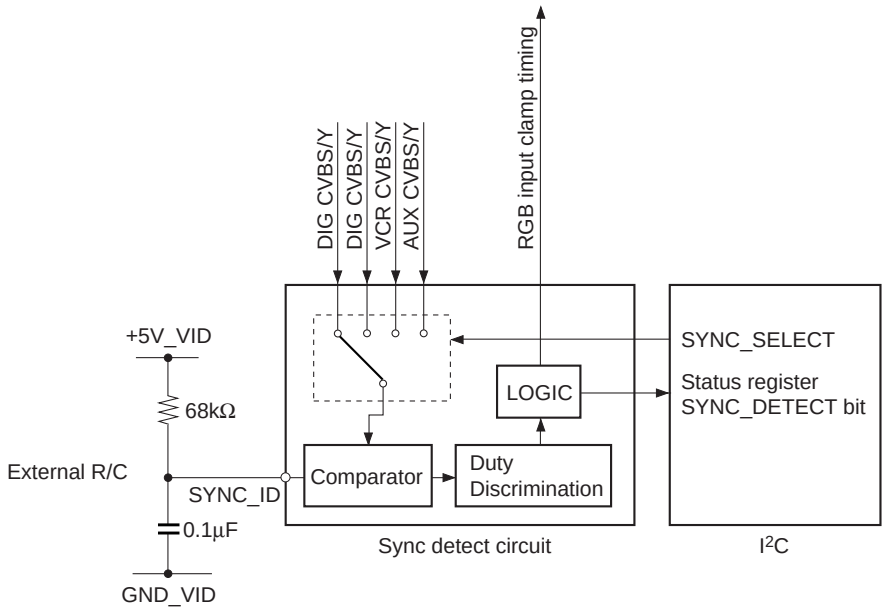


Fig. 12. Sync Detection Circuit

Chrominance Inputs

The chrominance signals are ac coupled to the input pins. The inputs have a fixed dc bias that sets the average level to approximately 3V for VIN_5 & VIN_7 and 2.35V for VIN_6 & VIN_13. For inputs that can also be RED signals the input circuit can be switched to the dc restore mode.

Typical waveforms:

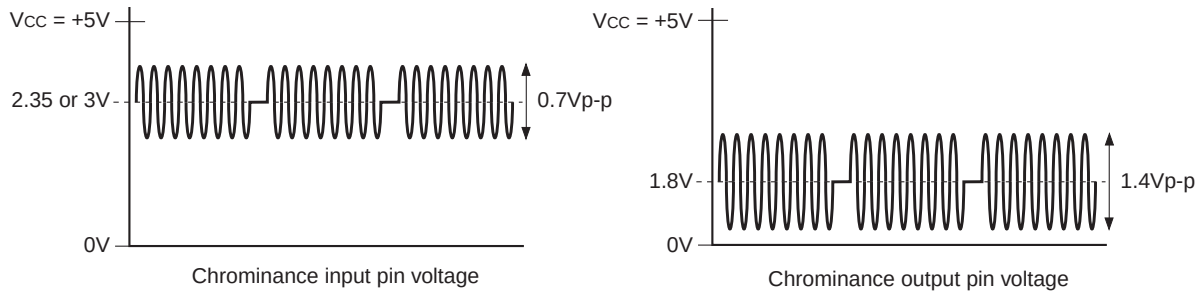


Fig. 13. Chrominance Waveforms

Y/C Mixer

A Y/C mixer can be used for mixing Luminance and Chrominance signals for use with an external RF modulator connected to VOUT_7. The Y/C mixer is controlled via the I²C data bus. The signal may be a mix of the TV Y/C signals or simply the TV CVBS signal. It is also possible to select the CVBS signal from the digital encoder. The circuit is shown in Fig 14. with a trap circuit used to give 6dB attenuation at 4.43MHz of the Luminance signal. The output VOUT_7 cannot drive loads higher than 20kΩ resistive. If it is necessary to drive a 75Ω load with this output then an external emitter follower arrangement should be used.

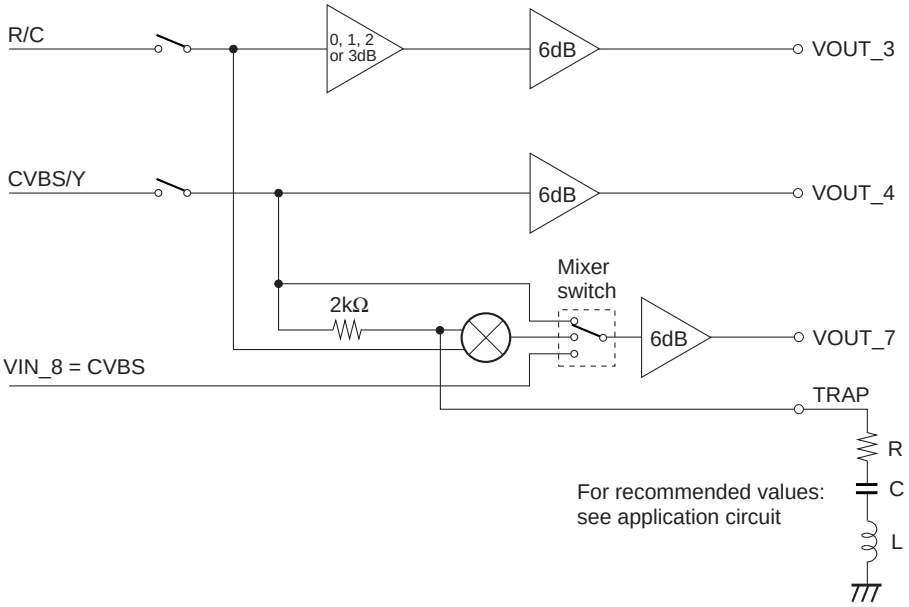


Fig. 14. Internal Y/C Mixer Circuit

Switching the Video Outputs Off

Each video output can be individually turned off using the I²C. When turned off, the output is set to a high impedance state and hence the current consumption and power dissipation is reduced. After power on, all the video outputs are set to the high impedance state.

Typical Video Interface Circuits

Single or Dual Supply

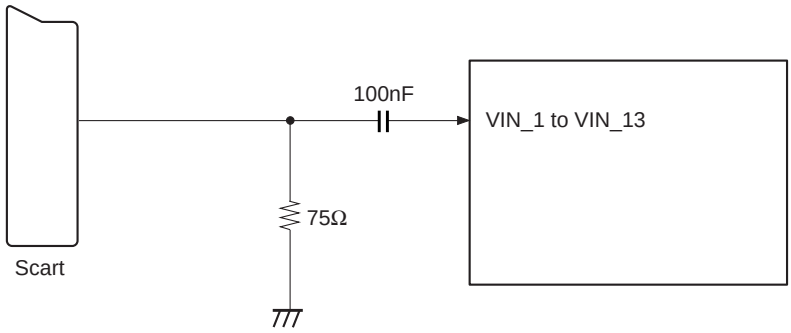


Fig. 15. Video Input Interface

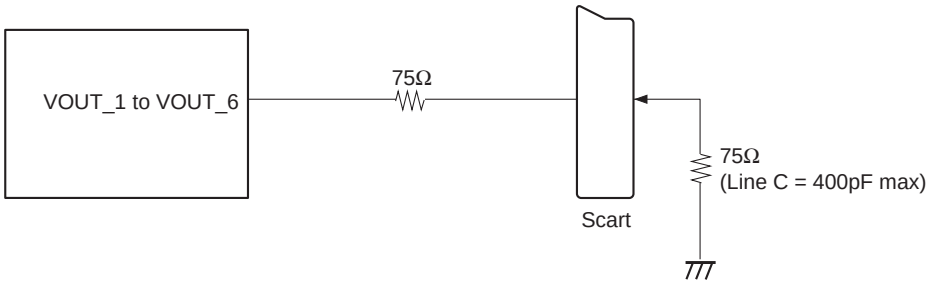


Fig. 16. Video Output Interface

Audio Section

Inputs and Outputs

The audio system consists of 4 stereo inputs, 2 stereo outputs and separate mono and Phono outputs. The stereo outputs can be connected to any one of the 4 stereo inputs. All audio inputs have a –6dB attenuator except RIN_1 and LIN_1. Therefore, the net gain of the audio system from input to output is 0dB, as an amplifier having +6dB of gain follows the internal switch. The stereo input RIN_1/LIN_1 has extra switchable gain as this input is typically connected to an audio DAC with full scale of 1Vrms or less.

The output impedance of each audio amplifier is near zero, and may be directly coupled to the scart in the case of a dual supply but must be ac coupled through a capacitor (typically 10µF) for the single supply case. The outputs are capable of driving 600Ω loads. The user may add additional low pass filters to the outputs.

TV Output Switching

The TV audio section is composed of an audio switch followed by a volume control stage. The volume is adjustable from +6dB to –56dB in 2dB steps. The volume control block includes a switchable limiter function to prevent the output signals exceeding 2.2Vrms. When activated, the output signals from the volume control block will be clamped to 2.2Vrms. A mono switch that allows the mixed R + L signal to be switched to the R and L output channels follows the volume control section. The mono switch is also capable of routing the R signal onto both R and L channel and similarly the L signal to the R and L output channels. This may be used if the audio channels consist of two different languages. It is also capable of swapping the R and L channels.

TV Mute

This I^2C mute function acts only on the TV, Phono and mono audio circuits. Audio mute will be implemented after an audio zero cross detection to reduce click noise if ZCD = 1.

Zero Cross Detector (ZCD)

The zero cross detector reduces the effect of click noise when implementing a volume change or an audio mute. The volume change or mute instruction sent by I^2C will only be implemented when a minimal (ie zero cross) signal amplitude is detected.

It can be seen from the I^2C write format that the same mute bit occurs in DATA1 and DATA3. This allows the software to action a mute, then after a delay (1/Audio_freq (min)) make any suitable changes to the audio source and then un-mute the output buffer. Such a period provides ample time to allow any audio signals to pass the zero cross point before the signal source is changed.

VCR Output Switching

The outputs ROUT1, LOUT1 have a fixed gain of 0dB from the input. If any attenuation is required then it is possible to insert a series resistance on the input. Again, this output has a mono switching block that allows the mixed R + L to be inserted on both output channels.

Phono outputs

There is a stereo Phono output that carries the same signal as the TV output. This is typically used for connection to a hi-fi. The signal level of the Phono outputs is normally the same as the TV outputs however it is possible to bypass the volume section and set the Phono outputs to a fixed level. If any attenuation is required then this can be done externally.

Mono Output

The mono output for the RF modulator has two settings. The first is a mix of the TV R + L channels. In this case, the output signal will have the same volume control as the RTV/LTV outputs. The second setting is a mix of the audio DAC inputs (RIN_1 + LIN_1). In this setting the output will always have fixed volume and if the tone overlay is used, this will appear on the output.

Audio Overlay

The inputs RIN_3, LIN_3 may be used for a normal stereo audio input or alternatively to overlay an external audio source onto the TV outputs. This may be a tone or voice. The R and L inputs are mixed and then added equally to the RIN_1 and LIN_1 inputs. The I^2C control bit Audio overlay enable is used to switch on this facility and control the attenuator block on RIN_3 which is set to give an extra 5dB of attenuation when switched on. If two tones are used then it is up to the user to switch them individually before the A/V switch. When the tone overlay is activated, the signals RIN_1, LIN_1 are attenuated by approximately 16dB before mixing.

Audio Disable

All the audio outputs may be disabled using the Audio Output Disable function in the VCR mono switching block [Data Byte 3 Bits 3, 4, 5 set to 111]. This disable mode is different from the normal mute as it can be used for power reduction in stand by modes.

Typical Audio Interface Circuits

Supply type 1: Dual supply

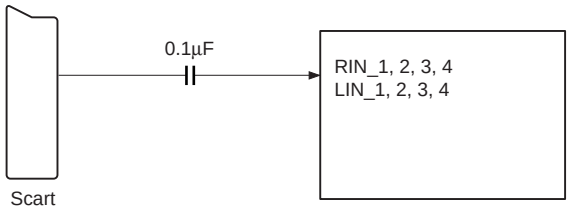


Fig. 17. Audio Input Interface

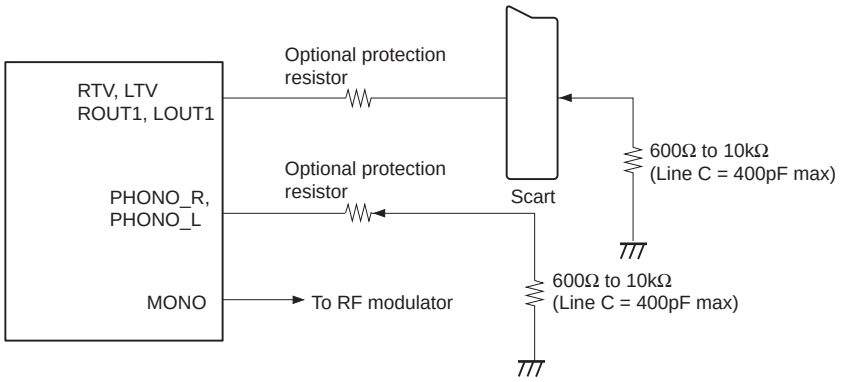


Fig. 18. Audio Output Interface

Supply type 2: Single supply

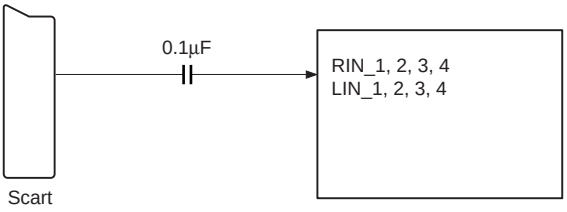
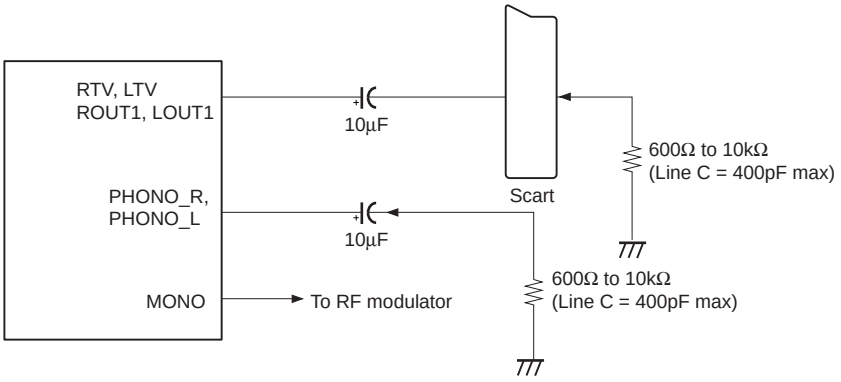


Fig. 19. Audio Input Interface



The user may use larger capacitors if required.

Fig. 20. Audio Output Interface

Application in Set Top Box

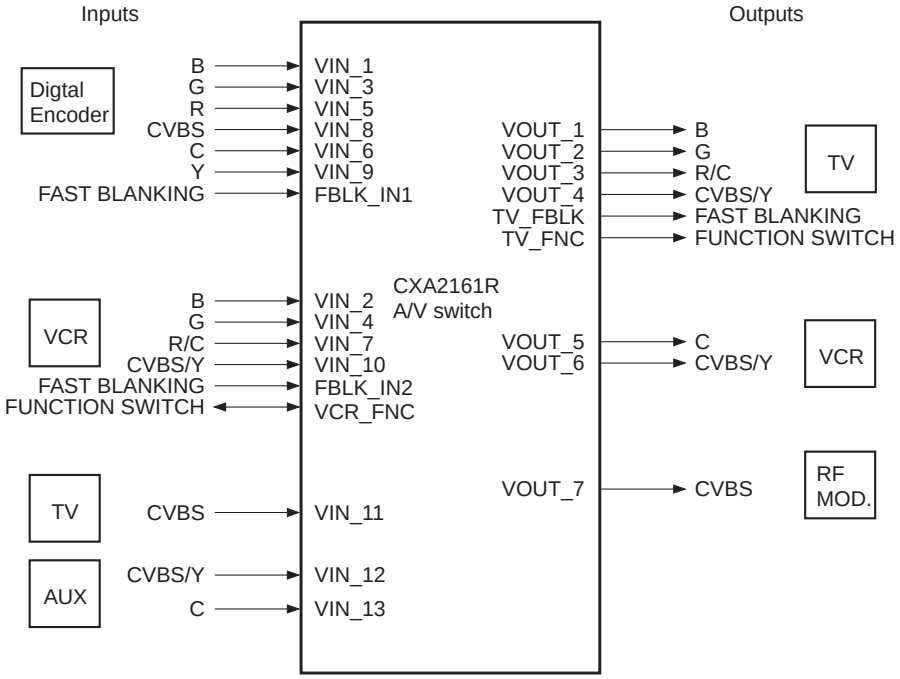


Fig. 21. Video Application with 6 Output Digital Encoder

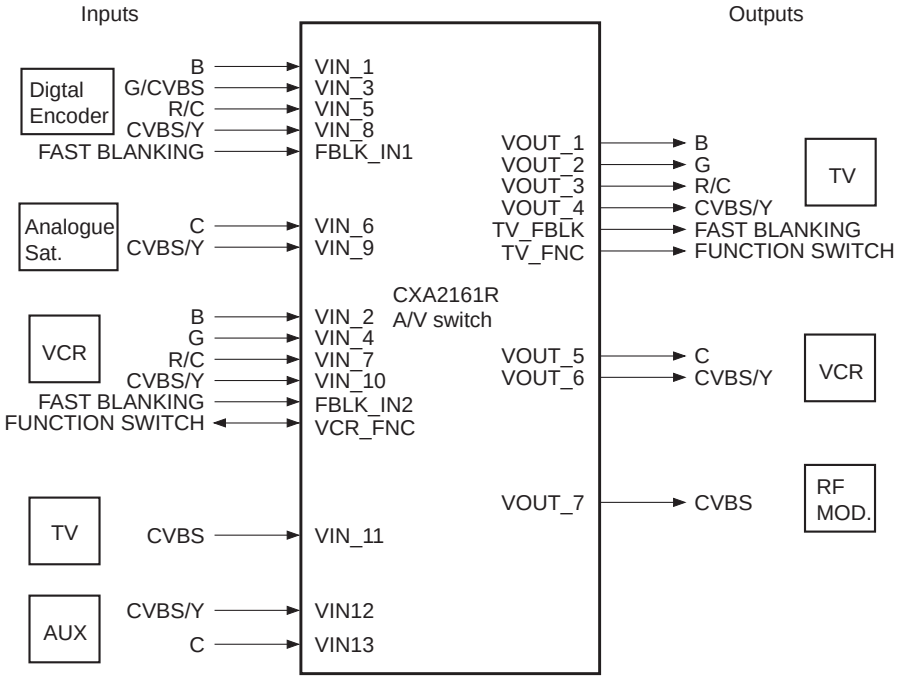


Fig. 22. Video Application with 4 Output Digital Encoder

Audio Application

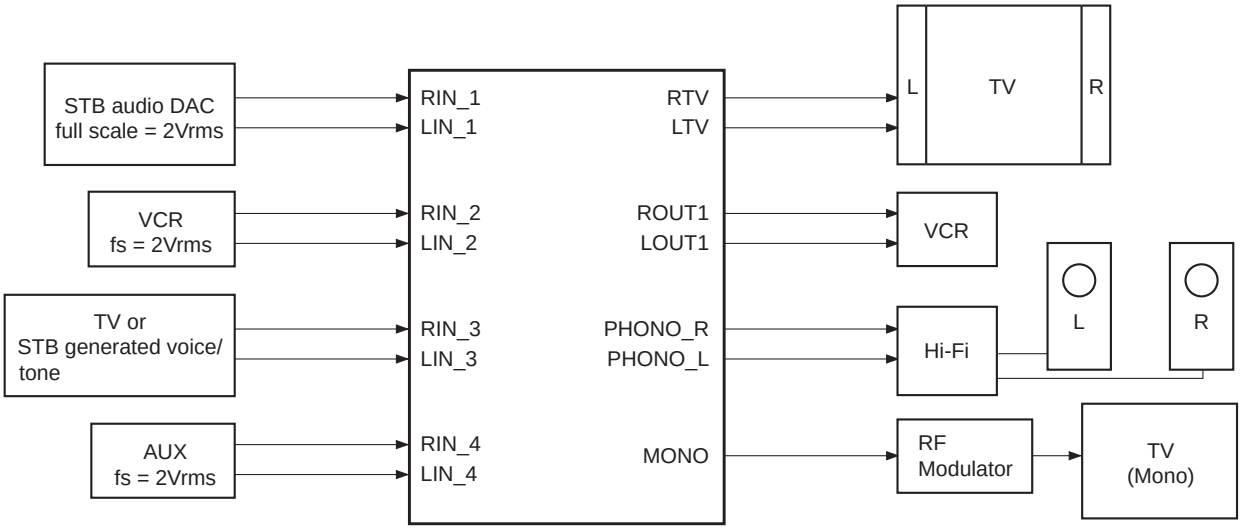


Fig. 23. Audio Application

Supply Connections

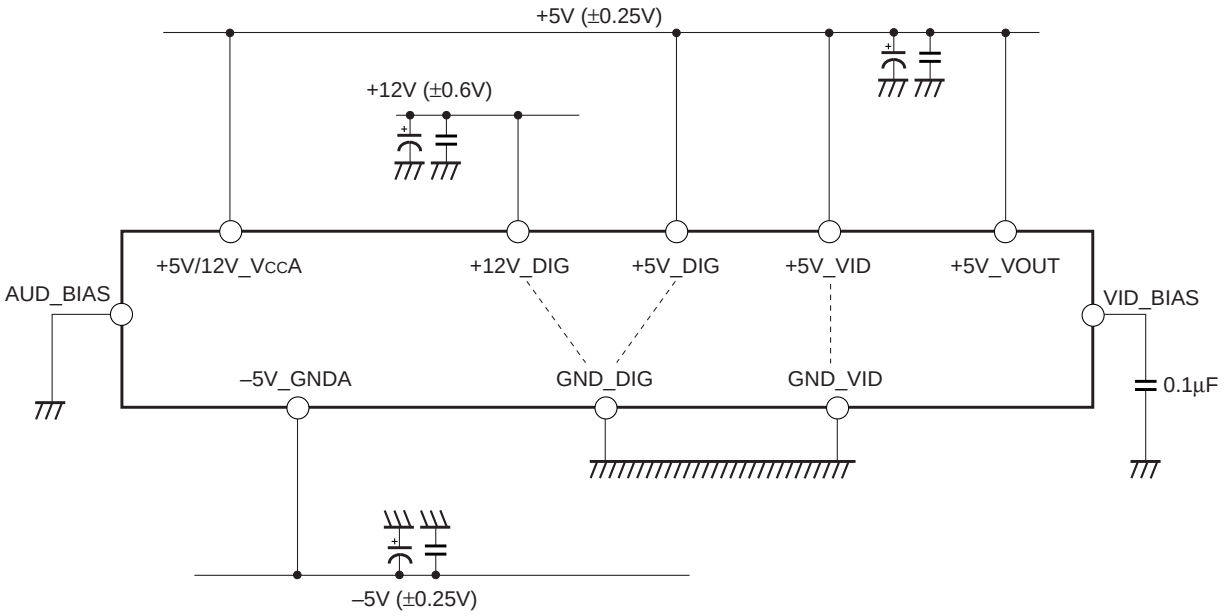


Fig. 24. Dual Supply

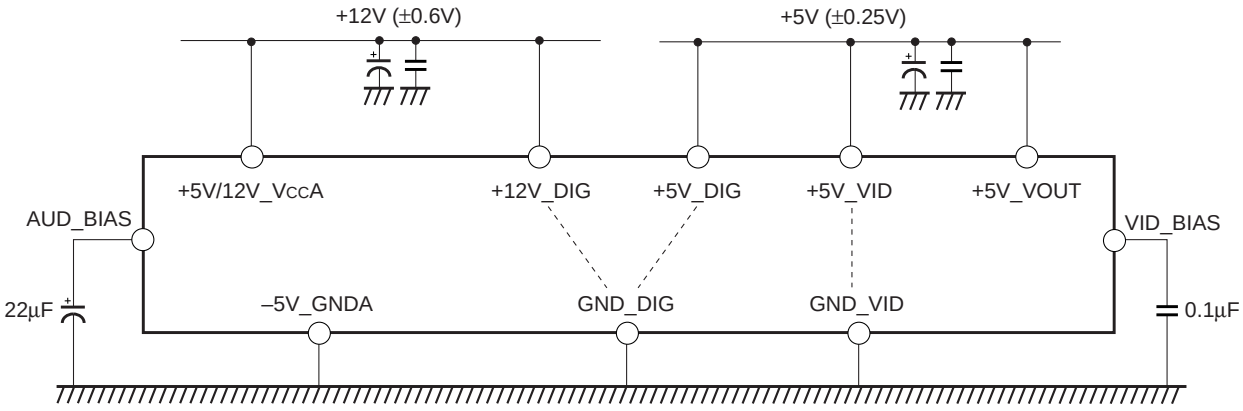
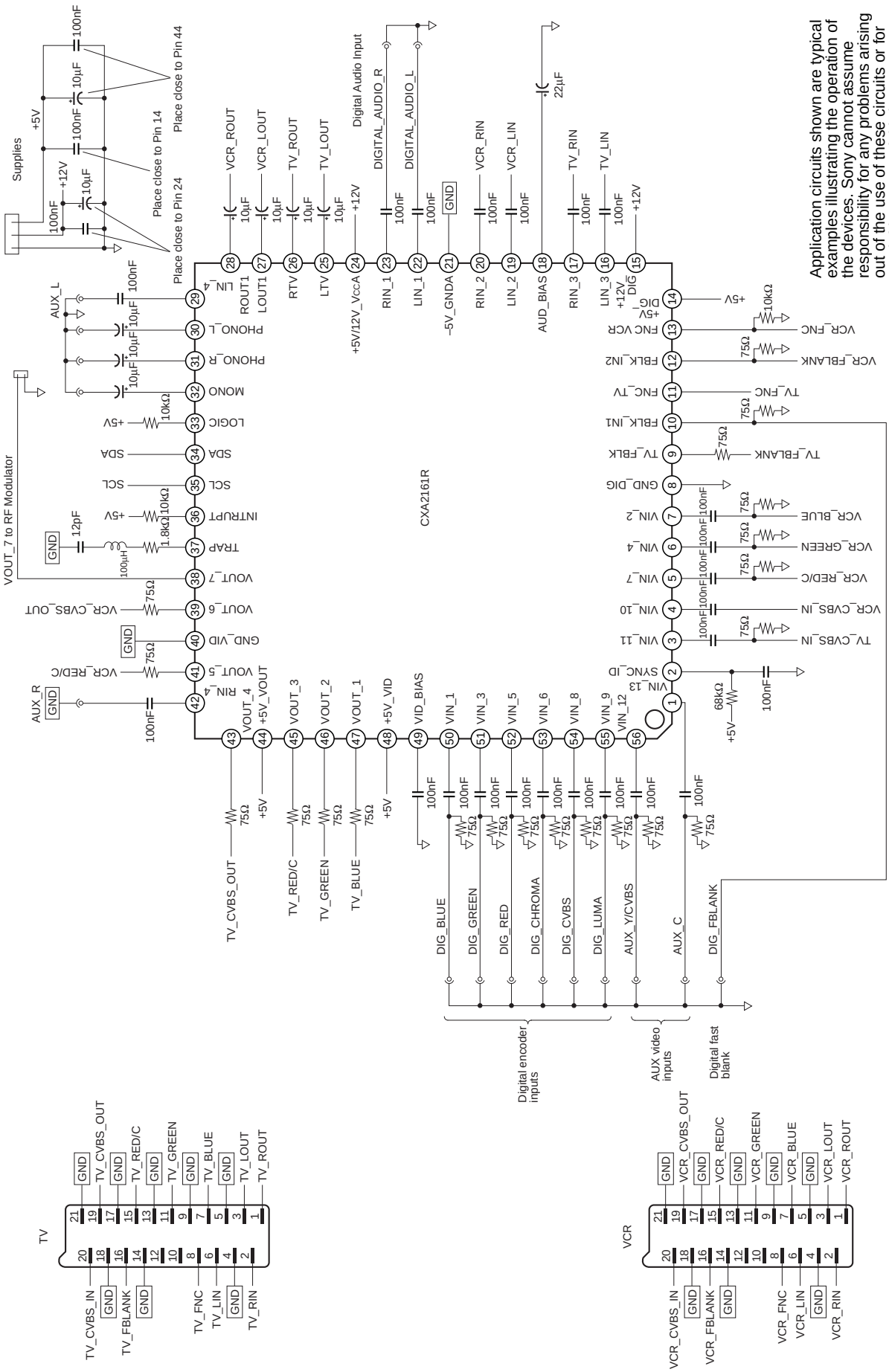
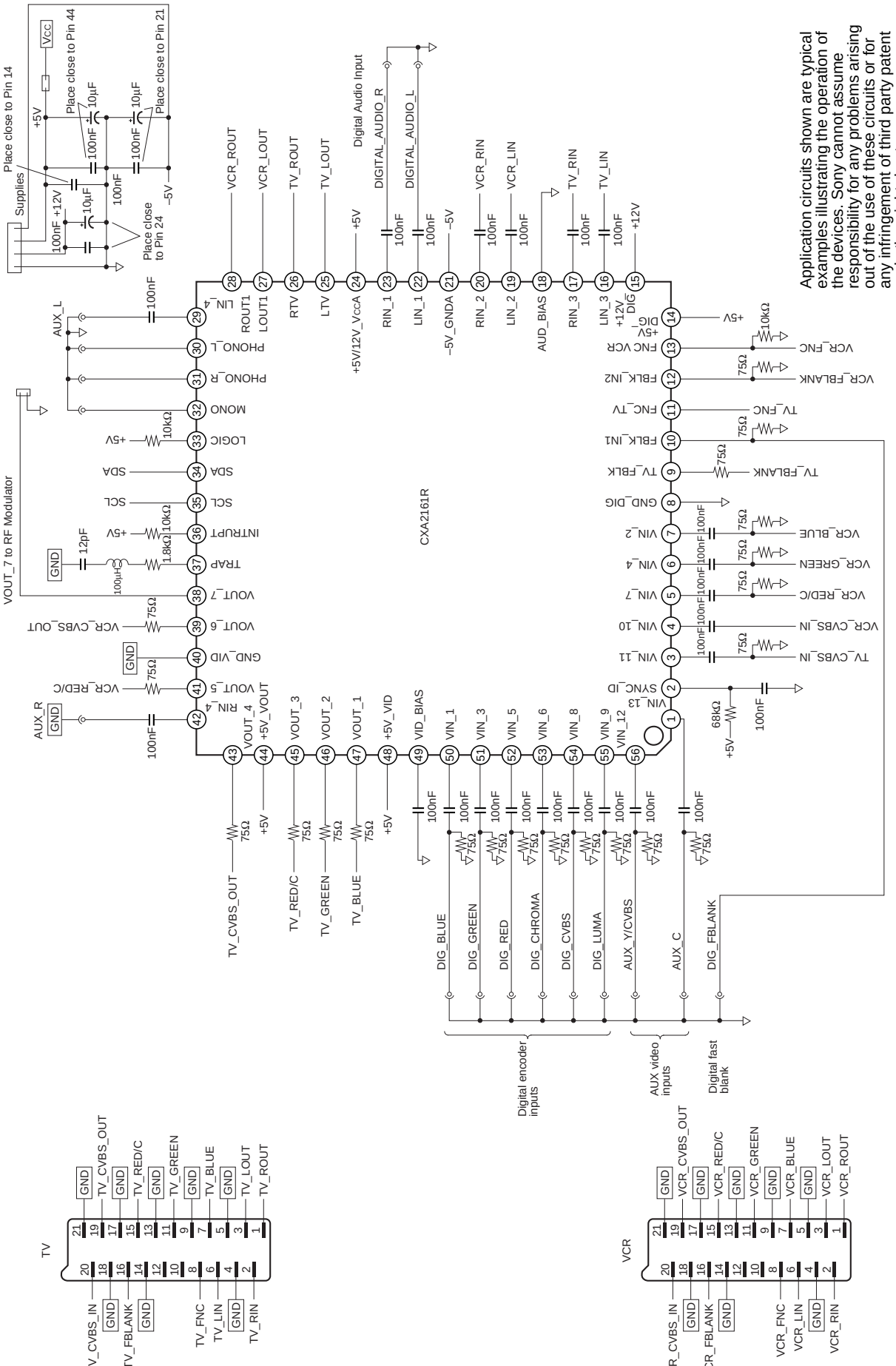


Fig. 25. Single Ended Supply

Application Circuit 1
Single Ended Supply



Application Circuit 2
Dual Supply



Notes on operation

1) Supply de-coupling capacitors, 10nF and 10µF in parallel should be inserted as close as possible to the supply Pins 14, 15, 24 and 44. When using the dual supply configuration apply the capacitors to Pin 21 in addition to the listed supply pins.

2) For best results with dual supply configuration, two +5V supplies should be used, audio (Pin 24) and video/digital (Pins 14, 44 and 49).

3) To minimize crosstalk, attention should be given to the routing of audio and video to the IC inputs. PCB track lengths should be kept as short as possible and preferably, audio placed on a separate layer to the video.

4) Attention should be given to the electrolytic capacitors on the output pins. In single supply configuration the audio pin dc bias voltage will be approximately 6.0V, therefore the positive terminal of the capacitors should be orientated towards the device pin.

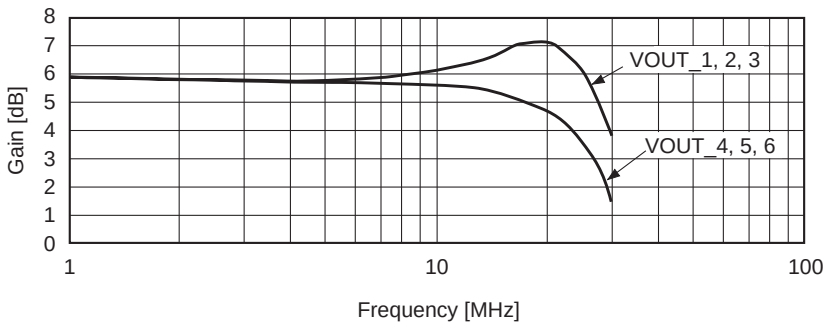
5) To minimise stray capacitance the 75Ω series resistor on video outputs VOUT_1 to VOUT_6 should be mounted as close as possible to the device Pins 47, 46, 45, 44, 41 and 39.

6) When driving video loads with impedance of 75Ω, video output VOUT_7 (Pin 38) must be connected to the load via a buffer or line driver. This buffer should be located close to the output (Pin 38).

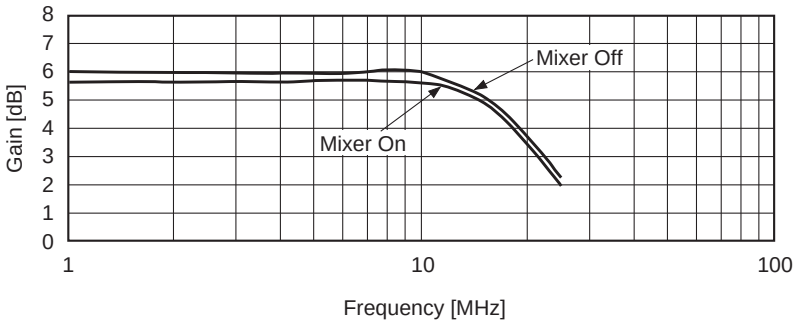
7) In dual supply mode, series protection resistors may be added on Audio outputs which are connected Scart connectors.

Typical Performance Curves

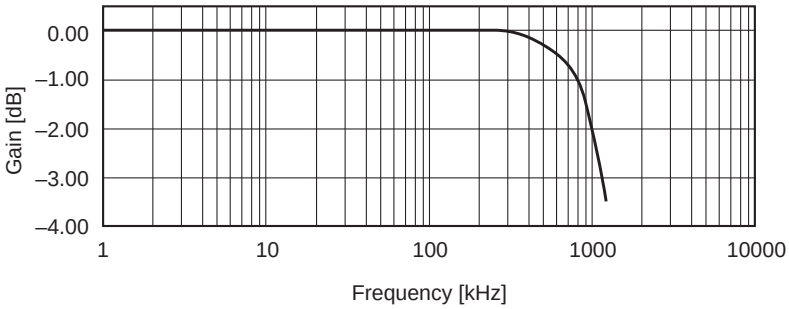
Video gain – VOUT_1, 2, 3, 4, 5, 6



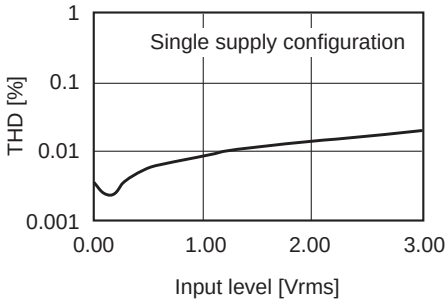
Video gain – VOUT_7



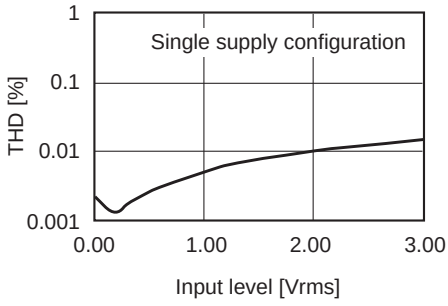
Audio gain



Audio output distortion TV outputs

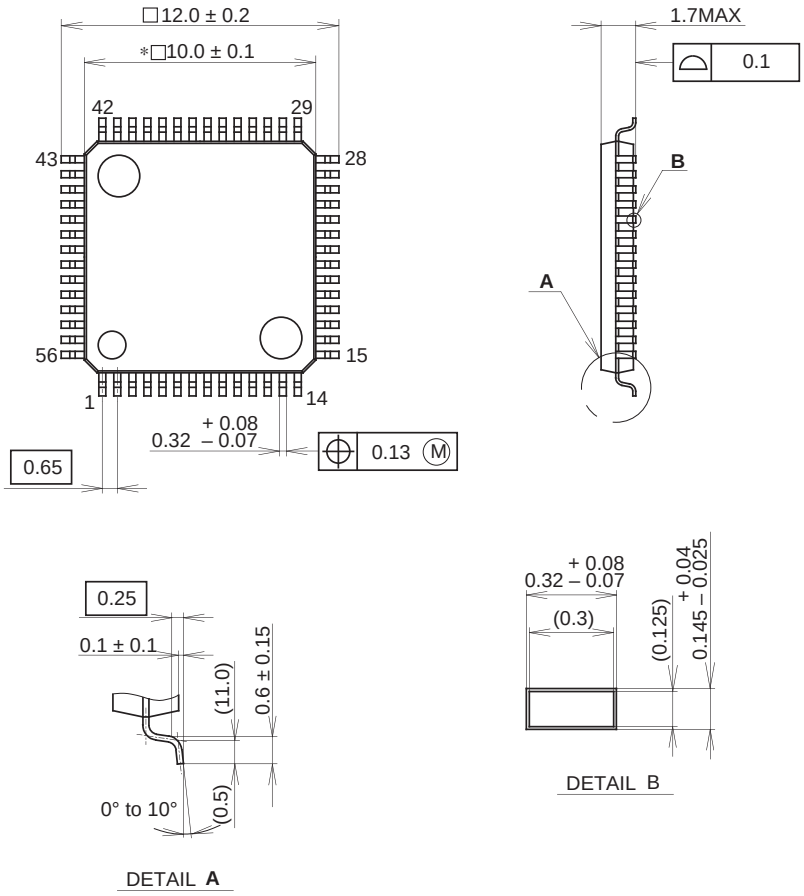


Audio output distortion ROUT1, LOUT1



Package Outline Unit: mm

56PIN LQFP(PLASTIC)



NOTE: Dimension "*" does not include mold protrusion.

SONY CODE	LQFP-56P-L01
EIAJ CODE	LQFP056-P-1010
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.3g