SONY

CXA3099N

IF Amplifier for M-ary FSK Pagers

For the availability of this product, please contact the sales office.

Description

The CXA3099N is a low current consumption FM IF amplifier which employs the newest bipolar process. It is suitable for M-ary FSK pagers.

Features

- Low current consumption: 590 µA (typ. at V_{CC} = 1.4 V)
- Low voltage operation: V_{CC} = 1.1 to 4.0 V
- Small package 16-pin SSOP
- Needless of IF decoupling capacitor
- Reference power supply for operational amplifier and comparator
- IF input, V_{CC} standard

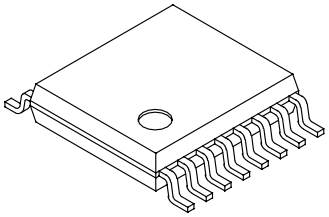
Applications

M-ary FSK pagers

Structure

Bipolar silicon monolithic IC

16 pin SSOP (Plastic)



Absolute Maximum Ratings

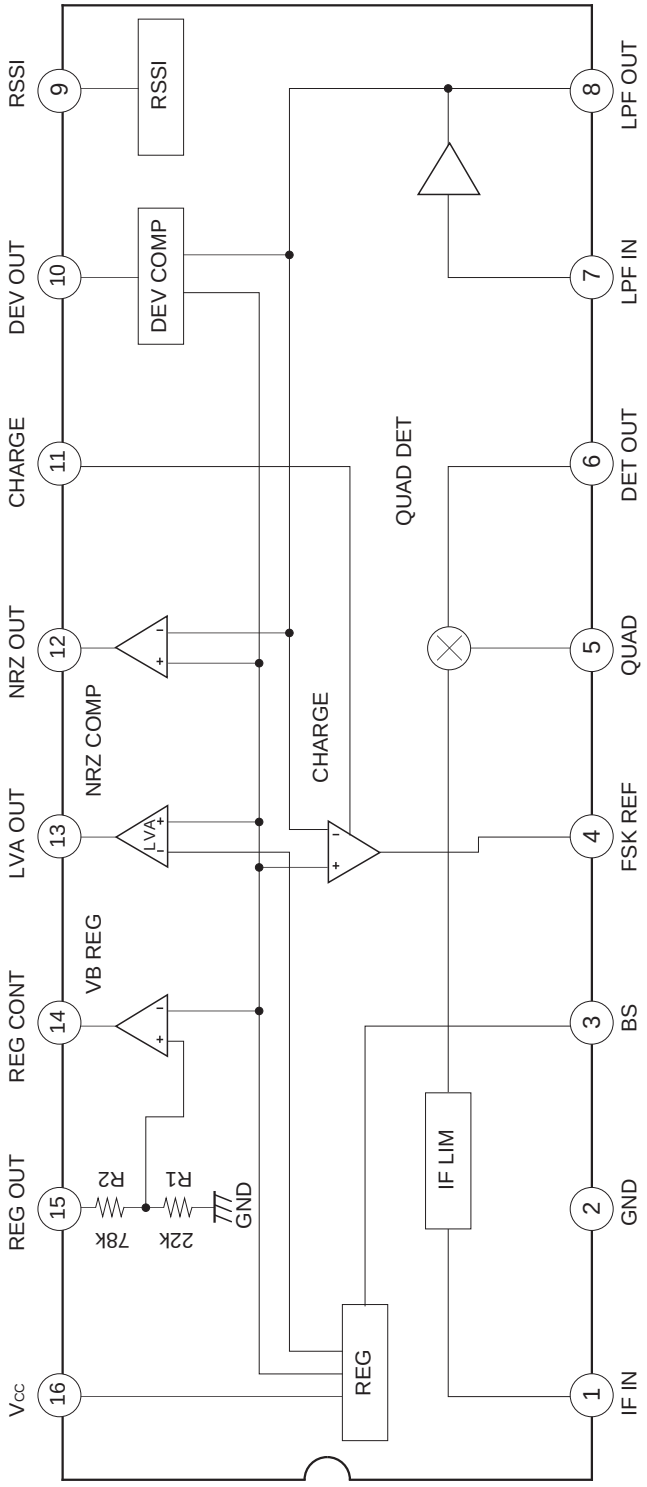
• Supply voltage	V_{CC}	7.0	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	312	mW

Operating Condition

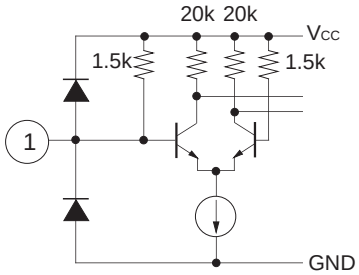
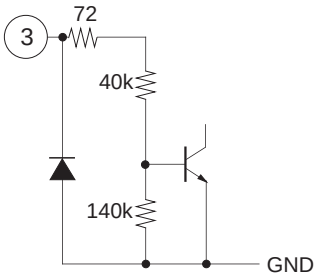
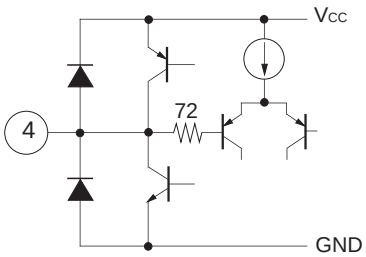
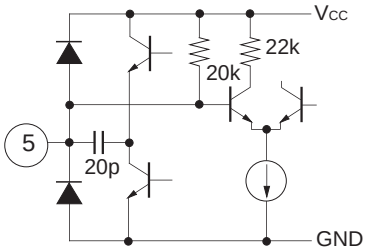
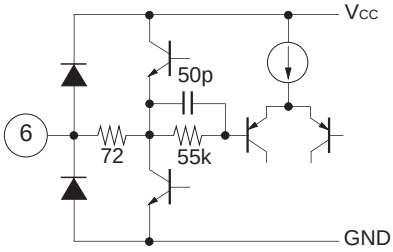
Supply voltage	$V_{CC}1$	1.1 to 4.0	V

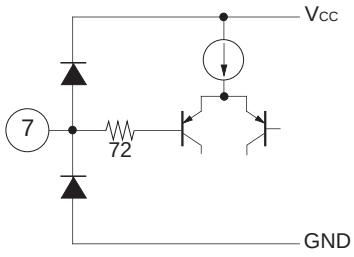
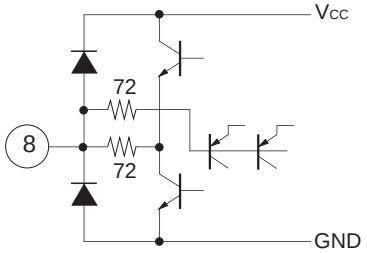
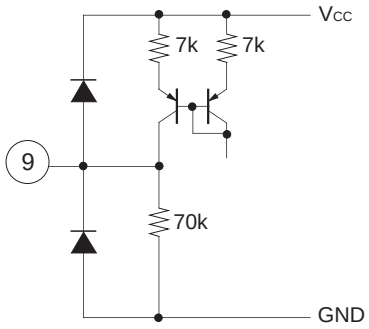
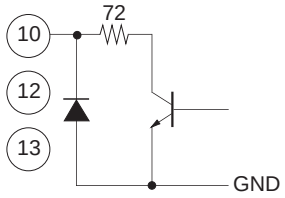
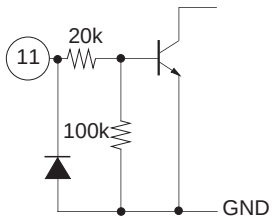
E95Y24A8Z

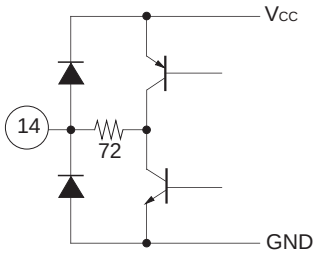
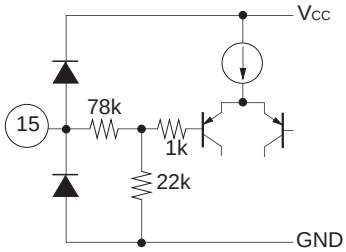
Block Diagram and Pin Configuration



Pin Description

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	IF IN	1.4 V		IF limiter amplifier input.
2	GND	—		Ground.
3	B.S.	—		Controls the battery saving. Setting this pin low suspends the operation of IC. (Applied voltage range: –0.5 V to +7.0 V)
4	FSK REF	0.2 V		Connects the capacitor that determines the low cut-off frequency for the entire system.
5	QUAD	1.4 V		Connects the phase shifter of FM detector circuit.
6	DET OUT	0.2V		FM detector output.

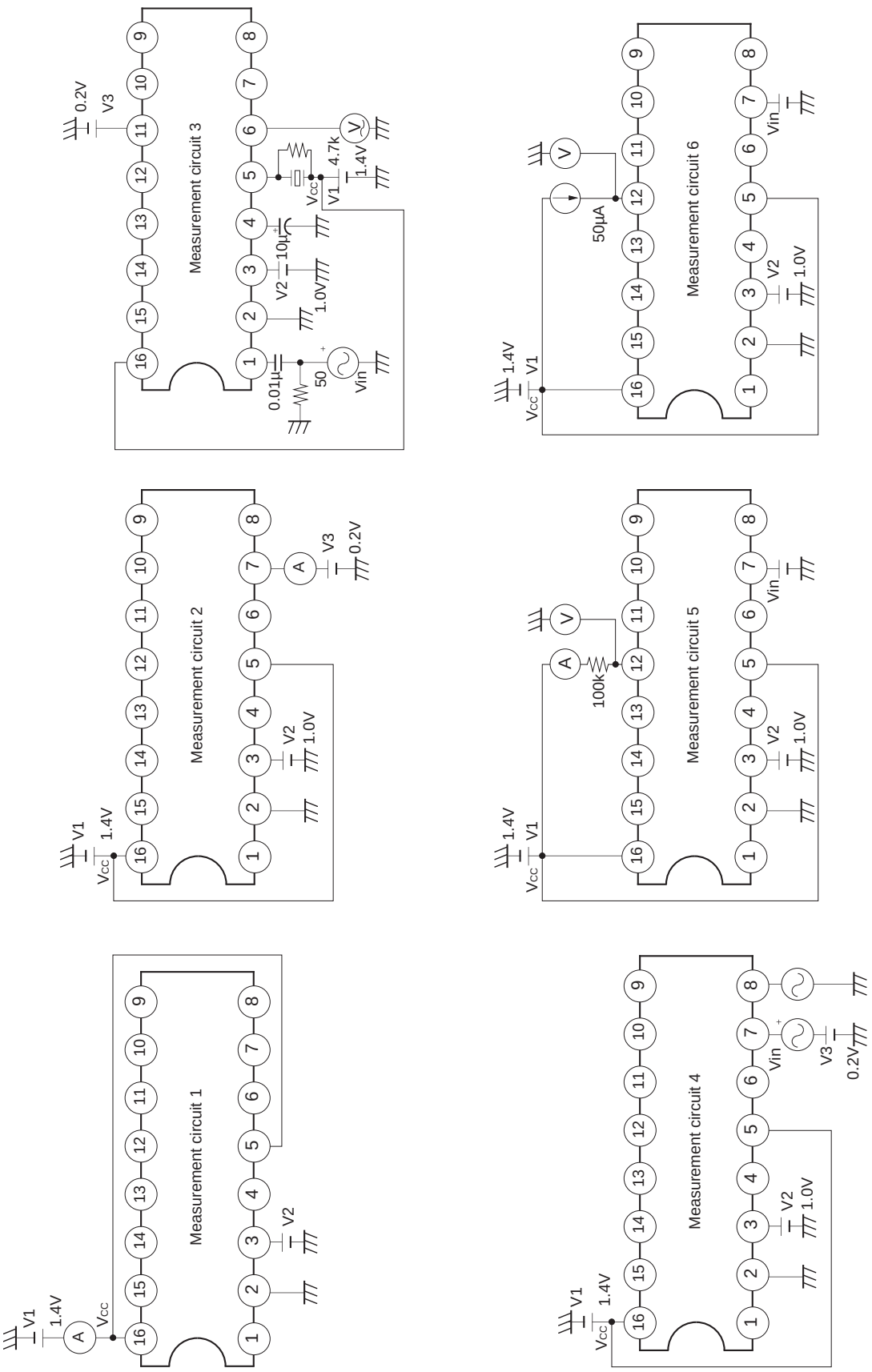
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
7	LPF IN	0.2 V		Operational amplifier input.
8	LPF OUT	0.2 V		Level comparator and NRZ comparator inputs. Output for operational amplifier is connected.
9	RSSI	0 V		RSSI circuit output.
10 12 13	DEV OUT NRZ OUT LVA OUT	— — —		Level comparator, NRZ comparator and LVA comparator outputs. They are open collectors. (Applied voltage range: –0.5 V to +7.0 V)
11	CHARGE	0 V		Controls the ON/OFF operation of the quick-charge circuit. Set this pin high to execute the quick charge. (Applied voltage range: –0.5 V to +7.0 V)

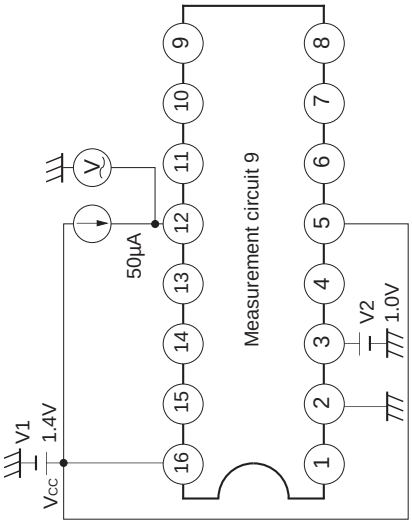
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
14	REG CONT	—		Output for internal constant-voltage source amplifier. Connect the base of PNP transistor. (Current capacity: 100 µA)
15	REG OUT	1.0 V		Constant-voltage source output. Controlled to maintain 1.0 V.
16	Vcc			Power supply.

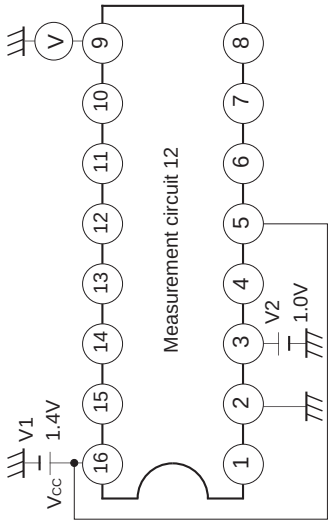
Electrical Characteristics (V_{CC} = 1.4 V, Ta = 25 °C, Fs =455kHz, F_{MOD} = 1.6 kHz, F_{DEV} = 4.8 kHz, AM_{MOD} = 30 %)

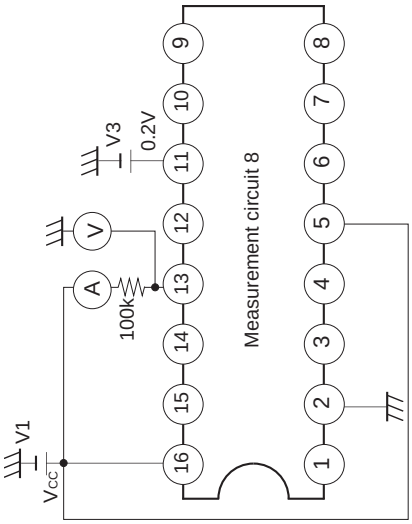
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption	I_{CC}	Measurement circuit 1 V2 = 1.0 V	410	590	800	µA
Current consumption	I_{CCS}	Measurement circuit 1, V2 = 0 V	—	6	20	µA
AM rejection ratio	AMRR	Measurement circuit 3 30k LPF	25	—	—	dB
Op amp. input bias current	I_{BIAS}	Measurement circuit 2	—	—	100	nA
Op amp. maximum output level	V_O	Measurement circuit 4	160	—	—	mVp-p
NRZ output saturation voltage	V_{SATNRZ}	Measurement circuit 6 Vin = 0.3 V	—	—	0.4	V
NRZ output leak current	I_{LNRZ}	Measurement circuit 5 Vin = 0.1 V	—	—	5.0	µA
NRZ hysteresis width	V_{TWNRZ}	Measurement circuit 5 Vin = 0.1 to 0.3 V	—	10	20	mV
VB output current	I_{OUT}	Measurement circuit 7	100	—	—	µA
VB output saturation voltage	V_{SATVB}	Measurement circuit 7	—	—	0.4	V
REG OUT voltage	V_{REG}	Output current 0 µA	0.89	0.96	1.04	V
LVA operating voltage	V_{LVA}	Measurement circuit 8 V1 = 1.4 to 1.0 V	1.00	1.05	1.10	V
LVA output leak current	I_{LLVA}	Measurement circuit 8 V1 = 1.0 V	—	—	5.0	µA
LVA output saturation voltage	V_{SATLVA}	Measurement circuit 9	—	—	0.4	V
Detector output voltage	V_{ODET}	Measurement circuit 3	38	50	68	mVrms
Logic input voltage high level	V_{THBSV}	—	0.9	—	—	V
Logic input voltage low level	V_{TLBSV}	—	—	—	0.35	V
Limiting sensitivity	$V_{IN\ (LIM)}$	Measurement circuit 3	—	17	24	dBµ
Level comparator output saturation voltage	V_{SATLC}	Measurement circuit 11	—	—	0.4	V
Level comparator output leak current	I_{LLC}	Measurement circuit 10	—	—	5.0	µA
RSSI output offset	V_{ORSSI}	Measurement circuit 12	—	135	310	mV
Mixer input resistance	R_{INLIM}	—	1.6	2.0	2.4	kΩ
Mixer output resistance	R_{OUTMIX}	—	1.2	1.5	1.8	kΩ
IF limiter input resistance	R_{INLIM}	—	1.2	1.5	1.8	kΩ

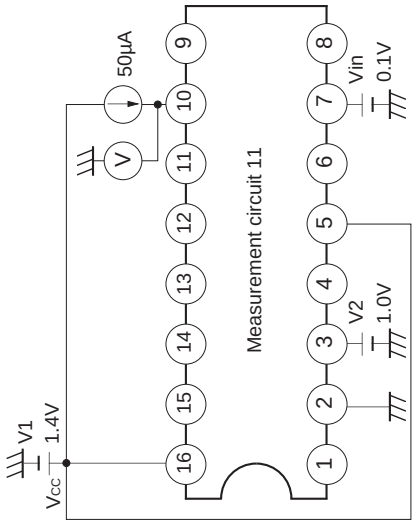
Electrical Characteristics Measurement Circuit

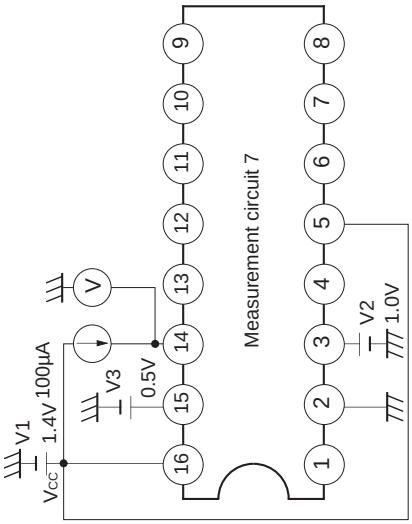


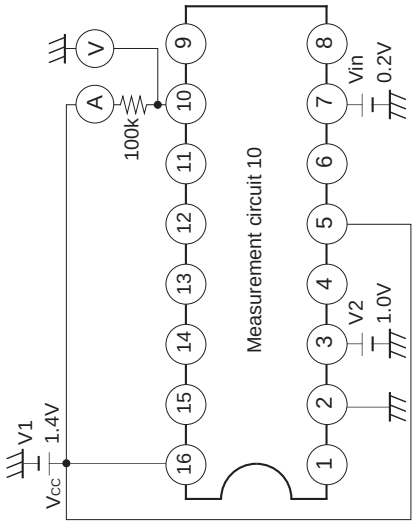

V1
1.4V
Vcc
50μA
V
V2
1.0V
Measurement circuit 9


V1
1.4V
Vcc
V
V2
1.0V
Measurement circuit 12

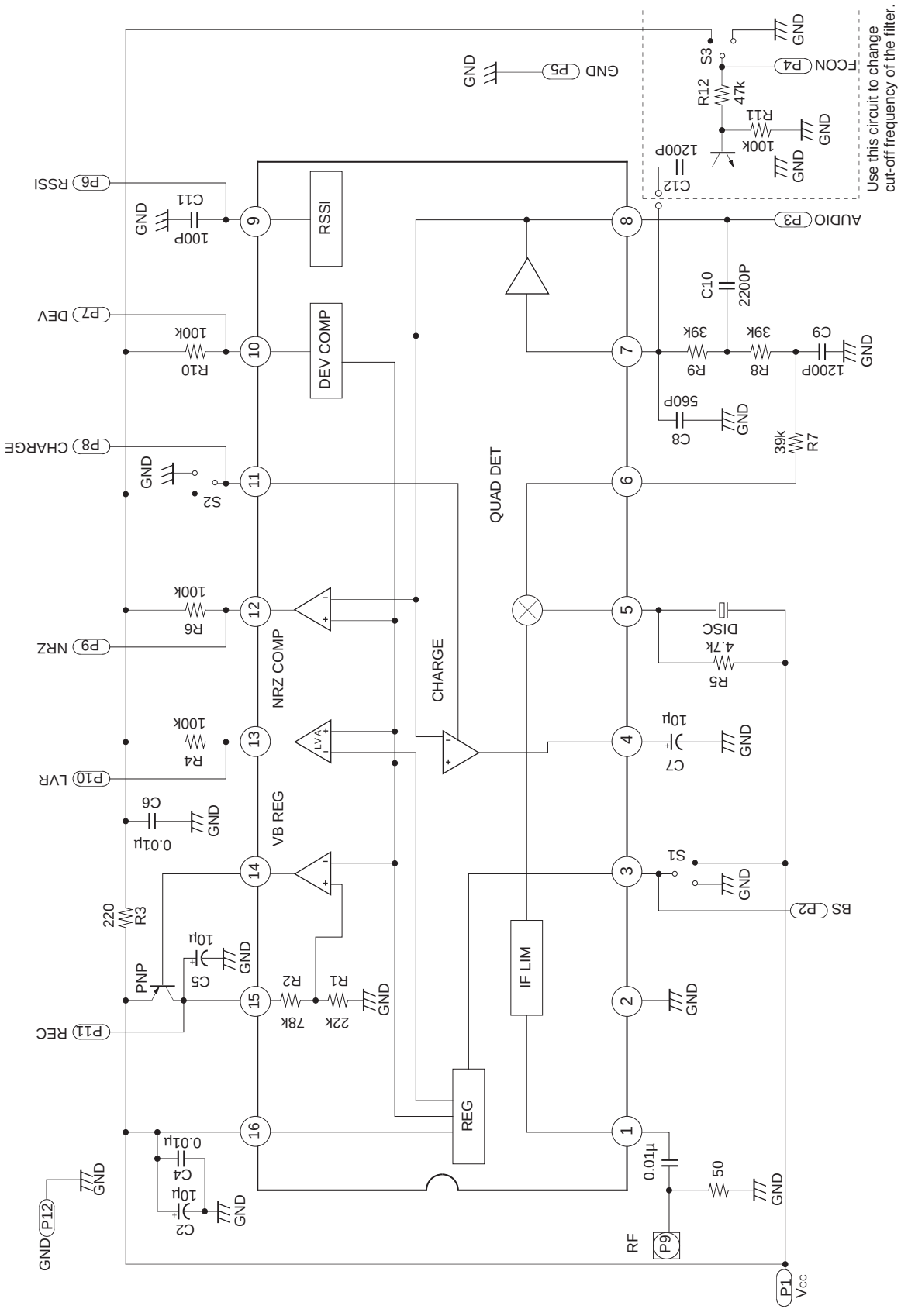

V1
Vcc
A
100k
V
V3
0.2V
V2
1.0V
Measurement circuit 8


V1
1.4V
Vcc
50μA
V
Vin
0.1V
V2
1.0V
Measurement circuit 11


V1
1.4V
Vcc
100μA
V3
0.5V
V
V2
1.0V
Measurement circuit 7


V1
1.4V
Vcc
A
100k
V
Vin
0.2V
V2
1.0V
Measurement circuit 10

Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Application Note

1) Power Supply

The CXA3099N, with built-in regulator, is designed to permit stable operation at wide range of supply voltage from 1.1 to 4.0 V. Decouple the wiring to VCC (Pin 16) as close to the pin as possible.

2) IF Limiter Amplifier

The gain of this IF limiter amplifier is approximately 100 dB. Take notice of the following points in making connection to the IF limiter amplifier input pin (Pin 1).

a) Wiring to the IF limiter amplifier input (Pin 1) should be as short as possible.
b) As the IF limiter amplifier output appears at QUAD (Pin 5), wiring to the ceramic discriminator connected to QUAD should be as short as possible to reduce the interference with the mixer output and IF limiter amplifier input.

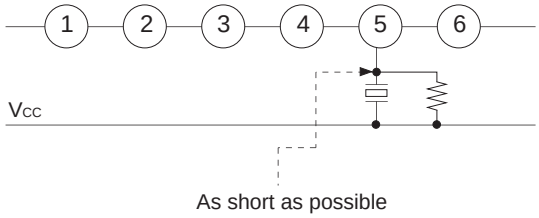


Fig. 2

3) Quick Charge

In order to hasten the rising time from when power is turned on, the CXA3099N features a quick charge circuit. Therefore, the quick charge circuit eliminates the need to insert a capacitor between the detector output and the LPF as is the case with conventional ICs, but capacitor should be connected to Pin 4 to determine the average signal level during steady-state reception. The capacitance value connected to Pin 4 should be chosen such that the voltage does not vary much due to discharge during battery saving.

Connect a signal for controlling the quick charge circuit to Pin 11. Setting this pin high enables the quick charge mode, and setting this pin low enables the steady-state reception mode. Quick charge is used when the power supply is turned on. The battery saving must be set high at the time.

Connect Pin 14 to GND when quick charge is not being used.

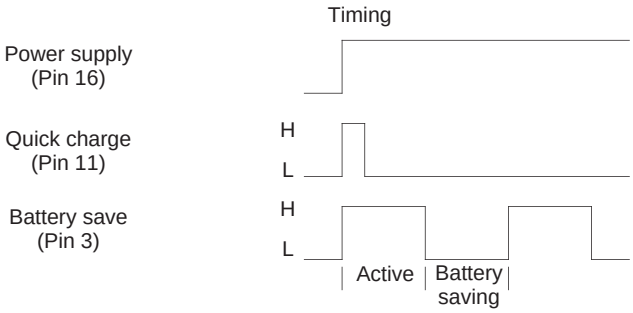


Fig. 3

4) Detector

The detector is of quadrature type. To perform phase shift, connect a ceramic discriminator to Pin 5.
The phase shifting capacitor for the quadrature detector is incorporated. The FM (FSK) signal with the demodulated detector will be output to DET OUT (Pin 6) through the internal primary LPF.
DET OUT output impedance is 200 Ω or less. The DET OUT output is the anti-phase output to NRZ OUT.

The CDBM455C28 (MURATA MFG. CO., LTD.) ceramic discriminator is recommended for the CXA3099N.

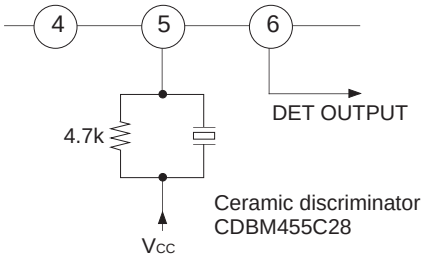


Fig. 4

5) Filter Buffer, Level Comparator and NRZ Comparator

An operational amplifier for LPF is built in this IC.
It is connected internally to the NRZ comparator, level comparator and quick charge circuit.

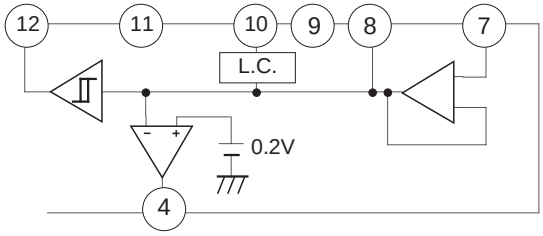


Fig. 5

Using the operational amplifier of Pins 7 and 8 to construct an LPF, remove noise from the demodulated signal and input the signal to the above three circuits.
The level comparator and the NRZ comparator shape waveform of this input signal and output it as a square wave. The comparator output stage is for open collector.
Thus, if the CPU is of CMOS type and the supply voltage is different, a direct interface as illustrated in the figure below can be implemented.

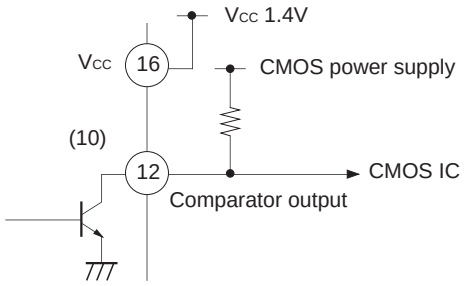


Fig. 6

6) REG CONT

Controls the base bias of the external transistors.

7) LVA OUT

This pin goes high (open) when the supply voltage becomes low. Since the output is an open collector, it can be used to directly drive CMOS device. The setting voltage of the LVA is 1.05 V (typ.), and it possesses a hysteresis with respect to the supply voltage. The hysteresis width is 50 mV (typ.).

8) B.S.

Operation of the CXA3099N can be halted by setting this pin low. This pin can be connected directly to CMOS device. The current consumption for battery saving is 20 µA or less (at 1.4 V).

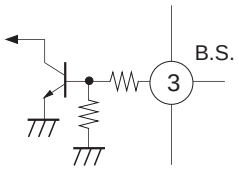
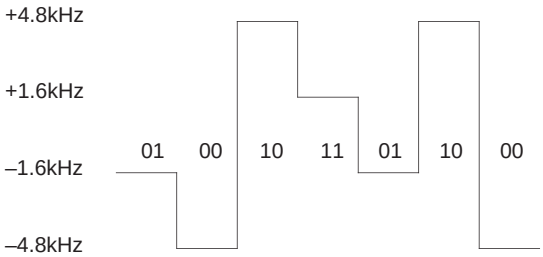


Fig. 7

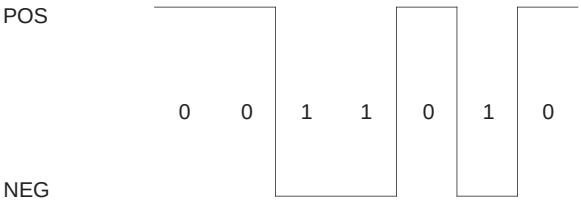
9) M-ary (M = 2- or 4-level) FSK Demodulation System

Polarity discrimination output and MSB comparator output are used to demodulate the 4-level waveform shown below.

[4-level FSK demodulating waveform]

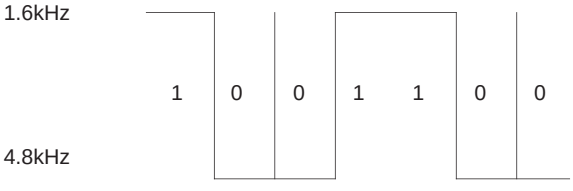


[NRZ OUT] Polarity discrimination output (When the input frequency is higher than the local frequency)



The polarity can be inverted by setting the local frequency higher than the input frequency.

[L.C. OUT] MSB comparator output



The 4-level FSK demodulating data is divided into an NRZ OUT and L.C. OUT shown above. Here, the NRZ OUT corresponds to a conventional NRZ comparator output. The L.C. OUT is made comparing the demodulated waveform amplitude to the IC internal reference voltage levels. When the threshold value of L.C. OUT is not appropriate to the detector output, the resistance value on Pin 5 should be adjusted for the detector output level adjustment.

For the 2-level FSK demodulation, it corresponds to a conventional NRZ comparator output.

10) Principle of Quick Charge Operation

BUF in Fig. 8 is the detector buffer amplifier, and AMP is an operational amplifier to construct an LPF. COMP is the level comparator or the NRZ comparator. The CXA3099N has a feedback loop from the comparator input to the input circuit of the detector output buffer. This equalizes the average value of the comparator input voltage to the reference voltage, with the quick charge circuit of CHG being set in the feedback loop. Switching the current of the quick charge circuit enables reduction of the rise time.

In this block, CHG is a comparator which compares input voltages and outputs a current based on this comparison. The current on CHG is switched between high and low at Pin 11. When the power is turned on, switch the current to high to increase the charge current at C in Fig. 8 and shorten the time constant. During steady-state reception mode, switch the current to low, lengthening the charge time constant and allowing for stable data retrieval.

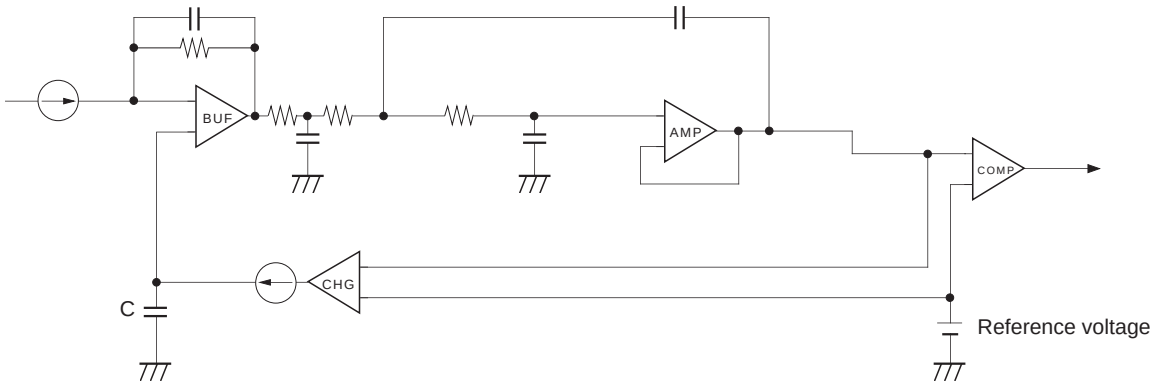


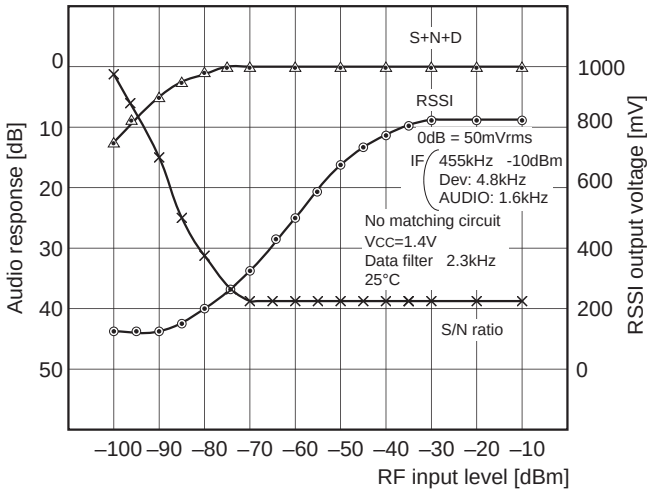
Fig. 8

11) S Curve Characteristics

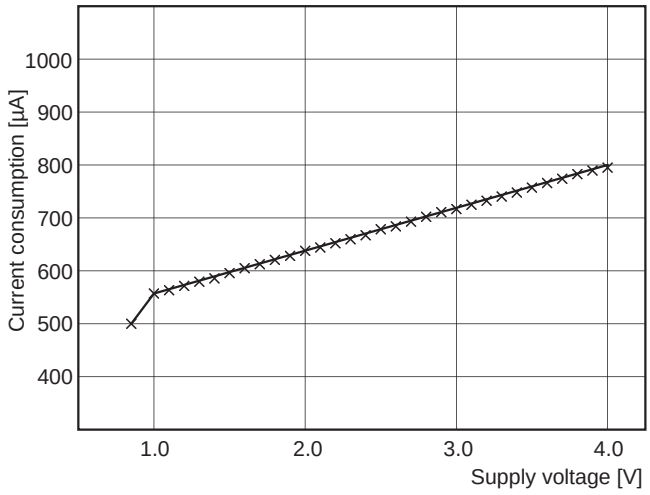
Even if the IF IN input signal frequency is deviated, the feedback is applied to the DET OUT operating point so as to match it to the comparator reference voltage by the quick charge operation shown in Fig. 8. Therefore, this feedback must be halted in order to evaluate the S curve characteristics.

To execute the evaluation, measure the average voltage on Pin 8 first and input this voltage to Pin 4 from the external power supply.

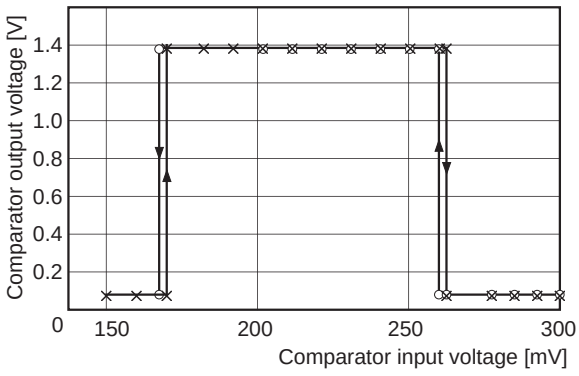
Example of Representative Characteristics



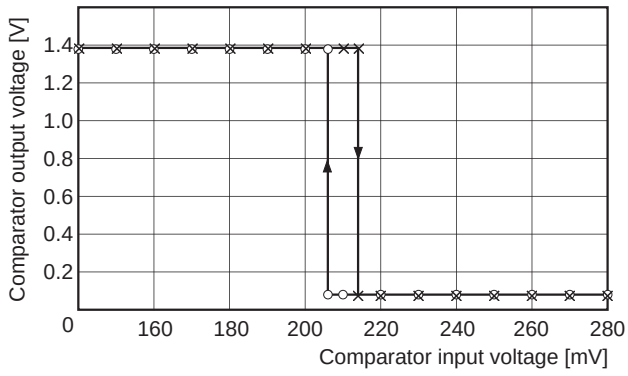
Audio response and RSSI output voltage characteristics



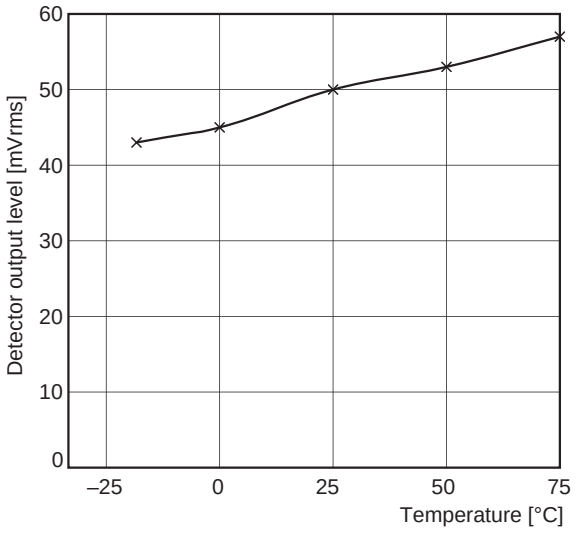
Supply voltage vs. Current consumption



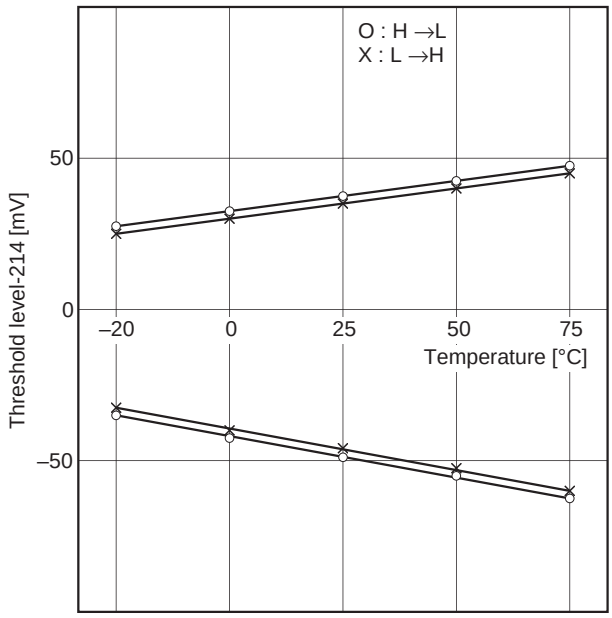
Deviation comparator characteristics



NRZ comparator characteristics



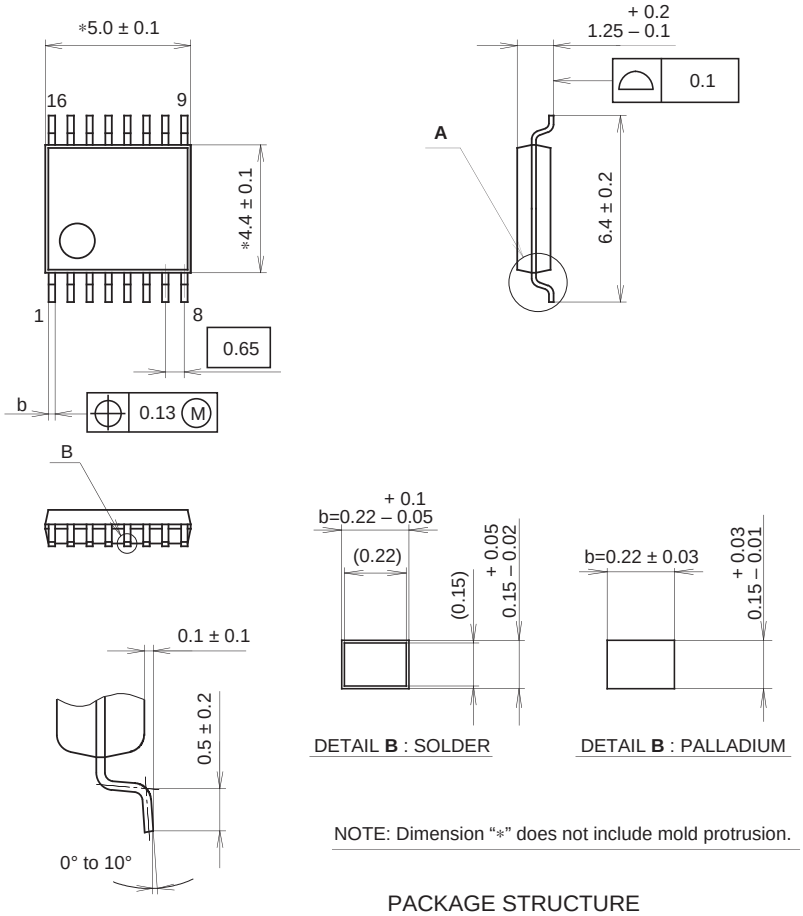
Detector output level temperature characteristics



Level comparator temperature vs.Threshold level

Package Outline Unit : mm

16PIN SSOP (PLASTIC)



DETAIL **B** : SOLDER

DETAIL **B** : PALLADIUM

DETAIL **A**

NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	SSOP-16P-L01
EIAJ CODE	SSOP016-P-0044
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.1g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).