SONY

CXA3272R

Driver/Timing Generator for Color LCD Panels

Description

The CXA3272R is an IC designed to drive the color LCD panels LCX032 and LCX033.

This IC greatly reduces the number of peripheral circuits and parts by incorporating an RGB driver and timing generator for video signals onto a single chip. This chip has a built-in serial interface circuit and electronic attenuators which allow various settings to be performed by microcomputer control, etc.

Features

- Color LCD panels LCX032 and LCX033 driver
- Supports NTSC and PAL systems
- Supports 16:9 wide display (letter box and pulse elimination display)
- Supports Y/color difference inputs and RGB inputs
- Supports OSD input
- Serial interface circuit
- Electronic attenuators (D/A converter)
- VCO (can be switched with an external oscillator circuit)
- LPF
- Common voltage output circuit
- Sharpness function (during Y/color difference input)
- 2-point γ correction circuit
- R, G, B signal delay time adjustment circuit
- Output polarity inversion circuit
- Supports AC drive for LCD panel during no signal

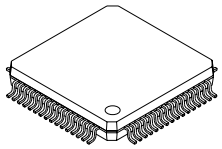
Applications

Color LCD viewfinder

Structure

Bi-CMOS IC

64 pin LQFP (Plastic)



Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	$V_{CC}1$	6	V
	$V_{CC}2$	14	V
	$V_{DD}0, 1, 2$	4.5	V
• Analog input pin voltage			
	VINA	–0.3 to $V_{CC}1$	V
• Digital input pin voltage			
VIND (other than Pins 9, 10 and 11)			
		–0.3 to V_{DD} + 0.3	V
VIND (Pins 9, 10 and 11)		–0.3 to +4.5	V
• Operating temperature	Topr	–15 to +75	°C
• Storage temperature	Tstg	–40 to +125	°C
• Allowable power dissipation*1			
	P_D (Ta ≤ +75°C)	350	mW

Operating Conditions

• Supply voltage	$V_{CC}1$ – GND1	2.7 to 3.6	V
	$V_{CC}2$ – GND2	11.0 to 13.5	V
	$V_{DD}0, 1, 2$ – V_{SS}	2.7 to 3.6	V
• Input conditions			
RGB input signal voltage (Pins 59, 60 and 61)*2			
	VRGB	0 to 0.7 (0.5 typ.)	V
Y input signal voltage (Pin 60)*3			
	VY	0 to 0.5 (0.35 typ.)	V
R-Y input signal voltage (Pin 59)*3			
	VR-Y	0 to 0.49 (0.245 typ.)	V
B-Y input signal voltage (Pin 61)*3			
	VB-Y	0 to 0.622 (0.311 typ.)	V

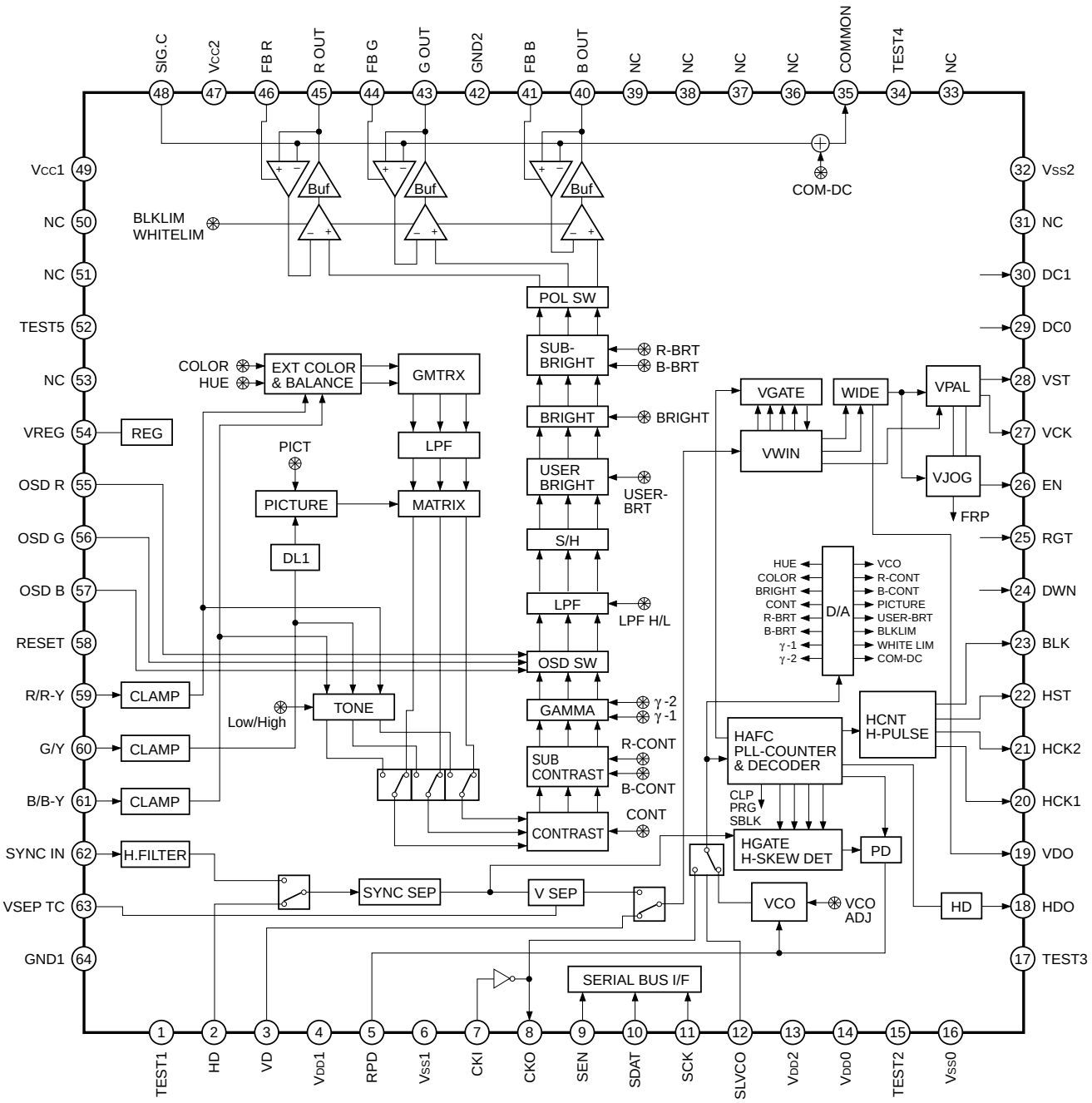
*1 With substrate Size: 30 × 30 × 1.6mm
Material: Glass fabric base epoxy

*2 During RGB input

*3 During Y/color difference input

E01Y30-PS

Block Diagram



Pin Description

Pin No.	Symbol	I/O	Description
1	TEST1	O	Test 1 (Leave open.)
2	HD	I	External sync signal input (HD or CSYNC)*1
3	VD	I	External sync signal input (VD)*1
4	$V_{DD}1$	—	Digital 3V power supply for oscillation cell
5	RPD	O	Phase comparator output
6	$V_{SS}1$	—	Digital 3V GND for oscillation cell
7	CKI	I	Oscillation cell input
8	CKO	O	Oscillation cell output
9	SEN	I	Serial bus load input
10	SDAT	I	Serial bus data input
11	SCK	I	Serial bus clock input
12	SLVCO	I	Internal VCO/external VCO system switching (GND = internal, $V_{CC}1$ = external)
13	$V_{DD}2$	—	Digital 3V power supply
14	$V_{DD}0$	—	Digital 3V output power supply
15	TEST2	I	Test 2 (Leave open or connect to GND.)
16	$V_{SS}0$	—	Digital 3V output GND
17	TEST3	O	Test 3 (Leave open.)
18	HDO	O	HD pulse output
19	VDO	O	VD pulse output
20	HCK1	O	H clock pulse 1 output
21	HCK2	O	H clock pulse 2 output
22	HST	O	H start pulse output
23	BLK	O	BLK pulse output
24	DWN	O	Up/down inverted display switching
25	RGT	O	Right/left inverted display switching
26	EN	O	EN pulse output
27	VCK	O	V clock pulse output
28	VST	O	V start pulse output
29	DC0 (STB)	O	DC0 output (L/H) (for STB)
30	DC1	O	DC1 output (L/H)
31	NC	—	NC
32	$V_{SS}2$	—	Digital 3V GND
33	NC	—	NC
34	TEST4	O	Test 4 (Leave open.)
35	COMMON	O	COM output
36	NC	—	NC
37	NC	—	NC

Pin No.	Symbol	I/O	Description
38	NC	—	NC
39	NC	—	NC
40	B OUT	O	B signal output
41	FB B	O	Time constant for B signal DC voltage feedback*2
42	GND2	—	Analog 12V GND
43	G OUT	O	G signal output
44	FB G	O	Time constant for G signal DC voltage feedback*2
45	R OUT	O	R signal output
46	FB R	O	Time constant for R signal DC voltage feedback*2
47	$V_{CC}2$	—	Analog 12V power supply
48	SIG.C	I	R, G and B output DC voltage adjustment
49	$V_{CC}1$	—	Analog 3V power supply
50	NC	—	NC
51	NC	—	NC
52	TEST5	O	Test 5 (Leave open or connect to 3V ($V_{CC}1$ or V_{DD}).)
53	NC	—	NC
54	VREG	—	Reference power supply
55	OSD R	I	External digital R input (common with test)*3
56	OSD G	I	External digital G input (common with test)*3
57	OSD B	I	External digital B input (common with test)*3
58	RESET	I	System reset*4
59	R/R-Y	I	R/R-Y signal input
60	G/Y	I	G/Y signal input
61	B/B-Y	I	B/B-Y signal input
62	SYNC IN	I	Sync signal input (composite)*5
63	VSEP TC	O	Time constant for vertical sync separation
64	GND1	—	Analog 3V GND

*1 HD (CSYNC)/VD signal is input during 3Vp-p separate SYNC and CSYNC input.

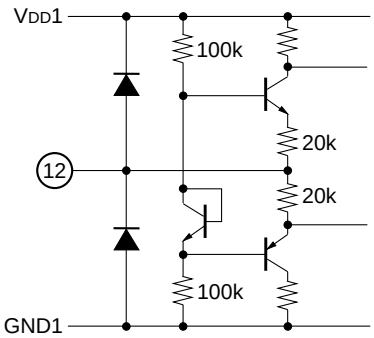
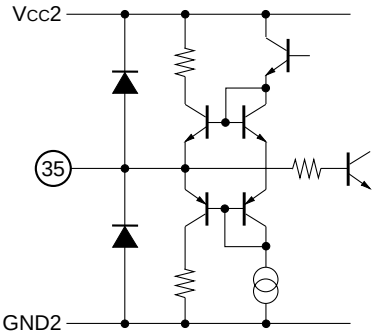
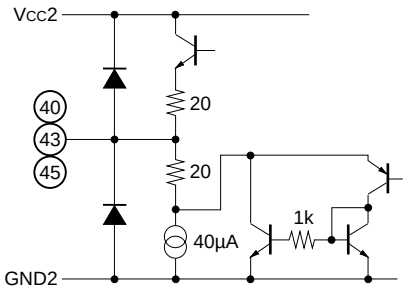
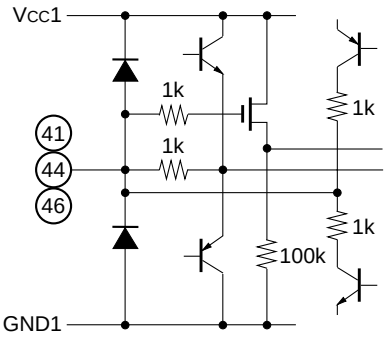
*2 Feedback circuit smoothing capacitor connection for R, G and B output DC level control. Low leakage capacitor is used because of high impedance.

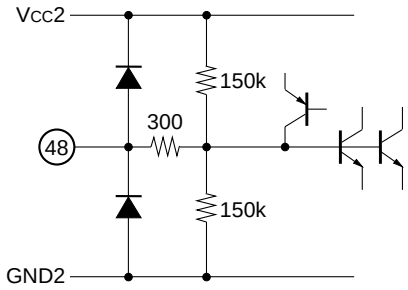
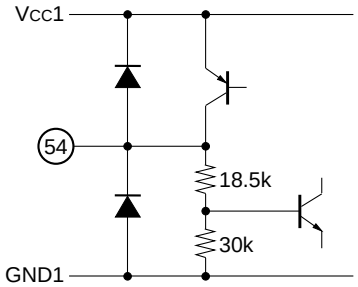
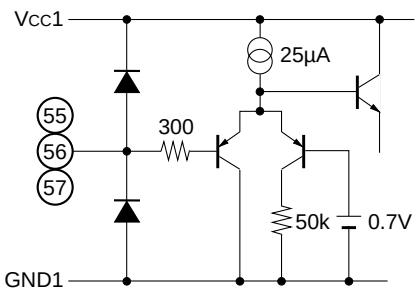
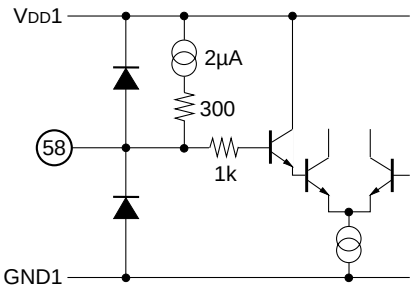
*3 External digital signal input. There are two threshold values Vth1 and Vth2. One of R, G and B exceeds Vth1, all RGB are black levels; exceeding Vth2, white level. Connect to GND during unused.

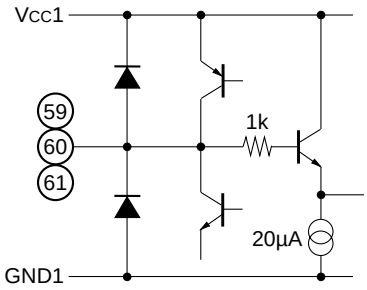
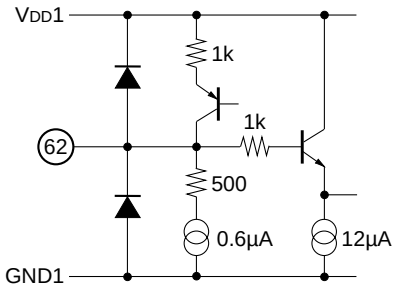
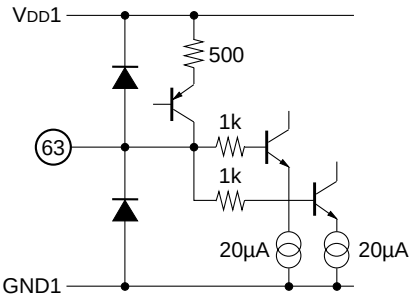
*4 TG block system reset. By connecting to GND, this pin is system reset. Capacitance is connected between this pin and GND, and used.

*5 SYNC input. Video signal with SYNC is input.

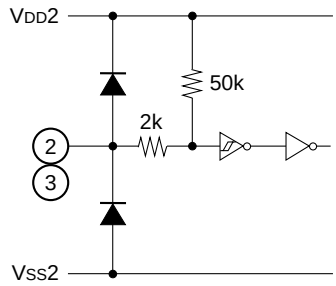
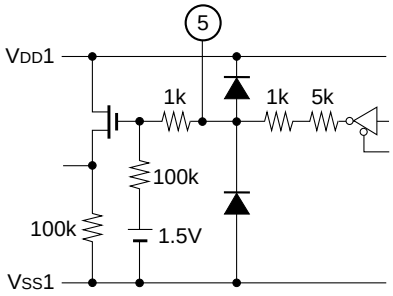
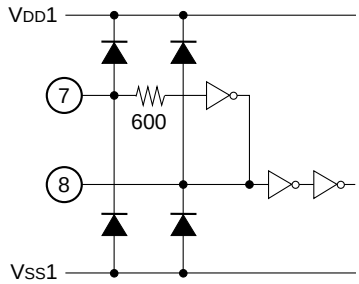
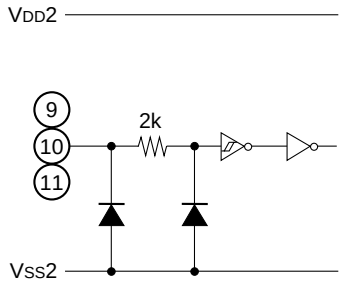
Analog Block Pin Description

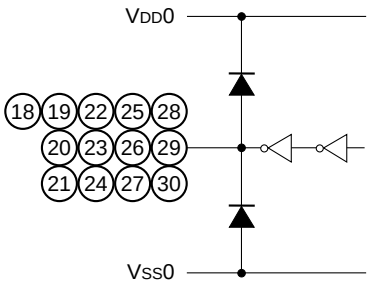
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
12	SLVCO	—		VCO internal/external switching. Connect to the GND potential when using the internal VCO, or to VDD1 when using an external VCO.
35	COMMON	Vcc2/2		Common voltage output.
40 43 45	B OUT G OUT R OUT	Vcc2/2		RGB primary color signal outputs.
41 44 46	FB B FB G FB R	1.5V		Smoothing capacitor connection for the feedback circuit of RGB output DC level control. Use a low-leakage capacitor because of high impedance.
42	GND2	0V		Vcc 12V GND.
47	Vcc2	12V		Vcc 12V power supply.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
48	SIG.C	$V_{CC}2/2$		R, G and B output DC voltage setting. Connect a 0.01µF capacitor between this pin and GND2. When used with a signal output DC voltage of other than $V_{CC}2/2$, apply voltage of 5.2 to 6.5V from an external source.
49	$V_{CC}1$	3.0V		Analog 3V power supply.
54	VREG	2.0V		Regulator output. Connect an external capacitor of 1µF or more.
55 56 57	OSD R OSD G OSD B	—		External digital signal inputs. There are two threshold values: Vth1 (approximately 1.0V) and Vth2 (approximately 2.0V). When one of the RGB signals exceeds Vth1, all of the RGB outputs go to black level; when an input exceeds Vth2, only the corresponding output goes to white level. Connect these pins to GND when not used.
58	RESET	—		TG block system reset. The system is reset by connecting this pin to GND. Normally connect a capacitor between this pin and GND. (Threshold value = 2.0V)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
59 60 61	R/R-Y G/Y B/B-Y	RGB: 1.2V Y/color difference: 1.6V		In RGB input mode, input the R signal to Pin 59, the G signal to Pin 60 and the B signal to Pin 61. In Y/color difference input mode, input the R-Y signal to Pin 59, the Y signal to Pin 60 and the B-Y signal to Pin 61. Pedestal clamp these pins with external coupling capacitors.
62	SYNC IN	1.6V		Sync separation input. Input a video signal with sync through an external capacitor. Leave this pin open during external HD and VD inputs. Connect to VDD during external CSYNC input.
63	VSEP TC	1.7V		Time constant connection for vertical sync separation.
64	GND1	—		Analog 3V GND.

Digital Block Pin Description

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
2 3	HD VD	—		External HD and external VD inputs. When inputting an external CSYNC, input to HD and connect VD to GND. Set to external sync signal input with the serial bus. Connect to GND other than during external sync signal input.
4	VDD1	—		Power supply for VCO.
5	RPD	—		Phase comparator output.
6	VSS1	0V		GND for VCO.
7 8	CKI CKO	—		Inverter I/O for external VCO. When using the internal VCO, fix CKI to the GND potential and leave CKO open.
9 10 11	SEN SDAT SCK	—		Serial bus inputs. Voltage up to 4.5V can be input regardless of the VDD2 supply voltage.
13	VDD2	—		Power supply for digital block.
14	VDD0	—		Power supply for digital output block.
16	VSS0	—		GND for digital output block.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
18 19 20 21 22 23 24 25 26 27 28 29 30	HDO VDO HCK1 HCK2 HST BLK DWN RGT EN VCK VST DC0 DC1	—		Digital block outputs.
32	VSS2	0V		GND for digital block.

Test Pin Description

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1 17 34	TEST1 TEST3 TEST4	—		Test. Leave open.
15	TEST2	—		Test. Leave open or connect to GND.
52	TEST5	—		Test. Leave open or connect to 3V block (VCC1 or VDD).

Setting Conditions for Measuring Electrical Characteristics

The following setting is required while measuring electrical characteristics.

Setting 1. System reset

After turning on the power, set SW58 to ON and start up V58 from GND in order to activate the MOS block system reset. (See Fig. 1-1.)
The serial bus is set to the default values.

Setting 2. Horizontal AFC adjustment

- When using the internal VCO
  Input SIG4 (VL = 0mV) to (A) and adjust serial bus register VCO so that the TP5 phase comparison output waveform is flat. (See Fig. 1-2.)
- When using the external VCO
  Input SIG4 (VL = 0mV) to (A) and adjust VR1 so that WL = WH in the TP5 phase comparison output waveform. (See Fig. 1-3.)

Note) VCO internal/external switching is performed by Pin 12 (SLVCO).
When using the internal VCO, connect Pin 12 to GND and set SW5 and SW7 in the Electrical Characteristics Measurement Circuit to B.
When using an external VCO, connect Pin 12 to V_{DD} and set SW5 and SW7 in the Electrical Characteristics Measurement Circuit to A.

Note) When measuring a band of 2MHz or more such as Y signal frequency response or sharpness characteristics among the items being measured, the measurement must be made with the sample-and-hold circuit set to through by the serial bus.

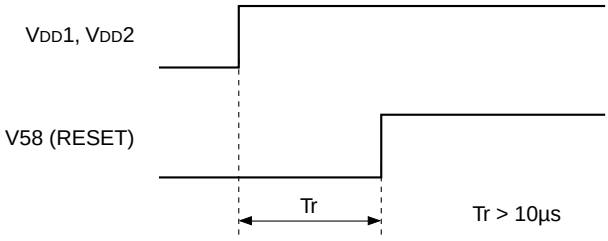


Fig. 1-1. System reset

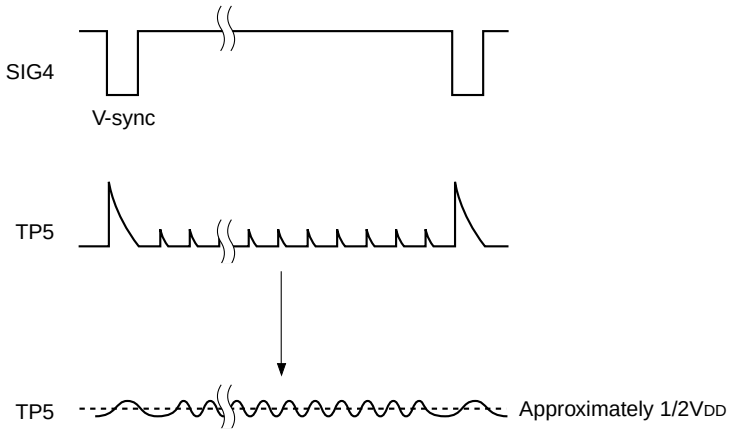


Fig. 1-2. Horizontal AFC adjustment (when using the internal VCO)

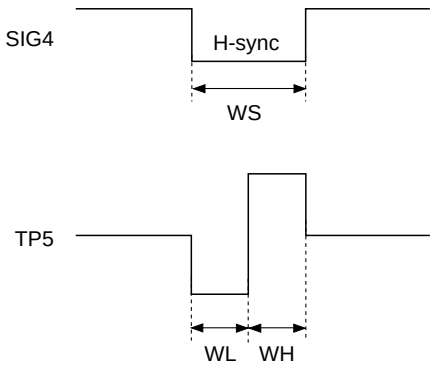


Fig. 1-3. Horizontal AFC adjustment (when using an external VCO)

Setting 3. Serial data initial setting (—: don't care)

The serial data other than conditions of each item during electrical characteristics measurement are set to the following serial data initial setting.

MSB Address LSB								MSB Data LSB							
A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	Unused (00000000)							
0	0	0	0	0	0	0	1	SLSH2 (1)	SLSH1 (1)	SLSH0 (1)	SLSYNC1 (0)	SLSYNC0 (0)	ASPECT (0)	SYSTEM (0)	INPUT (0)
0	0	0	0	0	0	1	0	VDO POL (0)	HDO POL (0)	SLCLP (0)	SYNC POL (0)	Unused (0)	Unused (0)	LCD1 (0)	LCD0 (0)
0	0	0	0	0	0	1	1	TEST2 (0)	TEST1 (0)	Unused (0)	MBK (0)	FRP1 (0)	FRP0 (0)	SLRGT (0)	SLDWN (0)
0	0	0	0	0	1	0	0	TEST4 (0)	Unused (0)	Unused (0)	Unused (0)	TEST3 (0)	SLDC1 (0)	SLDC0 (1)	SYNC GEN (0)
0	0	0	0	0	1	0	1	—	—	—	H-POSITION (10000)				
0	0	0	0	0	1	1	0	—	—	—	—	—	V-POSITION (011)		
0	0	0	0	0	1	1	1	—	—	—	HD-POSITION (00000)				
0	0	0	0	1	0	0	0	—	—	—	—	—	—		
0	0	0	0	1	0	0	1	—	—	—	TEST5 (10000)				
0	0	0	0	1	0	1	0	—	—	Unused (0)	Unused (0)	TEST7 (0)	TEST6 (0)	LPF (0)	TONE (0)
1	1	0	0	0	0	0	0	HUE (10000000)							
1	1	0	0	0	0	0	1	COLOR (10000000)							
1	1	0	0	0	0	1	0	BRIGHT (10000000)							
1	1	0	0	0	0	1	1	CONTRAST (10000000)							
1	1	0	0	0	1	0	0	R-BRIGHT (10000000)							
1	1	0	0	0	1	0	1	B-BRIGHT (10000000)							
1	1	0	0	0	1	1	0	γ-1 (00000000)							
1	1	0	0	0	1	1	1	γ-2 (00000000)							
1	1	0	0	1	0	0	0	Unused (10000000)							
1	1	0	0	1	0	0	1	R-CONTRAST (10000000)							
1	1	0	0	1	0	1	0	B-CONTRAST (10000000)							
1	1	0	0	1	0	1	1	BLACK-LIM (10000000)							
1	1	0	0	1	1	0	0	PICTURE (10000000)							
1	1	0	0	1	1	0	1	USER-BRIGHT (10000000)							
1	1	0	0	1	1	1	0	VCO (10000000)							
1	1	0	0	1	1	1	1	—	—	COMMON (101010)					
1	1	0	1	0	0	0	0	—	—	—	—	—	Unused (000)		
1	1	0	1	0	0	0	1	—	—	—	—	—	—	WHITE-LIM (11)	
1	1	1	0	1	0	1	0	TEST8							

Electrical Characteristics — DC Characteristics

Unless otherwise specified, Settings 1 and 2 are required.
$V_{CC}1$ = 3.0V, $V_{CC}2$ = 12.0V, GND1 = GND2 = 0V, $V_{DD}0$ = $V_{DD}1$ = $V_{DD}2$ = 3.0V, $V_{SS}0$ = $V_{SS}1$ = $V_{SS}2$ = 0V,
Ta = 25°C
S/H = 1

Item	Symbol	Measurement conditions		Min.	Typ.	Max.	Unit
Current characteristics							
Current consumption Vcc1 Analog low block	$I_{CC}11$	Input SIG4 (VL = 0mV) to (A). Measure the Icc1 current value.	Y/color difference input	16	21	28	mA
	$I_{CC}12$		RGB input	14	19	25	mA
Current consumption Vcc2 Analog high block	$I_{CC}2$	Input SIG4 (VL = 0mV) to (A). Measure the Icc2 current value.		3	4	5.5	mA
Current consumption V_{DD} Logic block	$I_{DD}1$	Input SIG4 (VL = 0mV) to (A). Measure the $I_{DD}11$ and $I_{DD}21$ current values. $I_{DD}1$ and $I_{DD}2$ = $I_{DD}11$ + $I_{DD}21$	113K pixels	7	10	13	mA
	$I_{DD}2$		180K pixels	8	11	14	mA
Digital block I/O characteristics							
Low level input voltage	VIL	Digital block input pins*1				0.3V_{DD}	V
High level input voltage	VIH	Digital block input pins*1		0.7V_{DD}			V
High level output voltage	VOH1	V_{DD} = 3.0V, IOH = –1.2mA*2		2.8			V
	VOH2	V_{DD} = 2.7V, IOH = –1.2mA*2		2.6			V
Low level output voltage	VOL1	IOL = 1.2mA*2				0.3	V
CKO pin high level output voltage	VOH2	IOH = –3mA		0.5V_{DD}			V
CKO pin low level output voltage	VOL2	IOL = 3mA				0.5V_{DD}	V
RPD pin high level output voltage	VOH3	IOH = –0.5mA, external VCO mode		V_{DD} – 1.2			V
RPD pin low level output voltage	VOL3	IOL = 0.7mA, external VCO mode				1	V
RPD pin output off leak current	IOFF	High impedance state, VOUT = V_{SS} or V_{DD}		–40		40	µA
Output transition time	tTLH	Load: 40pF (See Fig.2.)				30	ns
	tTHL					30	ns
Cross-point time difference	dT	Load: 40pF Measure the HCK1/HCK2. (See Fig. 3.)				10	ns
HCK duty ratio	DTYHC	Load: 40pF Measure the HCK1/HCK2 duty ratio.		47	50	53	%

*1 Digital block input pins: HD, VD, SEN, SDAT, SCK

*2 Digital block output pins (Pins 17 to 30)

Electrical Characteristics — AC Characteristics

Unless otherwise specified, Settings 1 and 2 are required.
$V_{CC}1$ = 3.0V, $V_{CC}2$ = 12.0V, GND1 = GND2 = 0V, $V_{DD}0$ = $V_{DD}1$ = $V_{DD}2$ = 3.0V, $V_{SS}0$ = $V_{SS}1$ = $V_{SS}2$ = 0V,
Ta = 25°C
Measure the non-inverted outputs for TP40, TP43 and TP45.

Item	Symbol	Serial data settings	Measurement conditions		Min.	Typ.	Max.	Unit
Luminance signal block								
Typical gain between input and output	GYTP	CONT 128 INPUT 1	SW59, SW60 and SW61 = B Input SIG3 to (A) and measure the ratio between the output amplitude (white-black) and input amplitude at TP43.	Y/color difference input	14	16	18	dB
	GRGBTP	CONT 128 INPUT 0		RGB input	11	13	15	dB
Minimum gain between input and output	GYMN	CONT 0 INPUT 1	SW59, SW60 and SW61 = B Input SIG3 to (A) and measure the ratio between the output amplitude (white-black) and input amplitude at TP43.	Y/color difference input	–2	1	4.5	dB
	GRGBMN	CONT 0 INPUT 0		RGB input	–5	–2	1.5	dB
Maximum gain between input and output	GYMX	CONT 255 INPUT 1	SW59, SW60 and SW61 = B Input SIG3 to (A) and measure the ratio between the output amplitude (white-black) and input amplitude at TP43.	Y/color difference input	19	21	23	dB
	GRGBMX	CONT 255 INPUT 0		RGB input	16	18	20	dB
Y input frequency response	FCY	INPUT 1 LCD1/0 0/0 PICT 80 LPF 1	SW59 and SW61 = A, SW60 = B, SW40, SW43 and SW45 = ON Assume the output amplitude at TP43 when SIG6 (100kHz) is input to (A) as 0dB. Vary the frequency of the input signal to obtain the frequency with an output amplitude of –3dB. S/H OFF, color difference input, CL = 100pF		5.5			MHz
Picture quality adjustment variable amount 1 180K pixels	GSHP1X	INPUT 1 LPF 1	SW59 and SW61 = A, SW60 = B Assume the output amplitude at TP43 when SIG6 (100kHz) is input to (A) as 0dB. Obtain the amount by which the output amplitude changes when serial bus register PICTURE is set to 255 and 0 with SIG6 (2.5MHz or 1.8MHz) as the input. S/H OFF, color difference input	2.5MHz max. (PIC = 255)	11	14		dB
	GSHP1N			2.5MHz min. (PIC = 0)		–3	0	dB
Picture quality adjustment variable amount 2 113K pixels	GSHP2X	INPUT 1 LPF 0		1.8MHz max. (PIC = 255)	11	14		dB
	GSHP2N			1.8MHz min. (PIC = 0)		–1	2	dB
I/O delay time	TDYYC	INPUT 1	Y/color difference input: SW59 and SW61 = A, SW60 = B RGB input: SW59, SW60 and SW61 = B Input SIG8 to (A). Measure the delay time from the 2T pulse peak of the input signal to the 2T pulse peak of the non-inverted output at TP43.	Y/color difference input	100	200	300	ns
	TDYRGB	INPUT 0		RGB input	0	100	200	ns

Item	Symbol	Serial data settings	Measurement conditions	Min.	Typ.	Max.	Unit
Color difference signal block (Y/color difference input)							
Color difference input color adjustment characteristics	GEXCMX	COLOR 255 INPUT 1	SW59 and SW61 = B, SW60 = A Input SIG1 (0dB, 100kHz) to (A) and measure the output amplitude (100kHz) at TP40. Assume the output amplitude when serial bus register COLOR = 128 as VC0, when COLOR = 0 as VC2, and when COLOR = 255 with SIG1 = –10dB as VC1. GEXCMX = 20 log (VC1/VC0) + 10 GEXCMN = 20 log (VC2/VC0), Color difference input	3	5		dB
	GEXCMN	COLOR 0 INPUT 1			–20	–15	dB
Color difference balance	VEXCBL	INPUT 1	SW59 and SW61 = B, SW60 = A Input SIG1 (0dB, 100kHz) to (A). Assume the output amplitude (100kHz) at TP40 as VB and the output amplitude (100kHz) at TP45 as VR. VR/VB	0.8	1.0	1.2	—
Color difference input balance adjustment R	GEXRMX	HUE 255 INPUT 1	SW59 and SW61 = B, SW60 = A Input SIG1 (–6dB, 100kHz) to (A). Measure the output amplitude (100kHz) VR at TP45 and the output amplitude (100kHz) VB at TP40. Assume the output amplitudes when serial bus register HUE = 128 as VR0 and VB0, respectively, when HUE = 255 as VR1 and VB1, respectively, and when HUE = 0 as VR2 and VB2, respectively. GEXRMX = 20 log (VR1/VR0) GEXRMN = 20 log (VR2/VR0) GEXBMX = 20 log (VB1/VB0) GEXBMN = 20 log (VB2/VB0), Color difference input		–5	–2	dB
	GEXRMN	HUE 0 INPUT 1		2	3		dB
Color difference input balance adjustment B	GEXBMX	HUE 255 INPUT 1		2	3		dB
	GEXBMN	HUE 0 INPUT 1			–5	–2	dB
G-Y matrix characteristics	VEXGB	INPUT 1	SW59 and SW60 = A, SW61 = B Input SIG1 (0dB, 100kHz) to (A). Assume the output amplitude (100kHz) at TP43 as VEXG and the output amplitude (100kHz) at TP40 as VEXB. VEXG/VEXB, Color difference input	0.16	0.19	0.22	—
	VEXGR	INPUT 1	SW59 = B, SW60 and SW61 = A Input SIG4 (0dB, 100kHz) to (A). Assume the output amplitude (100kHz) at TP43 as VEXG and the output amplitude (100kHz) at TP45 as VEXR. VEXG/VEXR, Color difference input	0.46	0.51	0.56	—

Item	Symbol	Serial data settings	Measurement conditions		Min.	Typ.	Max.	Unit
RGB signal output block								
RGB frequency response	FRGBH	LPF 0 TONE 1	SW59, SW60 and SW61 = B Assume the output amplitude at TP43 when SIG1 (0dB, 100kHz) is input to (A) as 0dB. Vary the frequency of the input signal to obtain the frequency with an output amplitude of –3dB. S/H OFF, RGB input	LPF high	5.5			MHz
	FRGBL	LPF 1 TONE 1		LPF Low	4.0			MHz
RGB signal DC output voltage	VOUT		SW59, SW60 and SW61 = B Input SIG4 (VL = 0mV) to (A) and adjust serial bus register BRIGHT so that the output at TP43 is 9Vp-p (black-black). Measure the DC voltage at TP40, TP43 and TP45.		5.8	6.0	6.2	V
RGB signal DC voltage difference	dVOUT		Obtain the maximum difference between each of the DC voltage measurement values of TP40, TP43 and TP45 in the preceding item VOUT.			0	120	mV
RGB maximum output range	OUTMAX	BRT 0 U-BRT 0	SW59, SW60 and SW61 = B Input SIG4 (VL = 0mV) to (A) and measure the output amplitude (black-black) at TP40, TP43 and TP45.		9.8			V
SIG.C variable range	VORNG		SW48 = ON Adjust V48 to 5.2V or 6.5V in the VOUT measurement conditions and confirm that dVOUT is satisfied and that $\|V48 - VOUT\| \leq 0.15V$.		5.2		6.5	V
Amount of change in U-BRIGHT	UBRTMX	U-BRT 255 CONT 255	SW59, SW60 and SW61 = B Input SIG2 to (A) and measure the amount of change in the black level output at TP40, TP43 and TP45 when serial bus register U-BRIGHT is changed from 128 to 255.		2.0	3.0		V
	UBRTMN	U-BRT 0 CONT 255	SW59, SW60 and SW61 = B Input SIG2 to (A) and measure the amount of change in the white level output at TP40, TP43 and TP45 when serial bus register U-BRIGHT is changed from 128 to 0.			–3.0	–2.0	V
Amount of change in BRIGHT	BRTMX	BRT 255 CONT 255	SW59, SW60 and SW61 = B Input SIG2 to (A) and measure the amount of change in the black level output at TP40, TP43 and TP45 when serial bus register BRIGHT is changed from 128 to 255.		2.0	2.5		V
	BRTMN	BRT 0 CONT 255	SW59, SW60 and SW61 = B Input SIG2 to (A) and measure the amount of change in the white level output at TP40, TP43 and TP45 when serial bus register BRIGHT is changed from 128 to 0.			–2.5	–2.0	V

Item	Symbol	Serial data settings	Measurement conditions	Min.	Typ.	Max.	Unit
Amount of change in SUB-BRIGHT	SBBRTR	BRT 160 R-BRT 255 R-BRT 0	SW59, SW60 and SW61 = B Input SIG4 (VL = 0mV) to (A) and measure the difference between the output (black-black) at TP45 when serial bus register R-BRT = 128 and when R-BRT = 0 and 255.	±1.3	±1.7		V
	SBBRTB	BRT 160 B-BRT 255 B-BRT 0	SW59, SW60 and SW61 = B Input SIG4 (VL = 0mV) to (A) and measure the difference between the output (black-black) at TP40 when serial bus register B-BRT = 128 and when B-BRT = 0 and 255.	±1.3	±1.7		V
Difference in gain between RGB output signals	dGRGB		SW59, SW60 and SW61 = B Input SIG3 to (A) and obtain the level difference between the maximum and minimum non-inverted output amplitudes (white-black) at TP40, TP43 and TP45.	–0.6	0	0.6	dB
Amount of change in SUB-CONTRAST	SBCNTR	CONT 70 R-CNT 255 R-CNT 0	SW59, SW60 and SW61 = B Input SIG3 to (A) and measure the difference between the non-inverted output (white-black) at TP45 and the non-inverted output (white-black) at TP43 when serial bus register R-CNT = 0 and when R-CNT = 255.	±2.0			dB
	SBCNTB	CONT 70 B-CNT 255 B-CNT 0	SW59, SW60 and SW61 = B Input SIG3 to (A) and measure the difference between the non-inverted output (white-black) at TP40 and the non-inverted output (white-black) at TP43 when serial bus register B-CNT = 0 and when B-CNT = 255.	±2.0			dB
Difference in RGB output inverted/ non-inverted gain	dGINV		SW59, SW60 and SW61 = B Input SIG3 to (A) and obtain the difference between the non-inverted output amplitudes (white-black) and the inverted output amplitudes at TP40, TP43 and TP45.	–0.3	0	0.3	dB
Difference in black level potential between RGB output signals	dVBL		SW59, SW60 and SW61 = B Input SIG3 to (A) and obtain the level difference between the maximum and minimum black levels of both the inverted and non-inverted outputs at TP40, TP43 and TP45.			300	mV
γ gain	Gγ1	γ1 120 γ2 210	SW59, SW60 and SW61 = B Input SIG7 to (A) and adjust the non-inverted output amplitude (white-black) at TP43 to 3.5Vp-p with serial bus register CONTRAST and the black level at TP43 to 1.5V with serial bus register BRIGHT. Measure VG1, VG2 and VG3. Gγ1 = 20 log (VG1/0.0357) Gγ2 = 20 log (VG2/0.0357) Gγ3 = 20 log (VG3/0.0357) (See Fig. 4.)	23.0	26.0	29.0	dB
	Gγ2			12.0	15.0	18.0	dB
	Gγ3			18.0	22.0	26.0	dB

Item	Symbol	Serial data settings	Measurement conditions	Min.	Typ.	Max.	Unit
γ1 adjustment variable range	Vγ1MN	γ1 0 γ2 0 CONT 60	SW59, SW60 and SW61 = B Input SIG7 to (A) and adjust serial bus register BRIGHT so that the output at TP43 is 9Vp-p (black-black). Read the point where the gain of the non-inverted output at TP43 changes when serial bus register γ1 = 0 and 255 from the input signal IRE level. Vγ1MN when γ1 = 0, and Vγ1MX when γ1 = 255.			0	IRE
	Vγ1MX	γ1 255 γ2 0 CONT 60		100			IRE
γ2 adjustment variable range	Vγ2MN	γ1 0 γ2 0 CONT 60	SW59, SW60 and SW61 = B Input SIG7 to (A) and adjust serial bus register BRIGHT so that the output at TP43 is 9Vp-p (black-black). Read the point where the gain of the non-inverted output at TP43 changes when serial bus register γ2 = 0 and 255 from the input signal IRE level. Vγ2MN when γ2 = 0, and Vγ2MX when γ2 = 255.	100			IRE
	Vγ2MX	γ1 0 γ2 255 CONT 60				0	IRE
RGB output white limiter operation voltage	VWLIMX	γ2 255 W-LIM 0 U-BRT 255	SW59, SW60 and SW61 = B Input SIG2 to (A) and measure the potential difference between the white limiter level of the TP43 output and SIG CENTER. VWLIMX when serial bus register WHITE-LIM = 0, and VWLIMN when WHITE-LIM = 3.	1.0	1.1	1.2	V
	VWLIMN	γ2 255 W-LIM 3 U-BRT 255		0.45	0.55	0.65	V
RGB output black limiter operation voltage	VBLIMX	B-LIM 255 U-BRT 0	SW59, SW60 and SW61 = B Input SIG2 to (A), vary serial bus register BLACK-LIM and measure the inverted/non-inverted black limiter amplitude (black-black) over which the black limiter operates for the TP40, TP43 and TP45 outputs. VBLIMX when BLACK-LIM = 255, and VBLIMN when BLACK-LIM = 0	9.0			V
	VBLIMN	B-LIM 0 U-BRT 0				7.0	V
Black limiter DC voltage difference	dVBLIM	BRT 0 W-LIM = 0	SW59, SW60 and SW61 = B Input SIG4 (VL = 0mV) to (A) and adjust serial bus register BLACK-LIM so that the output at TP43 is 9Vp-p (black-black). Measure the DC voltage at TP40, TP43 and TP45 and obtain the difference versus VOUT.		0	100	mV
White limiter DC voltage difference	dVWLIM	BRT 255 W-LIM = 0	SW59, SW60 and SW61 = B Input SIG4 (VL = 350mV) to (A), measure the DC voltage at TP40, TP43 and TP45 and obtain the difference versus VOUT.		0	100	mV
Amount of change in COMMON output	COMMX	COM 63	Measure the DC voltage of the TP35 output. Output current ±1mA COMMX when serial bus register COM = 63, and COMMN when COM = 0.	6.15			V
	COMMN	COM 0				4.65	V

Item	Symbol	Serial data settings	Measurement conditions		Min.	Typ.	Max.	Unit
Filter characteristics								
Color difference input LPF characteristics	DEMLPF	INPUT 1	SW59 and SW61 = B, SW60 = A Assume the output amplitude (100kHz) of TP43 when SIG1 (0dB, 100kHz) is input to (A) as 0dB. Vary the frequency of the input signal to obtain the frequency with an output amplitude of –3dB.		1.7	2.3	3.0	MHz
Sync separation, TG block								
Input sync signal width sensitivity	WSSEP		SW59, SW60 and SW61 = B Input SIG4 (VL = 0mV, VS = 143mV, WS variable) to (A) and confirm that it is synchronized with the TP18 (HDO) output. Gradually narrow the WS of SIG4 from 4.7µs and obtain the value at which synchronization with the TP18 (HDO) output is lost.		2.0			µs
Sync separation input sensitivity	VSSEP		SW59, SW60 and SW61 = B Input SIG4 (VL = 0mV, WS = 4.7µs, VS variable) to (A) and confirm that it is synchronized with the TP18 (HDO) output. Gradually reduce the VS of SIG4 from 143mV and obtain the value at which synchronization with the TP18 (HDO) output is lost.			40	60	mV
Sync separation output delay time	TDSY1		SW59, SW60 and SW61 = B Input SIG4 (VL = 0mV, WS = 4.7µs, VS = 143mV) to (A) and measure the delay time with the TP5 (RPD) output. TDSY1 is from the falling edge of the input HSYNC to the front edge of the TP5 (RPD) output, and TDSY2 is from the rising edge of the input HSYNC to the rear edge of the TP5 (RPD) output.		300	500	700	ns
	TDSY2				150	350	550	ns
Horizontal pull-in range	HPLLN	SYSTEM 0	SW59, SW60 and SW61 = B Input SIG4 (VL = 0mV, WS = 4.7µs, VS = 143mV, horizontal frequency variable) to (A) and confirm that it is synchronized with the TP18 (HDO) output. Obtain the frequency f_H at which the input and output are synchronized by changing the horizontal frequency of SIG4 from the non-synchronized condition. Calculate the following: NTSC = f_H – 15734, PAL = f_H – 15625	NTSC	±500			Hz
	HPLLP	SYSTEM 1		PAL	±500			Hz

Item	Symbol	Serial data settings	Measurement conditions	Min.	Typ.	Max.	Unit
OSD I/O characteristics							
OSD RGB input threshold voltage	VTEXTB		SW59, SW60 and SW61 = B Input SIG4 (VL = 0mV) to (A) and SIG5 (VL variable) to (B). Raise the amplitude (VL) from 0V and assume the voltage where the outputs at TP40, TP43 and TP45 go to black level as VTEXTB. Then raise the amplitude further and assume the voltage where these outputs go to white level as VTEXTW.	0.9	1.0	1.1	V
	VTEXTW	BRT 90		1.9	2.0	2.1	V
Propagation delay time between input and output during OSD RGB input	TD1EXT		SW59, SW60 and SW61 = B Input SIG4 (VL = 0mV) to (A) and SIG5 (VL = 3V) to (B). Measure the rise delay time TD1EXT and the fall delay time TD2EXT of the outputs at TP40, TP43 and TP45. (See Fig. 5.)	50	90	130	ns
	TD2EXT			70	100	150	ns
Output blanking level during OSD RGB input	EXTBK		SW59, SW60 and SW61 = B Input SIG4 (VL = 0mV) to (A) and SIG5 (VL = 1.0V) to (B). Measure the difference from the black level of the outputs at TP40, TP43 and TP45.			0	V
Output white level during OSD RGB input	EXTWT		SW59, SW60 and SW61 = B Input SIG4 (VL = 0mV) to (A) and SIG5 (VL = 2.7V) to (B). Measure the difference from the black level of the outputs at TP40, TP43 and TP45.	3.0			V
Minimum pulse width during OSD RGB input	TEXMIN		SW59, SW60 and SW61 = B Input SIG4 (VL = 0mV) to (A) and SIG5 (VL = 2.7V) to (B). Measure the minimum pulse width at which each of the outputs at TP40, TP43 and TP45 reach the white limiter.			145	ns
Serial transfer block							
Data setup time	ts0		SEN setup time, activated by the rising edge of SCK. (See Fig. 6.)	150			ns
	ts1		SDAT setup time, activated by the rising edge of SCK. (See Fig. 6.)	150			ns
Data hold time	th0		SEN hold time, activated by the rising edge of SCK. (See Fig. 6.)	150			ns
	th1		SDAT hold time, activated by the rising edge of SCK. (See Fig. 6.)	150			ns
Minimum pulse width	tw1L		SCK pulse width. (See Fig. 6.)	145			ns
	tw1H		SCK pulse width. (See Fig. 6.)	145			ns
	tw2		SEN pulse width. (See Fig. 6.)	1			µs

Electrical Characteristic Measurement Method Diagrams

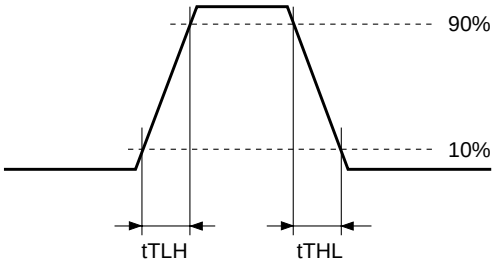


Fig. 2. Output transition time measurement conditions

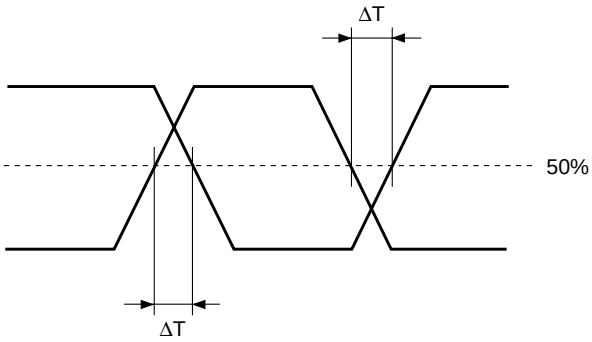


Fig. 3. Cross-point time difference measurement conditions

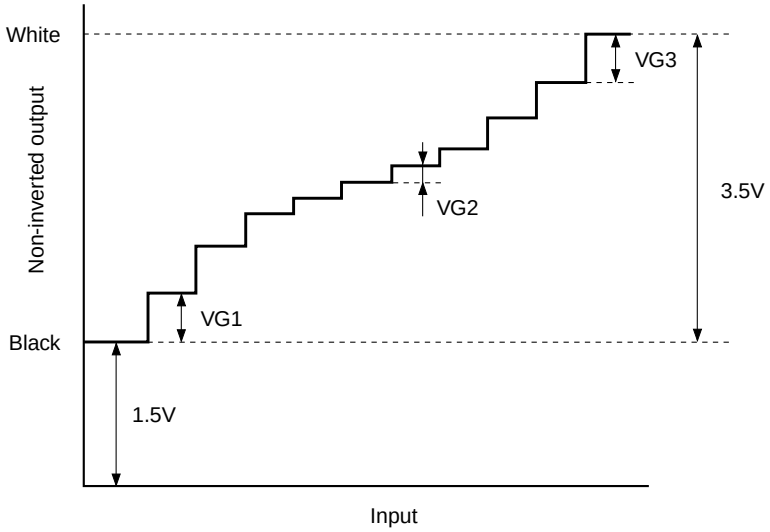


Fig. 4. γ characteristics measurement conditions

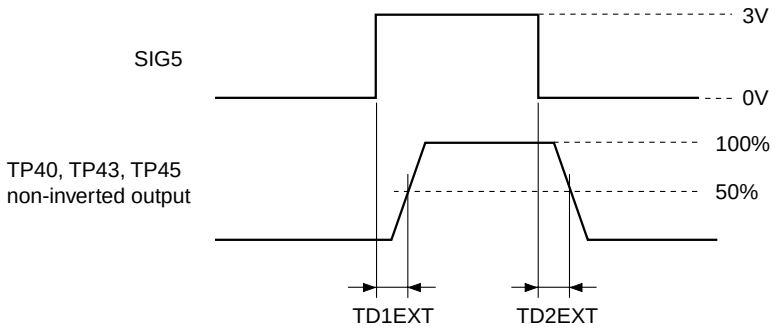


Fig. 5. Delay between external RGB input and output

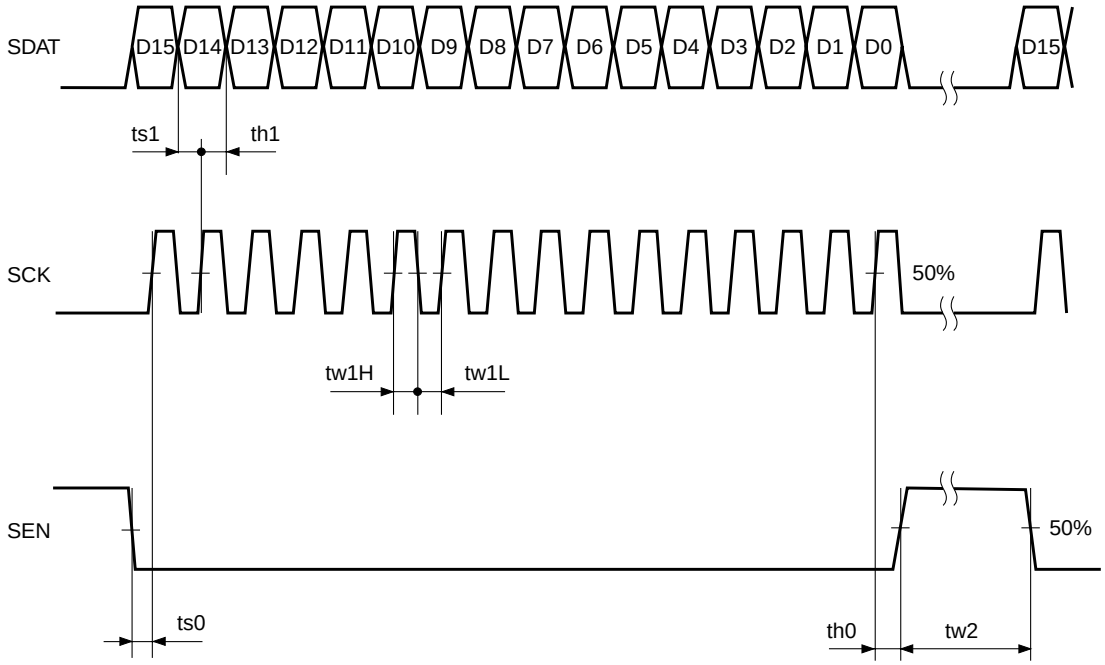
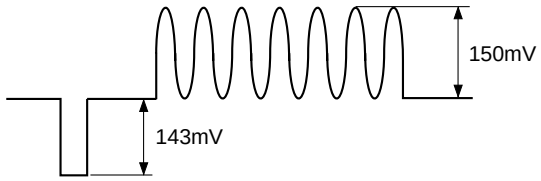
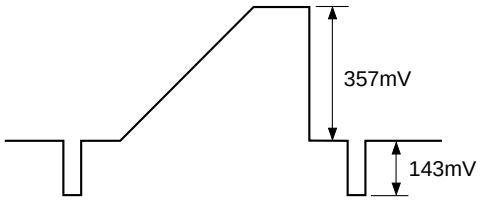
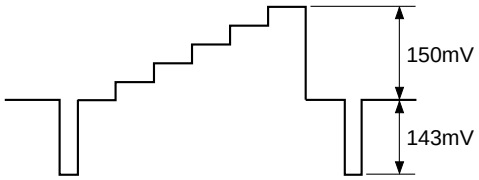
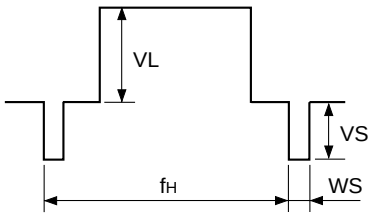
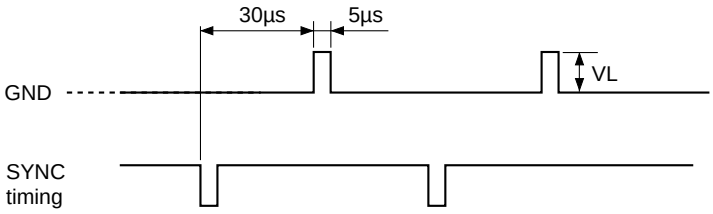
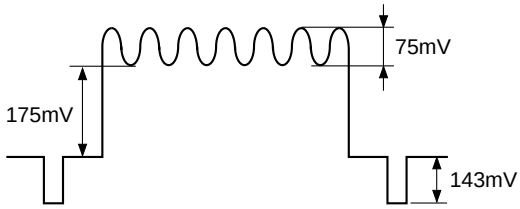
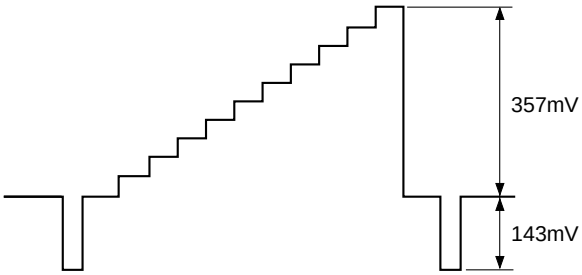
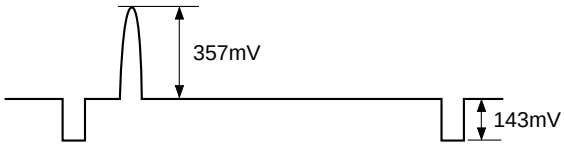


Fig. 6. Serial transfer block measurement conditions

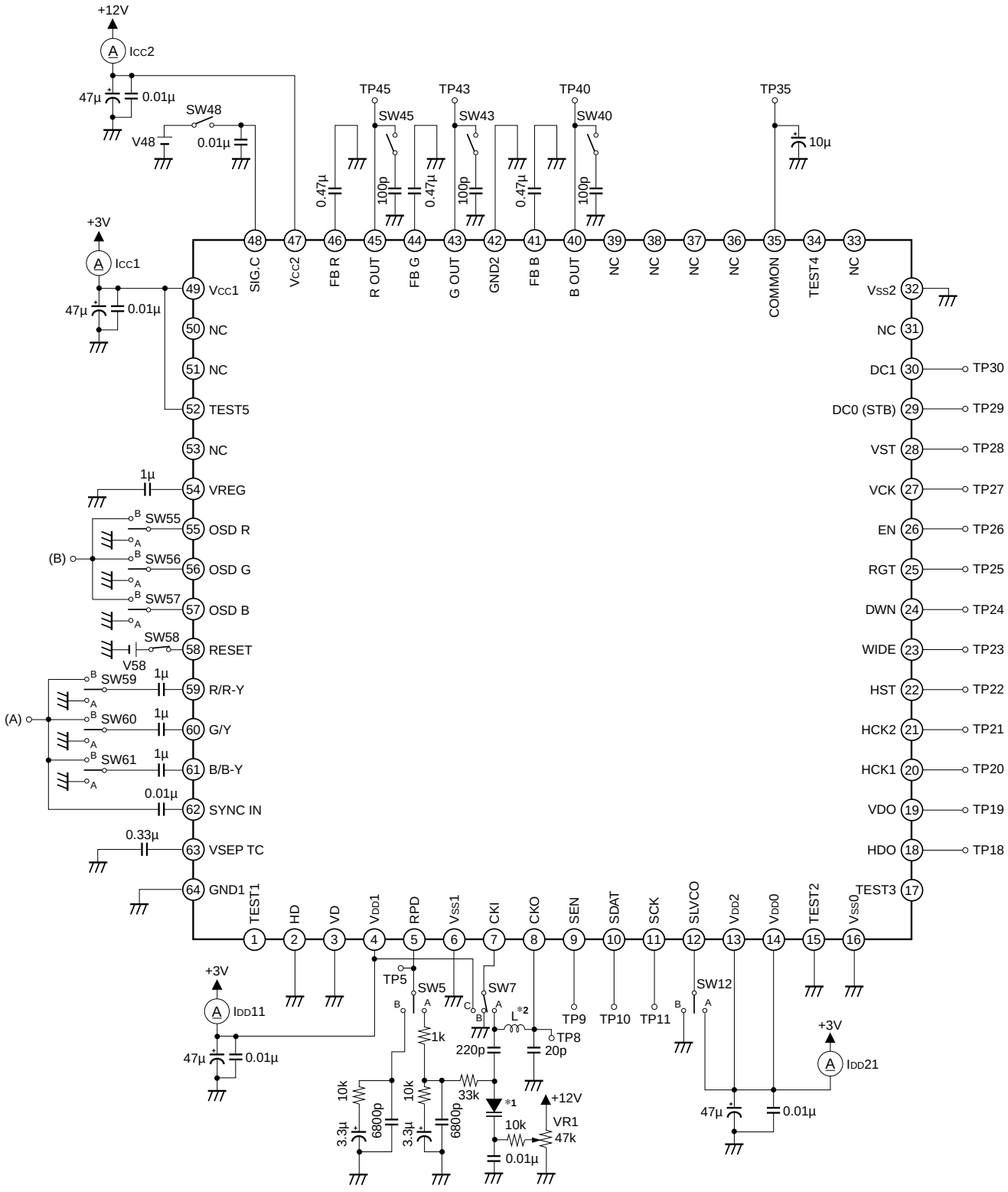
Input Waveforms (1)

SIG No.	Waveform
SIG1	 Sine wave video signal (amplitude and frequency variable) ← Value noted on left: 0dB
SIG2	
SIG3	 5-step staircase waveform
SIG4	 VL amplitude variable VS variable: 143mV unless otherwise specified WS variable: 4.7µs unless otherwise specified fH variable: 15.734kHz (NTSC) or 15.625kHz (PAL) unless otherwise specified
SIG5	 VL amplitude: variable

Input Waveforms (2)

SIG No.	Waveform
SIG6	 Frequency variable
SIG7	10-step staircase waveform 
SIG8	SIN^2 2T pulse waveform 

Electrical Characteristics Measurement Circuit



*1 Varicap diode: MA365 (Matsushita)
*2 L value: 113K pixels = 8.2µH
180K pixels = 3.9µH

Description of Operation

1) RGB and Y/color difference signal processing block

Signal processing is comprised of PICTURE, EXTCOL & BALANCE, LPF (color difference signal), MATRIX, TONE, CONTRAST, SUB-CONTRAST, γ correction, OSD, LPF (RGB signal), sample-and-hold, USER-BRIGHT, BRIGHT, SUB-BRIGHT and output circuits.

• Input mode switching
The input mode (Y/color difference input, RGB input) is switched by serial communication.

During internal sync separation signal input
- During RGB input: The R signal is input to Pin 59, the G signal to Pin 60, the B signal to Pin 61, and SYNC on SIGNAL to Pin 62.
- During Y/color difference input: The R-Y signal is input to Pin 59, the Y signal to Pins 60 and 62, and the B-Y signal to Pin 61.

During external sync separation signal input
- During RGB input: The R signal is input to Pin 59, the G signal to Pin 60, the B signal to Pin 61, CSYNC/HD to Pin 2, and VD to Pin 3.
- During Y/color difference input: The R-Y signal is input to Pin 59, the Y signal to Pin 60, the B-Y signal to Pin 61, CSYNC/HD to Pin 2, and VD to Pin 3.

• NTSC/PAL switching
The input system (NTSC/PAL) is switched by serial communication.

• PICTURE circuit
This performs aperture correction for the Y signal (sharpness function). The correction amount is controlled by serial communication.

• EXTCOL & BALANCE circuit
This is the chromaticity and hue adjustment circuit for the color difference signal. It is set by the serial communication registers COLOR and HUE.

• LPF circuit (color difference signal)
This is the band limitation filter for the color difference signal. It is used to eliminate the noise component.

• MATRIX circuit
This circuit converts Y/color difference signals into RGB signals.

• TONE circuit
This circuit switches the frequency response during RGB input. Switching is performed by serial communication.

• CONTRAST adjustment circuit
This adjusts the white-black amplitude by serial communication to set the input RGB signal to the appropriate level.

• SUB-CONTRAST circuit

This adjusts the white-black amplitude of the R and B signals by serial communication. This circuit is used to adjust the white balance.

• γ correction

In order to support the characteristics of LCD panels, the I/O characteristics are as shown in Fig. 1. The γ1 gain transition point A voltage changes as shown in Fig. 2 by adjusting the serial bus register γ1, and the γ2 gain transition point B voltage changes as shown in Fig. 3 by adjusting γ2.

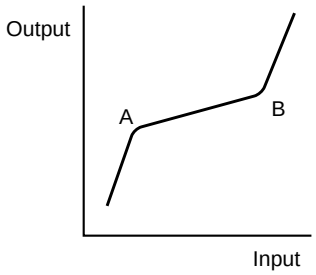


Fig. 1

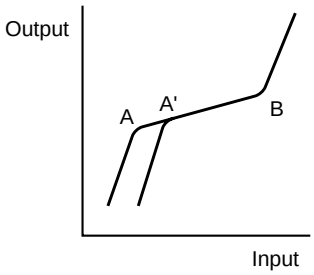


Fig. 2. γ1 adjustment

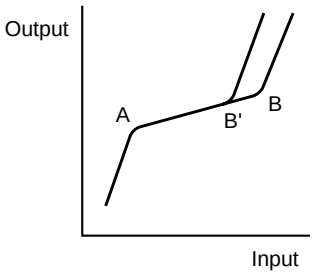


Fig. 3. γ2 adjustment

• OSD circuit

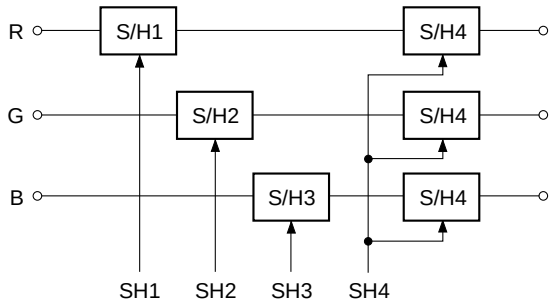
This inputs the OSD pulses. There are two input threshold values: Vth1 (Vcc1 × 1/3) and Vth2 (Vcc1 × 2/3). When an input exceeds Vth1, the corresponding output falls to the level specified by BLACK-LIMITER. When an input exceeds Vth2, the corresponding output rises to the level specified by WHITE-LIMITER. Also, when one of the RGB inputs exceeds Vth1, any signal outputs not exceeding Vth1 also fall to the level specified by BLACK-LIMITER.

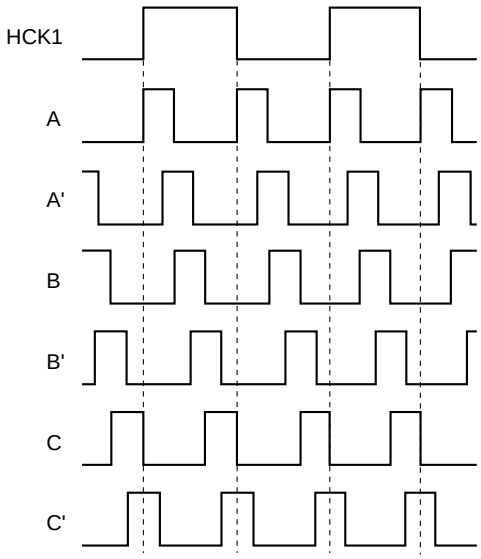
• LPF circuit (RGB signal)

This is the band limitation filter for the RGB signal. It is used to eliminate the noise component generated at the front end of this IC. The characteristics can be switched to match the panel by serial communication.

• Sample-and-hold circuit

As LCD panels sample RGB signals simultaneously, RGB signals output from the CXA3272R must be sampled-and-held in sync with the LCD panel drive pulses.





RGT = H (normal display)

	SHS1	SHS2	SHS3	SHS4	SHS5	SHS6
SH1	B	A'	A	C'	C	B'
SH2	Through	Through	Through	Through	Through	Through
SH3	A	C'	C	B'	B	A'
SH4	C	B'	B	A'	A	C'

RGT = L (right/left inverted display)

	SHS1	SHS2	SHS3	SHS4	SHS5	SHS6
SH1	B	A'	A	C'	C	B'
SH2	A	C'	C	B'	B	A'
SH3	Through	Through	Through	Through	Through	Through
SH4	C	B'	B	A'	A	C'

SH1: R signal SH pulse
SH2: G signal SH pulse
SH3: B signal SH pulse
SH4: RGB signal SH pulse

SHS1 to SHS6: Serial data settings

The sample-and-hold circuit performs sample-and-hold by receiving the SH1 to SH4 pulses from the TG block. Since LCD panels perform color coding using an RGB delta arrangement, each horizontal line must be compensated by 1.5 dots. This relationship is reversed during right/left inverted display. This compensation timing is also generated by the digital block. The sample-and-hold timing changes according to the phase relationship with the HCK pulse, so the timing should be set to position SHS1 to SHS6 in accordance with the actual board.

• USER-BRIGHT circuit

This is used to adjust the black-black amplitude of polarity-inverted RGB output signals. It is not interlinked with the γ transition points.

• BRIGHT circuit

This is used to adjust the black-black amplitude of polarity-inverted RGB output signals. It is interlinked with the γ transition points.

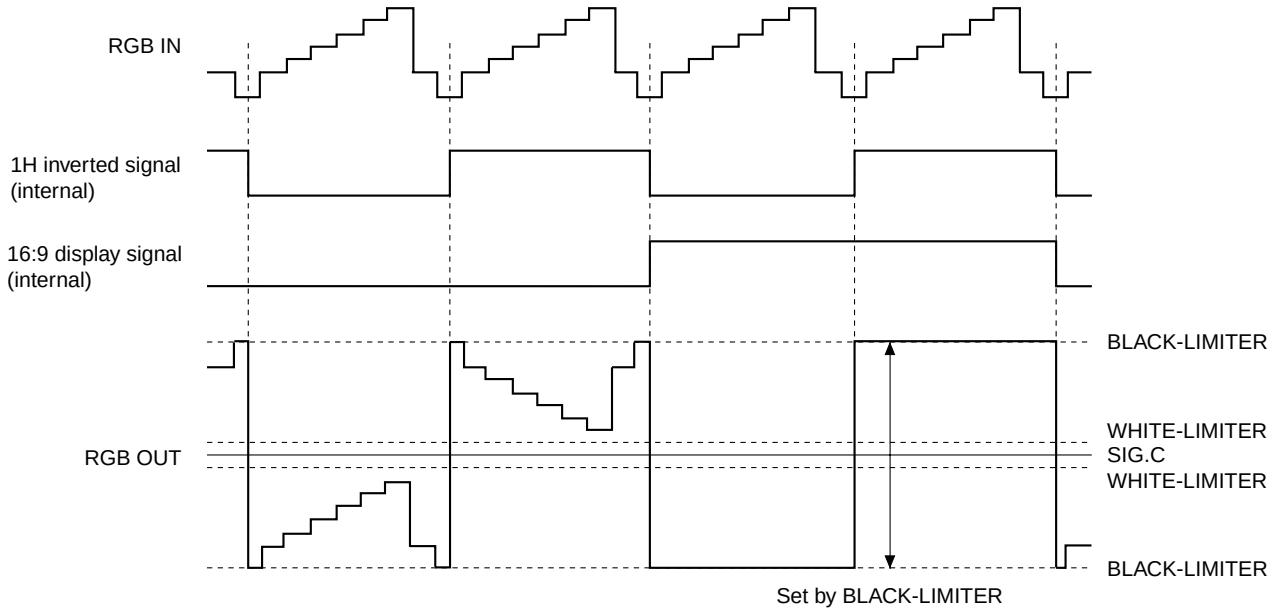
• SUB-BRIGHT circuit

This adjusts the black level of the R and B signals by serial communication. This circuit is used to adjust the white balance.

• Output circuit

RGB output (Pins 40, 43, and 45) signals are inverted each horizontal line by the FRP pulse (internal pulse) supplied from the TG block as shown in the figure below. Feedback is applied so that the center voltage (SIG.C) of the output signal matches the reference voltage (Vcc2 + GND2)/2 (or the voltage adjusted by applying the reference potential to Pin 48 SIG.C from an external source). In addition, the white level output is clipped at the limiter operation point that is set by the serial communication register WHITE-LIMITER, and the black level output is clipped at the limiter operation point that is set by the serial communication register BLACK-LIMITER.

During 16:9 display the RGB output is specified by BLACK-LIMITER at some timings, and the RGB output goes to BLACK-LIMITER level output.



2) Common voltage generation circuit block

The common voltage generation circuit generates and supplies the common pad voltage of the LCD panel. The voltage is offset by serial communication using the SIG.C voltage as the reference and then output.

3) DC output circuit

There are two DC output circuit systems.
3V can be supplied from the DC0 ad DC1 outputs. On/off control for each output is performed by serial communication.

4) Sync system

- H.FILTER
  This amplifies the sync signal of the input video signal and eliminates the noise with an internal LPF. The sync signal is clamped at the input, so always input via a capacitor.

- SYNC SEP
  This performs horizontal and vertical sync signal separation.

- V SEP
  This performs vertical sync signal separation.

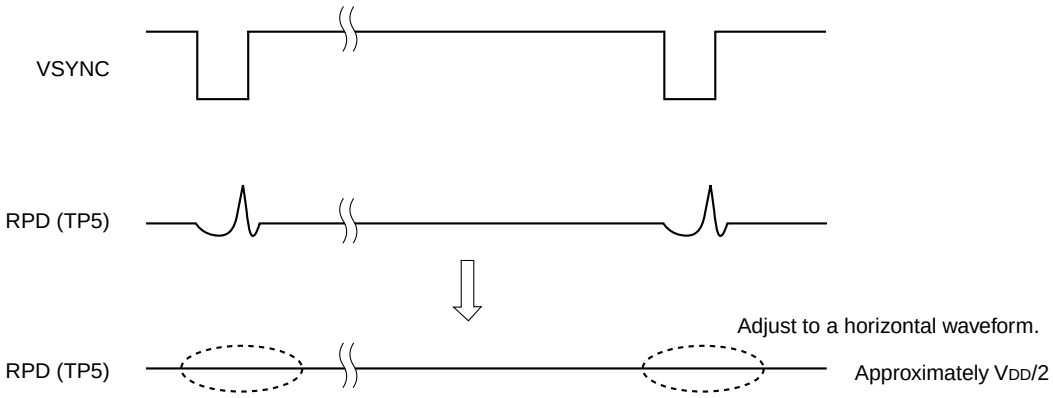
5) TG block

• PLL and AFC circuits

1. Internal VCO circuit

A PLL circuit is comprised by connecting the phase comparator, frequency division counter, internal VCO circuit, and an external LPF circuit. The PLL error detection signal is generated by the HSYNC block, and the integral value of the phase comparison output of the entire bottom of HSYNC and the internal frequency division counter becomes the RPD output (Pin 5).

When using an internal VCO, the PLL is adjusted by setting the serial bus VCO so that the RPD output waveform is horizontal near VSYNC.



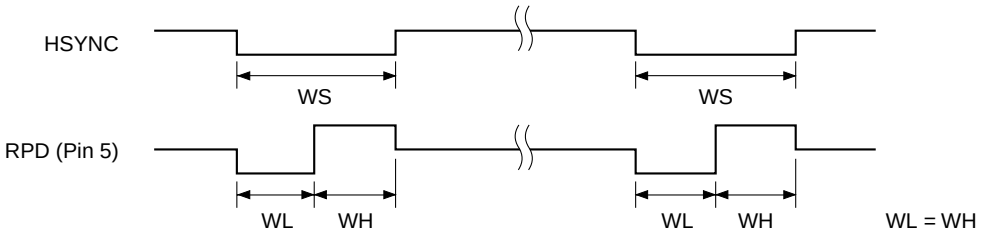
2. External VCO circuit

A PLL circuit is comprised by connecting external VCO and LPF circuits to the phase comparator and frequency division counter.

The PLL error detection signal is generated using the phase comparison output of the entire bottom of the HSYNC and the internal frequency division counter as the RPD output.

RPD output is converted to DC error voltage with the lag-lead filter, and then it changes the capacitance of the varicap diode to maintain a constant oscillation frequency.

When using an external VCO, the PLL is adjusted by setting the reverse bias voltage of the varicap diode so that the point at which RPD changes is at the center of the horizontal sync signal window as shown in the figure below.

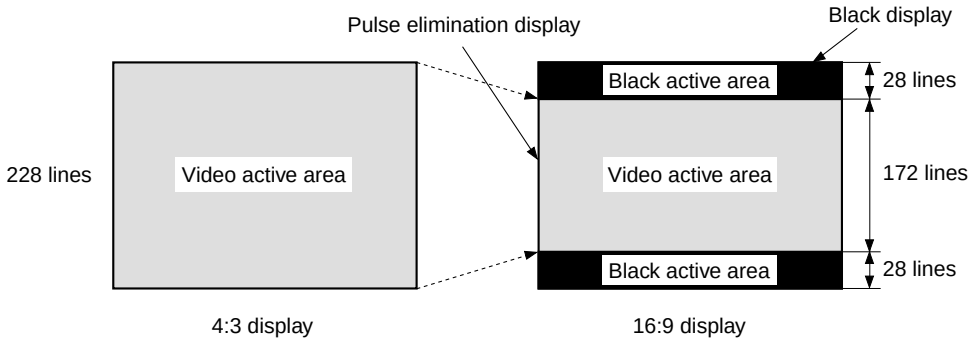


• H-POSITION
This adjusts the horizontal display position. Set by serial communication so that the picture center matches the center of the LCD panel.

• V-POSITION
This adjusts the vertical display position. Set by serial communication so that the picture center matches the center of the LCD panel.

• Right/left (RGT) and/or up/down (DWN) inversion
The video display direction can be switched. The horizontal direction can be switched between right scan and left scan, and the vertical direction can be switched between down scan and up scan. Set the display direction in accordance with the LCD panel mounting position by serial communication.

• Wide mode
16:9 quasi-WIDE display can be achieved by performing aspect ratio conversion through pulse elimination processing. The signal is pulse eliminated and displayed at the rate of 1/4 scanning lines in NTSC mode and 10/28 scanning lines in PAL mode. In addition, a letter box is displayed in the upper and lower portions of the panel at the black level set by BLACK-LIMITER. This function achieves a quasi-display by simply pulse eliminating the video signal, so some video information is lost.

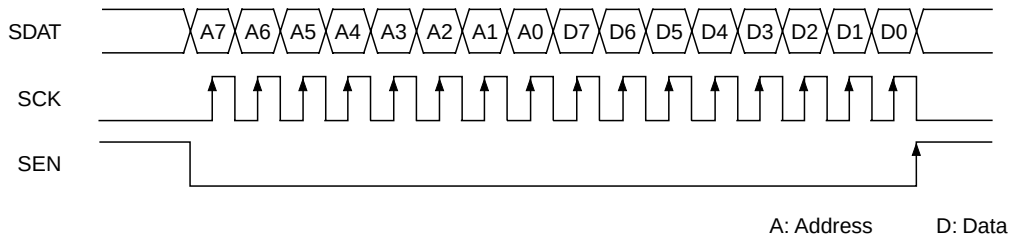


• AC driving of LCD panels during no signal
The output signal runs freely so that the LCD panel is AC driven even when there is no sync signal from the SYNC IN (Pin 62) pin or from the HD (Pin 2) and VD (Pin 3) pins.

Description of Serial Control Operation

1) Control method

Control data consists of 16 bits of data which is loaded one bit at a time at the rising edge of SCK. This loading operation starts from the falling edge of SEN and is completed at the next rising edge.
Digital block control data is established by the vertical sync signal, so if data is transferred multiple times for the same item, the data immediately before the vertical sync signal is valid. Analog (electronic attenuator) block control data becomes valid each time the SEN signal is input.
In addition, if 16 bits or more of SCK are not input while SEN is low, the transferred data is not loaded to the inside of the IC and is ignored. If 16 bits or more of SCK are input, the 16 bits of data before the rising edge of the SEN pulse are valid data.



Serial transfer timing

2) Serial data map (—: don't care)

The serial data map is as follows. Values inside parentheses are the default values.

MSB Address LSB								MSB Data LSB							
A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	Unused (00000000)							
0	0	0	0	0	0	0	1	SLSH2 (0)	SLSH1 (0)	SLSH0 (0)	SLSYNC1 (0)	SLSYNC0 (0)	ASPECT (0)	SYSTEM (0)	INPUT (0)
0	0	0	0	0	0	1	0	VDO POL (0)	HDO POL (0)	SLCLP (0)	SYNC POL (0)	Unused (0)	Unused (0)	LCD1 (0)	LCD0 (0)
0	0	0	0	0	0	1	1	TEST2 (0)	TEST1 (0)	Unused (0)	MBK (0)	FRP1 (0)	FRP0 (0)	SLRGT (0)	SLDWN (0)
0	0	0	0	0	1	0	0	TEST4 (0)	Unused (0)	Unused (0)	Unused (0)	TEST3 (0)	SLDC1 (1)	SLDC0 (0)	SYNC GEN (0)
0	0	0	0	0	1	0	1	—	—	—	H-POSITION (10000)				
0	0	0	0	0	1	1	0	—	—	—	—	—	V-POSITION (011)		
0	0	0	0	0	1	1	1	—	—	—	HD-POSITION (00000)				
0	0	0	0	1	0	0	0	—	—	—	—	—	—	—	—
0	0	0	0	1	0	0	1	—	—	—	TEST5 (10000)				
0	0	0	0	1	0	1	0	—	—	Unused (0)	Unused (0)	TEST7 (0)	TEST6 (0)	LPF (0)	TONE (0)
1	1	0	0	0	0	0	0	HUE (10000000)							
1	1	0	0	0	0	0	1	COLOR (10000000)							
1	1	0	0	0	0	1	0	BRIGHT (10000000)							
1	1	0	0	0	0	1	1	CONTRAST (10000000)							
1	1	0	0	0	1	0	0	R-BRIGHT (10000000)							
1	1	0	0	0	1	0	1	B-BRIGHT (10000000)							
1	1	0	0	0	1	1	0	γ-1 (00000000)							
1	1	0	0	0	1	1	1	γ-2 (00000000)							
1	1	0	0	1	0	0	0	Unused (10000000)							
1	1	0	0	1	0	0	1	R-CONTRAST (10000000)							
1	1	0	0	1	0	1	0	B-CONTRAST (10000000)							
1	1	0	0	1	0	1	1	BLACK-LIM (10000000)							
1	1	0	0	1	1	0	0	PICTURE (10000000)							
1	1	0	0	1	1	0	1	USER-BRIGHT (10000000)							
1	1	0	0	1	1	1	0	VCO (10000000)							
1	1	0	0	1	1	1	1	—	—	COMMON (101010)					
1	1	0	1	0	0	0	0	—	—	—	—	—	Unused (000)		
1	1	0	1	0	0	0	1	—	—	—	—	—	—	WHITE-LIM (11)	
1	1	1	0	1	0	1	0	TEST8							

3) Serial data mode settings (X: don't care)

• INPUT

This switches the input signal format.

INPUT D0	Input signal format	Default
0	RGB input	O
1	Y/color difference input	

• SYSTEM

This switches the input signal system.

SYSTEM D1	Input signal format	Default
0	NTSC	O
1	PAL	

• ASPECT

This switches the video display aspect ratio.

ASPECT D2	Display aspect ratio	Default
0	4:3 display (normal display)	O
1	16:9 display (letterbox, pulse elimination display)	

• SLSYNC1 and SLSYNC0

This switches the sync signal input format.

SLSYNC1: external sync signal input switching, SLSYNC0: external VD input switching

SLSYNC1 D4	SLSYNC0 D3	Sync signal input format	Default
0	0	An analog CSYNC on SIGNAL signal is input to the SYNC IN input. (Internal V separation is used.)	O
1	0	An external digital CSYNC signal is input to the HD input. (Internal V separation is used.)	
1	1	An external digital HD signal is input to the HD input for H. An external digital VD signal is input to the VD input for V.	

• SLSH2 to SLSH0

This switches the sample-and-hold timing.

SLSH2 D7	SLSH1 D6	SLSH0 D5	Sample-and-hold position	Default
0	0	0	SHS1	O
0	0	1	SHS2	
0	1	0	SHS3	
0	1	1	SHS4	
1	0	0	SHS5	
1	0	1	SHS6	
1	1	X	Through (sample-and-hold off)	

• LCD1, LCD0

This switches the supported panel.

LCD1 D1	LCD0 D0	Used panel	Default
0	0	180K pixels: LCX033	
0	1	113K pixels: LCX032	O
1	X	Test mode	

• SYNC POL

This switches the polarity of the input horizontal and vertical sync signals or the C.SYNC signal.

SYNC POL D4	Input horizontal and vertical sync signal or C.SYNC signal polarity	Default
0	Negative polarity input	O
1	Positive polarity input	

• SLCLP

This switches the position at which the input signals are clamped during color difference input.

SLCLP D5	Input signal clamp position	Default
0	Pedestal position	O
1	Sync position	

• HDO POL

This switches the HDO output polarity.

HDO POL D6	HDO output polarity	Default
0	Positive polarity	O
1	Negative polarity	

• VDO POL

This switches the VDO output polarity.

VDO POL D7	VDO output polarity	Default
0	Positive polarity	O
1	Negative polarity	

• SLDWN

This switches the panel display direction (vertical direction).

Each output timing and the DWN pin output are switched.

SLDWN D0	Display	DWN pin output	Default
0	Normal display (down scan)	H	O
1	Up/down inverted display (up scan)	L	

• SLRGT

This switches the panel display direction (horizontal direction).

Each output timing and the RGT pin output are switched.

SLRGT D1	Display	RGT pin output	Default
0	Normal display (right scan)	H	O
1	Right/left inverted display (left scan)	L	

• FRP0

This further inverts the polarity of the RGB output that is inverted every 1H for 4096 fields.

FRP0 D2	4096-field inversion	Default
0	OFF	O
1	ON	

• FRP1

This switches the RGB signal output polarity inversion period. Normally set to 1H inversion.

FRP1 D3	Output polarity inversion period	Default
0	1H inversion	O
1	1-field inversion	

• MBK

This switches the PAL display pulse elimination on/off.

MBK D4	Pulse elimination on/off	Default
0	ON	O
1	OFF	

• SYNC GEN

This sets the sync generator function. Outputs other than HDO and VDO of the TG block are stopped when the sync generator is on.

The DC0 and DC1 outputs always operate regardless of this setting.

SYNC GEN D0	Sync generator	Default
0	OFF	O
1	ON	

• SLDC1, SLDC0

This outputs DC 3V to the DC0 and DC1 pins.

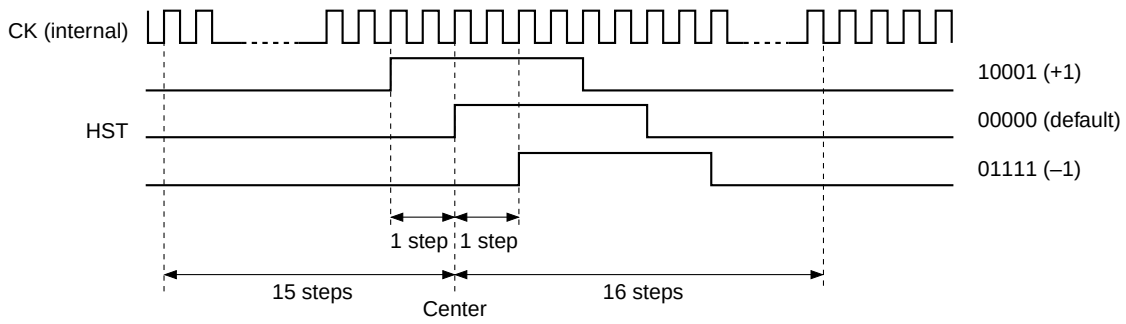
SLDC1 D2	DC1 output	Default
0	L	
1	H	O

SLDC0 D1	DC0 output	Default
0	L	O
1	H	

• H-POSITION

This sets the horizontal display start position. (1 step = 32 settings in 2ck intervals)

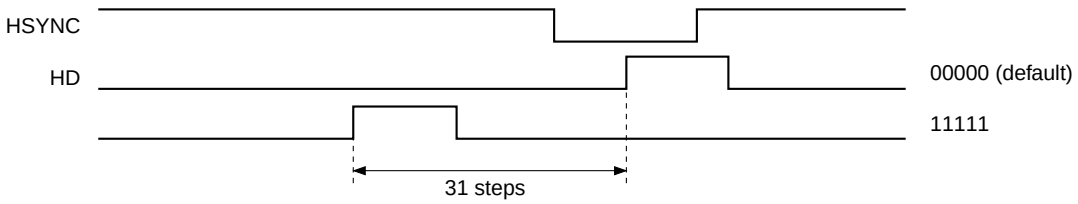
D4/D3/D2/D1/D0 = 00000 to 11111, 10000 (default)



• HD-POSITION

This sets the HD output pulse phase. (1 step = 32 settings in 4ck intervals)

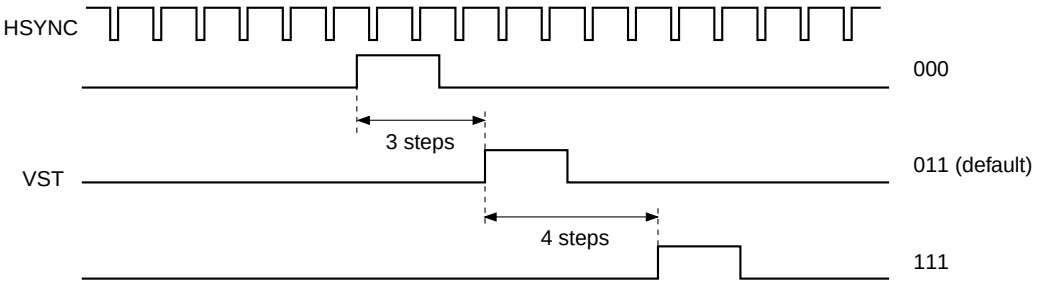
D4/D3/D2/D1/D0 = 00000 to 11111, 00000 (default)



• V-POSITION

This sets the vertical display start position. (1 step = 8 settings in 1H intervals)

D2/D1/D0 = 000 to 111, 011 (default)



• TONE

This switches the frequency response during RGB input.

TONE D0	RGB frequency response	Default
0	Low	O
1	High	

• LPF

This switches the characteristics of the band limitation filter for the RGB signals to match the panel.

LPF D1	LPF frequency response	Default
0	Low	O
1	High	

4) Serial data electronic attenuator settings

• HUE (8 bits)
This adjusts the hue during Y/color difference input.
D7/D6/D5/D4/D3/D2/D1/D0: 00000000 to 10000000 (default) to 11111111 changes the hue.

• COLOR (8 bits)
This adjusts the color gain during Y/color difference input.
D7/D6/D5/D4/D3/D2/D1/D0: 00000000 → 10000000 (default) → 11111111 increases the gain.

• BRIGHT (8 bits)
This adjusts the brightness of the RGB output signals. It is interlinked with the γ transition points.
D7/D6/D5/D4/D3/D2/D1/D0: 00000000 → 10000000 (default) → 11111111 reduces the amplitude (black-black).

• CONTRAST (8 bits)
This adjusts the contrast of the RGB output signals.
D7/D6/D5/D4/D3/D2/D1/D0: 00000000 → 10000000 (default) → 11111111 increases the amplitude (black-white).

• R-BRIGHT/B-BRIGHT (8 bits)
This adjusts the brightness of the R and B output signals.
D7/D6/D5/D4/D3/D2/D1/D0: 00000000 → 10000000 (default) → 11111111 reduces the amplitude (black-black).

• γ-1 (8 bits)
This sets the black side γ point level of the RGB output signals.
D7/D6/D5/D4/D3/D2/D1/D0: 00000000 (default) → 11111111 increases the γ point.
Set the γ-1 point to the black side of the γ-2 point.

• γ-2 (8 bits)
This sets the white side γ point level of the RGB output signals.
D7/D6/D5/D4/D3/D2/D1/D0: 00000000 (default) → 11111111 reduces the γ point.
Set the γ-2 point to the white side of the γ-1 point.

• R-CONTRAST/B-CONTRAST (8 bits)
This adjusts the contrast of the R and B output signals.
D7/D6/D5/D4/D3/D2/D1/D0: 00000000 → 10000000 (default) → 11111111 increases the amplitude (black-white).

• BLACK-LIMITER (8 bits)
This adjusts the black side limiter level of the RGB output signals.
D7/D6/D5/D4/D3/D2/D1/D0: 00000000 → 10000000 (default) → 11111111 reduces the limiter level (black-black).

• PICTURE (8 bits)
This adjusts the picture (sharpness function) gain during Y/color difference input.
D7/D6/D5/D4/D3/D2/D1/D0: 00000000 → 10000000 (default) → 11111111 increases the gain.

• USER-BRIGHT (8 bits)
This adjusts the brightness of the RGB output signals. It is not interlinked with the γ transition points.
D7/D6/D5/D4/D3/D2/D1/D0: 00000000 → 10000000 (default) → 11111111 reduces the amplitude (black-black).

• VCO (8 bits)
This adjusts the PLL when using the internal VCO.
Adjust the serial bus register VCO so that the RPD output waveform is horizontal near VSYNC.
D7/D6/D5/D4/D3/D2/D1/D0: 00000000 to 10000000 (default) to 11111111

• COMMON (6 bits)
This adjusts the common output voltage.
D5/D4/D3/D2/D1/D0: 000000 → 101010 (default) → 111111 increases the output voltage.

• WHITE-LIMITER (2 bits)
This adjusts the white side limiter level of the RGB output signals.
D1/D0: 00 → 11 (default) reduces the potential difference with SIG.C.

5) Setting of serial data unused block and test mode block

• Unused block
The default value of serial data map is set and used.

• TEST0 1, 2, 3, 4, 6 and 7 (1 bit)
This is test mode. "0" is set and used.

TEST0, 1, 2, 3, 4, 6, 7 D2, D3, D4, D6, D7	Status	Default
0	Normal operation	O
1	Test mode	

• TEST5 (5 bits)
This is test mode. Data transmitting to TEST5 address is not required.

TEST5 D4 to D0	Status	Default
XXXXX	Test mode	

• TEST8 (8 bits)
This is a test mode which results automatically if data is sent to the TEST addresses, regardless of the data contents. For this reason, do not perform data transfer using these addresses.

TEST8 D7 to D0	Status	Default
XXXXXXXX	Test mode	

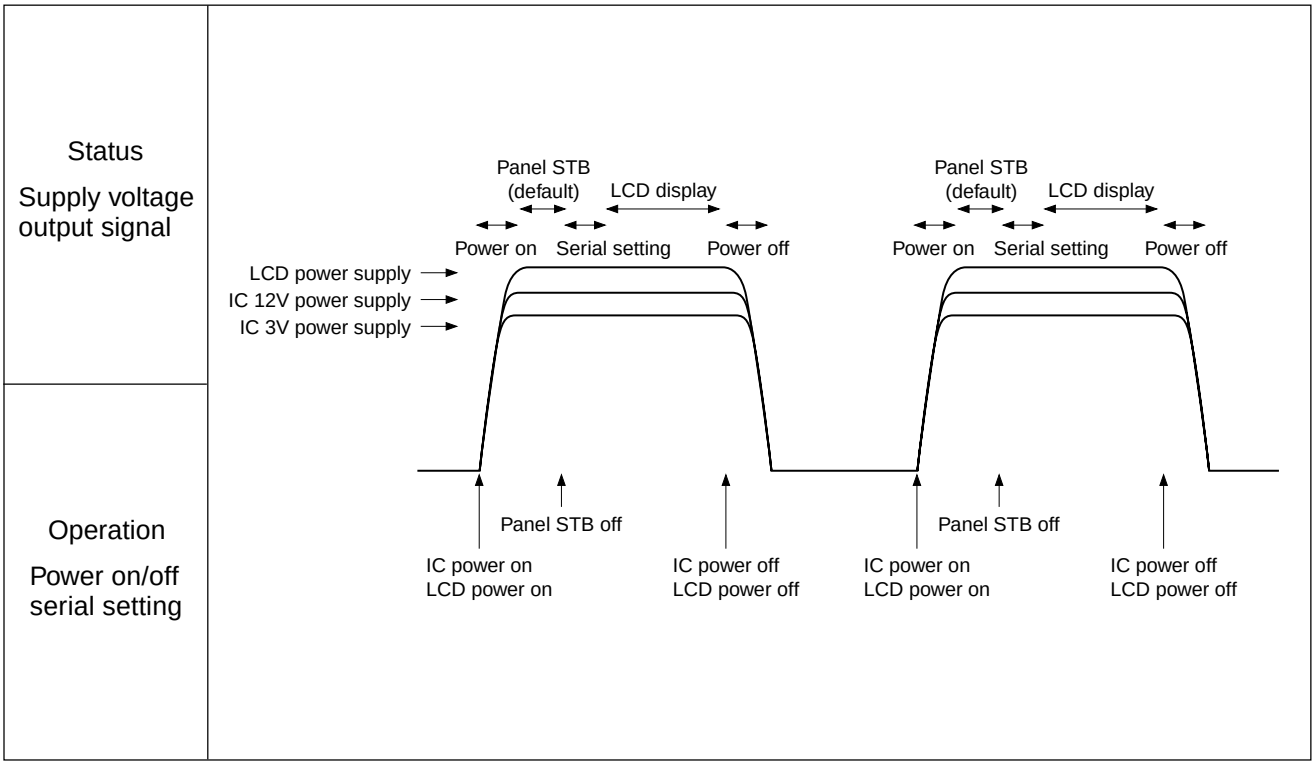
Power Supply and SYNC GEN Mode Sequence

When this IC is used, it is necessary about power supply ON/OFF to surely perform the following power supply sequence on the reliability of a LCD drive system.

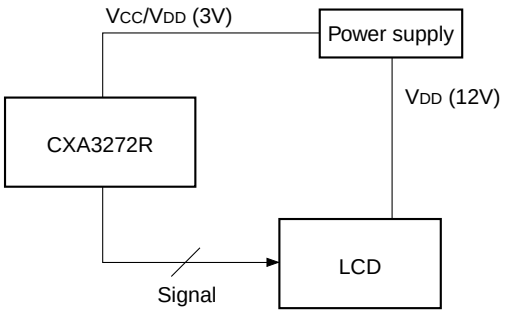
Control timing 1 (when IC and LCD is raised)

(1) IC power on (3V, 12V), LCD power on (V_{DD}: 12V)
(2) Panel STB release-Execute after IC and LCD power supplies are raised
(3) IC power off (3V, 12V), LCD power off (V_{DD}: 12V) — Arbitrary execution

Panel specification should be satisfied as for LCD power supply (V_{DD}: 12V) rise timing.



When IC power is on (default), since STB of the panel is in ON state at the default, cancel STB by serial setting. The serial setting other than STB should be performed during control period to (2) after rising the IC power 3V.

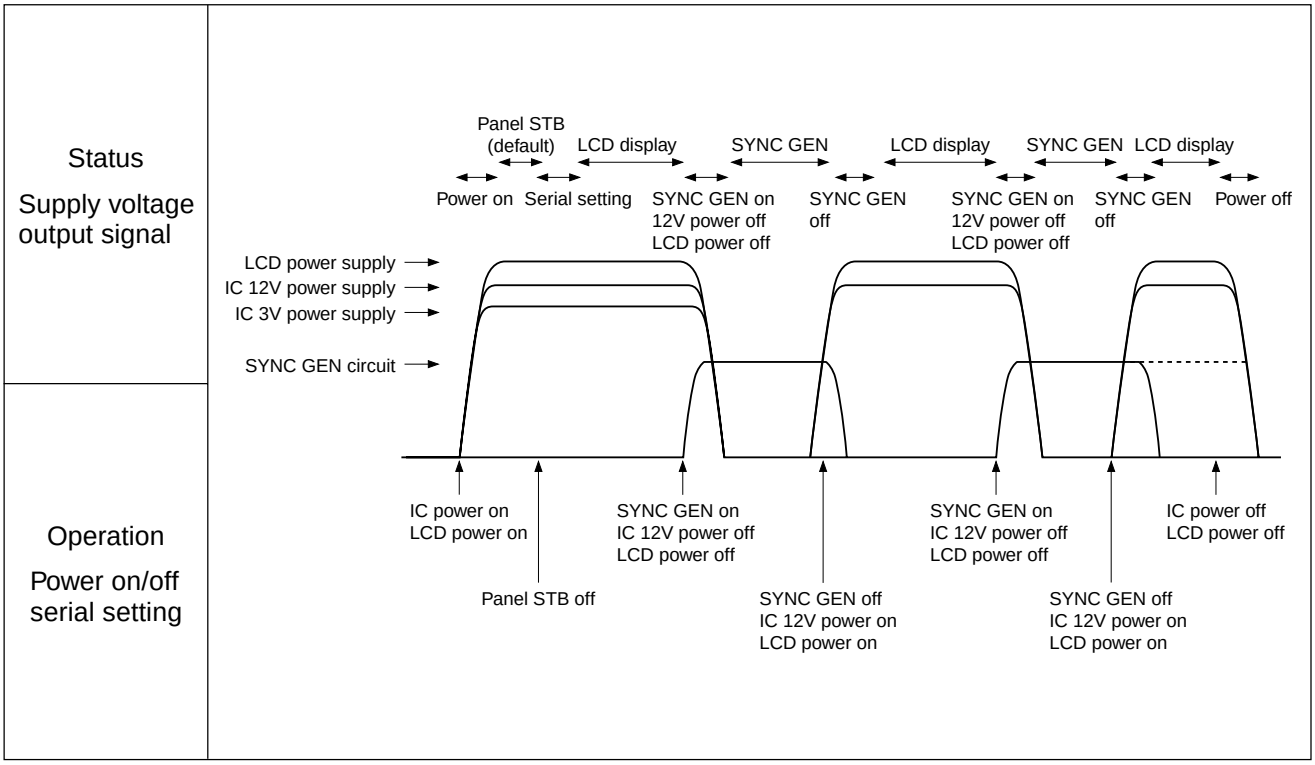


System block diagram

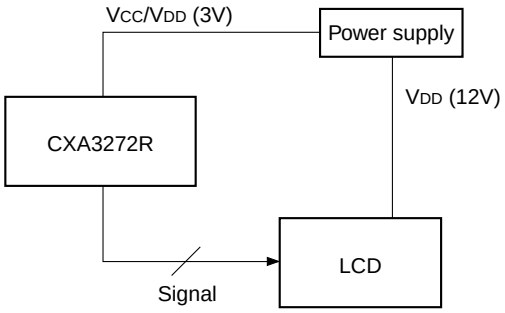
Control timing 2 (SYNC GEN mode on)

(1) IC power on (3V, 12V), LCD power on (V_{DD}: 12V)
(2) Panel STB release — IC and LCD power supplies are raised and executed
(3) SYNC GEN mode on, IC 12V power off, LCD power off — Arbitrary execution
(4) SYNC GEN mode off, IC 12V power on, LCD power on — Arbitrary execution
(5) IC power off (3V, 12V), LCD power off (V_{DD}: 12V) — Arbitrary execution
(4) is not performed, but even if it shifts to (5) from (3), there is no problem. (Dotted line in the figure below.)

Panel specification should be satisfied as for LCD power supply (V_{DD}: 12V) rise timing.



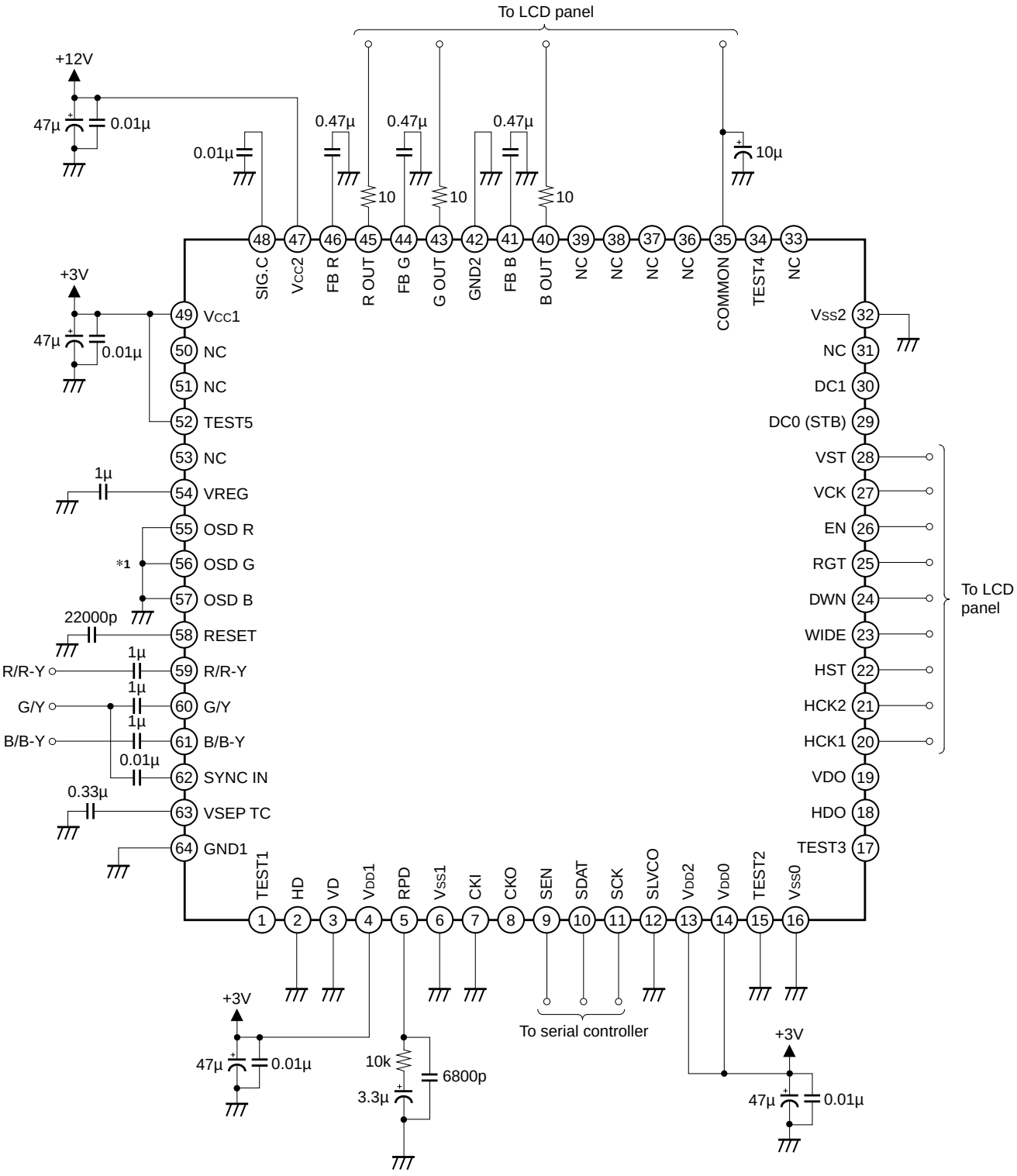
When IC power is on (default), since STB of the panel is in ON state at the default, cancel STB by serial setting. The serial setting other than STB should be performed during control period to (2) after rising the IC power 3V. When SYNC GEN mode is on, turn off IC 12V power and LCD power supplies simultaneously.



System block diagram

Application Circuit

(RGB input or Y/color difference input, internal sync separation signal input, when using the internal VCO)

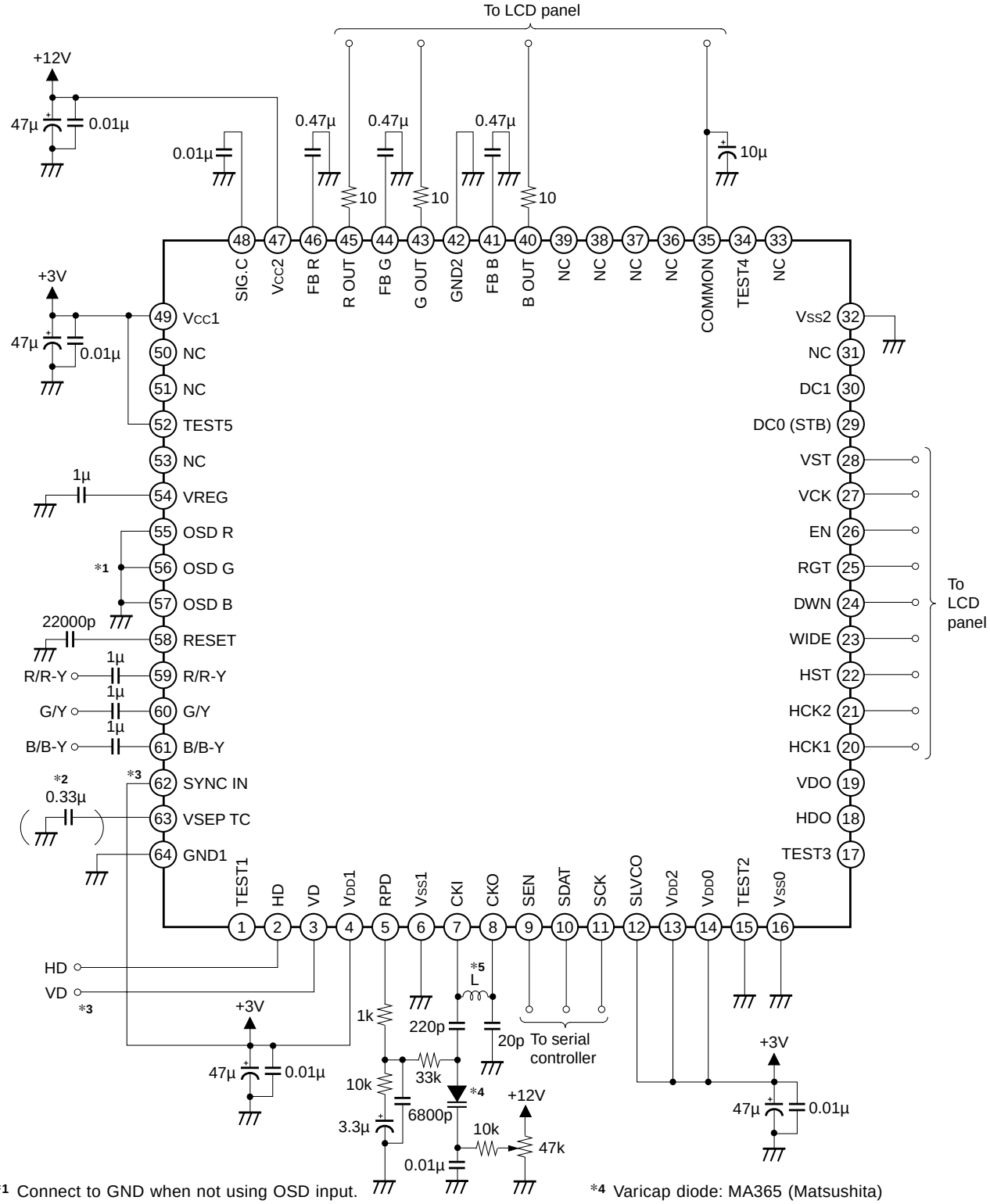


*1 Connect to GND when not using OSD input.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Application Circuit

(RGB input or Y/color difference input, external sync separation signal input, when using an external VCO)



*1 Connect to GND when not using OSD input.
*2 Eliminate (open) during external VD input.
*3 During external CSYNC input, connect Pin 3 to GND and Pin 62 to V_{DD}.
*4 Varicap diode: MA365 (Matsushita)
*5 L value: 113K pixels = 8.2µH
180K pixels = 3.9µH

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Notes on Operation

(1) The CXA3272R contains digital circuits, so the set board pattern must be designed in consideration of undesired radiation, interference to analog circuits, etc. Care should also be taken for the following items when designing the pattern.

- The digital and analog IC power supplies should be separated, but the GND and Vss should not be separated and a plain GND (Vss) pattern should be used in order to reduce impedance as much as possible. The power supplies should also use a plain pattern.
- Use ceramic capacitors for the by-pass capacitors between the power supplies and GND, and connect these capacitors as close to the pins as possible.
- The capacitors connected to Pin 35 should be located as close to the LCD panel as possible.
- The external PLL block (LPF/VCO) should be compact and located near the IC.

(2) The R/R-Y (Pin 59), G/Y (Pin 60), B/B-Y (Pin 61) and SYNC IN (Pin 62) pin input signals are clamped at the inputs using the capacitors connected to each pin, so these signals should be input at sufficiently low impedance.
(Input at an impedance of 1kΩ (max.) or less.)

(3) The smoothing capacitors connected to the RGB output DC level control feedback pins (Pins 41, 44 and 46) should have a leak current with a small absolute value and variance. Also, when using the pulse elimination (PAL display, WIDE display) function, a thorough evaluation of the picture quality should be made before deciding the capacitance values of the capacitors.

(4) A thorough study of whether the capacitor connected to the COM output pin satisfies the LCD panel specifications should be made before deciding the capacitance value.

(5) If this IC is used in connection with a circuit other than an LCD, it may cause that circuit to malfunction depending on the order in which power is supplied to the circuits. Thoroughly study the consequences of using this IC with other circuits before deciding on its use.

(6) Since this IC utilizes a CMOS structure, it may latch up due to excessive noise or power surge greater than the maximum rating of the I/O pins, or due to interface with the power supply of another circuit, or due to the order in which power is supplied to circuits. Be sure to take measures against the possibility of latch up.

(7) Do not apply a voltage higher than V_{DD} or lower than Vss to I/O pins.

(8) Do not use this IC under operating conditions other than those given.

(9) Absolute maximum rating values should not be exceeded even momentarily. Exceeding those ratings may damage the device, leading to eventual breakdown.

(10) This IC has a MOS structure which is easily damaged by static electricity, so thorough measures should be taken to prevent electrostatic discharge.

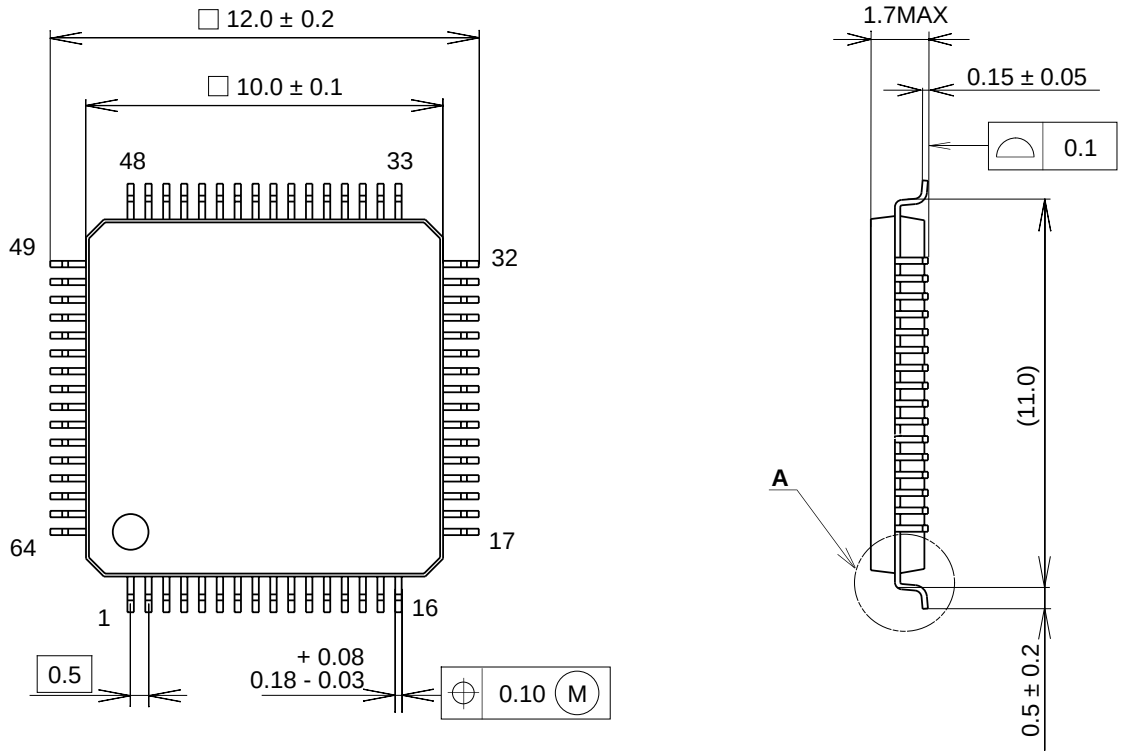
(11) Always connect the Vss0, Vss1, Vss2, GND1 and GND2 pins to the lowest potential applied to this IC; do not leave these pins open. The voltages applied to the power supply pins should be as follows.
Vss0, Vss1, Vss2 = GND1, GND2 ≤ V_{DD}0, V_{DD}1, V_{DD}2 = Vcc1 ≤ Vcc2.

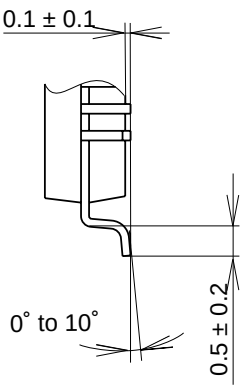
(12) Connecting damping resistor of 10kΩ to the R OUT, G OUT and B OUT outputs is recommended.

(13) The optimum L and C values of the external PLL block change according to the floating capacitance of the wiring pattern, so change these constants to match the circuit.

Package Outline Unit: mm

64PIN LQFP (PLASTIC)





DETAIL A

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.4g

SONY CODE	LQFP-64P-L321
EIAJ CODE	P-LQFP64P-10x10-0.5
JEDEC CODE	————

LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER PLATING	Sn-Bi Bi:1-4wt%
LEAD TREATMENT THICKNESS	5-18µm