

Pin List

Power/Ground

Pin Name	Pin Number	Descriptions
VccT	10, 20, 30, 40, 48, 70, 80	TTL power supply, should be connected to 3.3V \pm 5%
VEET	1, 11, 21, 31, 41, 71	TTL ground, connected to 0V
VccG	25, 32, 69, 76	Logical core power supply, connected to 3.3V \pm 5%
VEEG	26, 33, 68, 75	Logical core ground, connected to 0V
VccE	54	Serial driver power supply, connected to 3.3V \pm 5%
VEEE	51	Serial driver ground, connected to 0V
VccA	56	Analog power supply, connected to 3.3V \pm 5%
VEEA	57	Analog ground, connected to 0V
VEES	58	Analog substrate, connected to 0V

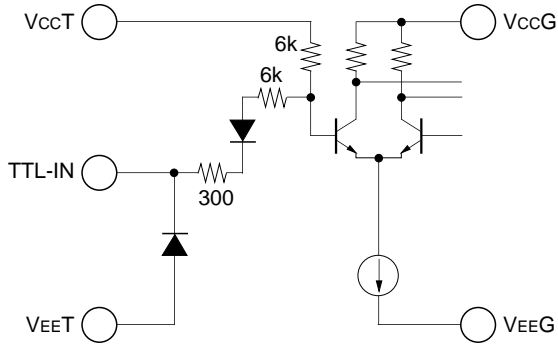
Digital Signals

Pin Name	Pin Number	Type	Descriptions
SFTCLK	72	TTL in	Shift clock, for the data fetch at rising or falling edge
RED1 (5 to 0) GRN1 (5 to 0) BLU1 (5 to 0)	14, 15, 16, 17, 18, 19 6, 7, 8, 9, 12, 13 78, 79, 2, 3, 4, 5	TTL in	Pixel data input in 1 pixel/sftclk mode 2nd pixel data input in 2 pixel/sftclk mode
RED0 (5 to 0) GRN0 (5 to 0) BLU0 (5 to 0)	42, 43, 44, 45, 46, 47 34, 35, 36, 37, 38, 39 22, 23, 24, 27, 28, 29	TTL in	Ignored in 1 pixel/sftclk mode 1st pixel data input in 2 pixel/sftclk mode
HSYNC	73	TTL in	Hsync data
VSYNC	74	TTL in	Vsync data
CNTL (3 to 0)	65, 66, 67, 77	TTL in	Control data
PANEL (1, 0)	62, 63	TTL in	Panel mode select switch
CKMODE	64	TTL in	Clock mode select switch
IDLE	49	TTL in	Idle mode select switch
SDATAP/N	52, 53	Tx	Serial Output & Refclk request input
REFREQ	50	TTL out	Refclk request detect flag

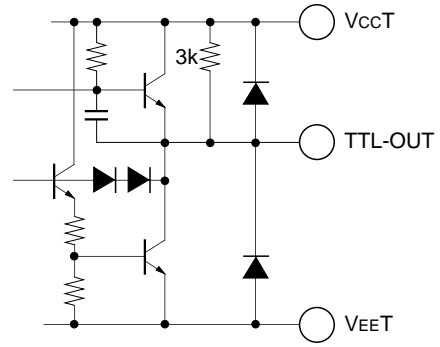
Special

Pin Name	Pin Number	Descriptions
TESTSB/DT	55, 61	SFTCLK polarity / TEST function control
LPFA/B	59, 60	External loop filter

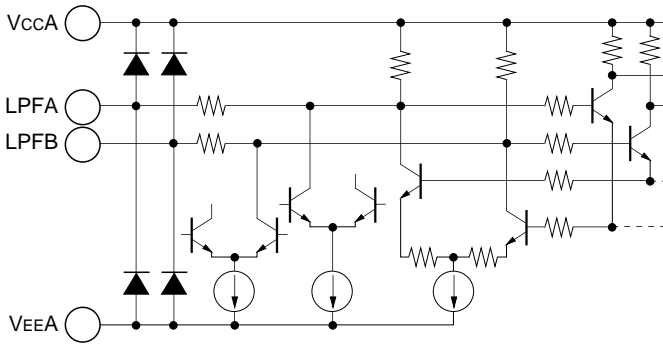
Equivalent I/O circuit



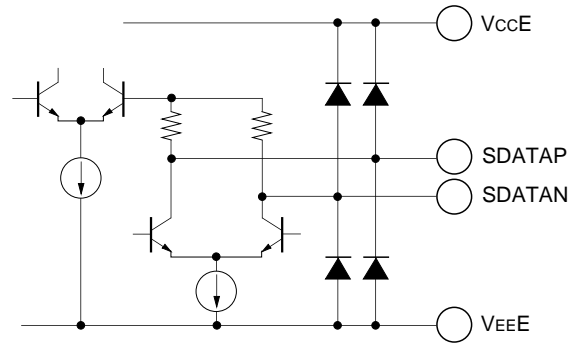
(a) TTL input equivalent circuit



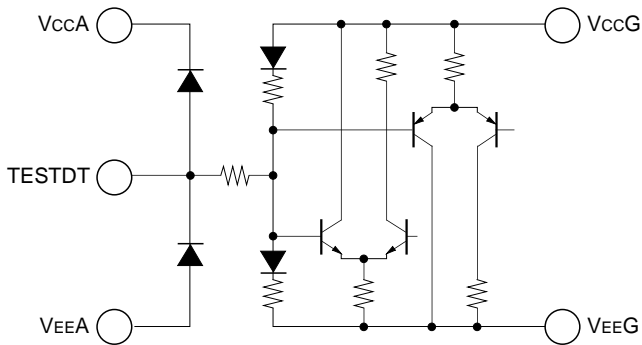
(b) TTL output equivalent circuit



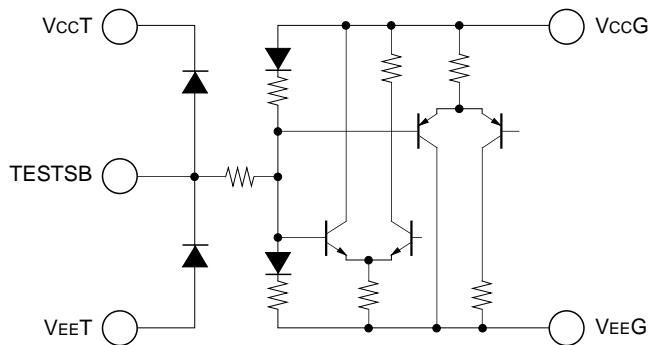
(c) LPFA/B equivalent circuit



(d) SDATAP/N equivalent circuit



(e) TESTDT equivalent circuit



(f) TESTSB equivalent circuit

Electrical characteristics

Tab. 1. Absolute Maximum Rating

Description	Symbol	Min.	Typ.	Max.	Unit	Comments
Power supply voltage	V _{CC}	-0.3		4	V	
TTL DC input voltage	V _{I_T}	-0.5		5.5	V	
TTL output current (High)	I _{OH_T}	-20		0	mA	
TTL output current (Low)	I _{OL_T}	0		20	mA	
Serial output pin voltage	V _{sdout}	-0.5		V _{CC} + 0.5	V	
Ambient temperature	T _a	-55		70	°C	Under bias
Storage temperature	T _{stg}	-65		150	°C	

Tab. 2. Recommended Operating Conditions

Description	Symbol	Min.	Typ.	Max.	Unit	Comments
Power supply voltage (Include V _{CC} T5)	V _{CC}	3.135	3.3	3.465	V	
Ambient temperature	T _a	0		70	°C	

Tab. 3. DC Characteristics (Under the recommended conditons. See Tab. 2)

Description	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input HIGH voltage (TTL)	V _{IH_T}	2		5.5	V	
Input LOW voltage (TTL)	V _{IL_T}	-0.5		0.8	V	
Input HIGH current (TTL)	I _{IH_T}			20	μA	V _{IN} = V _{CC}
Input LOW current (TTL)	I _{IL_T}	-400			μA	V _{IN} = 0
Output HIGH voltage (TTL)	V _{OH_T}	2.3			V	I _{OH} = -0.2mA
Output LOW voltage (TTL)	V _{OL_T}			0.4	V	I _{OL} = 4mA
Output HIGH current (SDATA)	I _{OH_SD}	-0.1	0	+0.1	mA	See Fig. 2
Output LOW current (SDATA)	I _{OL_SD}	14.7	16	17.3	mA	
Input HIGH voltage (SDATA)	V _{IH_SD}	V _{CC} - 0.6			V	Common mode voltage
Input LOW voltage (SDATA)	V _{IL_SD}			V _{CC} - 0.7	V	
Supply current	I _{CC}	165	215	265	mA	XGA, Outputs open SVGA/VGA, Outputs open
		175	225	275	mA	

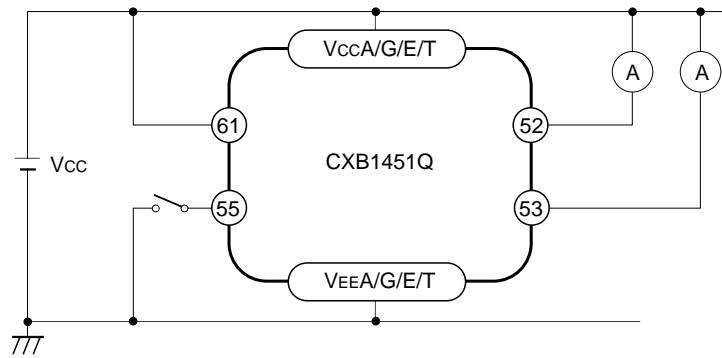


Fig. 2. IOH_SD and IOL_SD DC measurement

Tab. 4. AC Characteristics (Under the recommended conditons. See Tab. 5)

Description	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input TTL rise time	Tir	0.7		4.8	ns	0.8V to 2.0V
Input TTL fall time	Tir	0.7		4.8	ns	2.0V to 0.8V
SFTCLK frequency	Fsftclk	20.0	25.0	28.0	MHz	VGA, 1 pixel/sftclk mode
		10.0	12.5	14.0	MHz	VGA, 2 pixel/sftclk mode
		38.0	40.0	48.0	MHz	SVGA, 1 pixel/sftclk mode
		19.0	20.0	24.0	MHz	SVGA, 2 pixel/sftclk mode
		60.0	65.0	68.0	MHz	XGA, 1 pixel/sftclk mode
		30.0	32.5	34.0	MHz	XGA, 2 pixel/sftclk mode
SFTCLK duty factor	Dsftclk	40		60	%	Vth = 1.4V
Pixel/Sync/Cntl setup to SFTCLK	Tsetup	4.0			ns	XGA 1 pixel/sftclk mode @65MHz See Fig. 4
Pixel/Sync/Cntl hold to SFTCLK	Thold	1.0			ns	
SDATA rise time	Tor			400	ps	20 to 80%, CL = 2pF See Fig. 3
SDATA fall time	Tof			400	ps	
CLOCK mode assert time	TAclk		130		ns	
CLOCK mode deassert time	TDclk		10		ns	
IDLE mode assert time	TAidle		150		ns	
IDLE mode deassert time	TDidle		350		ns	
PLL lockin time	Tlockin		0.1		ms	

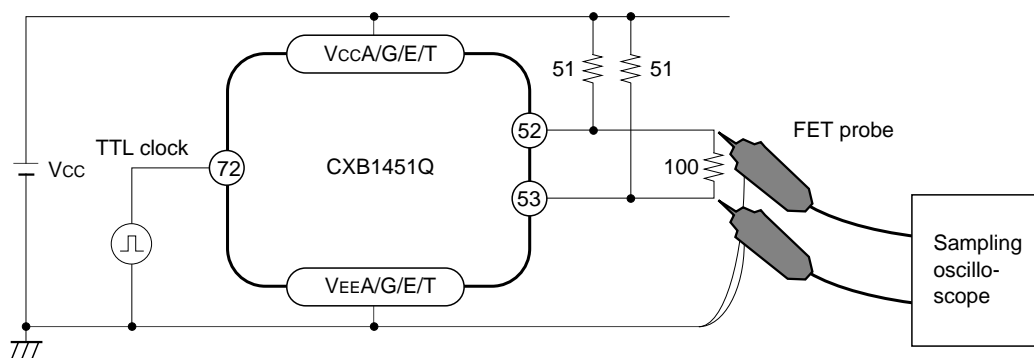


Fig. 3. SDATA waveform measurement

Timing Chart

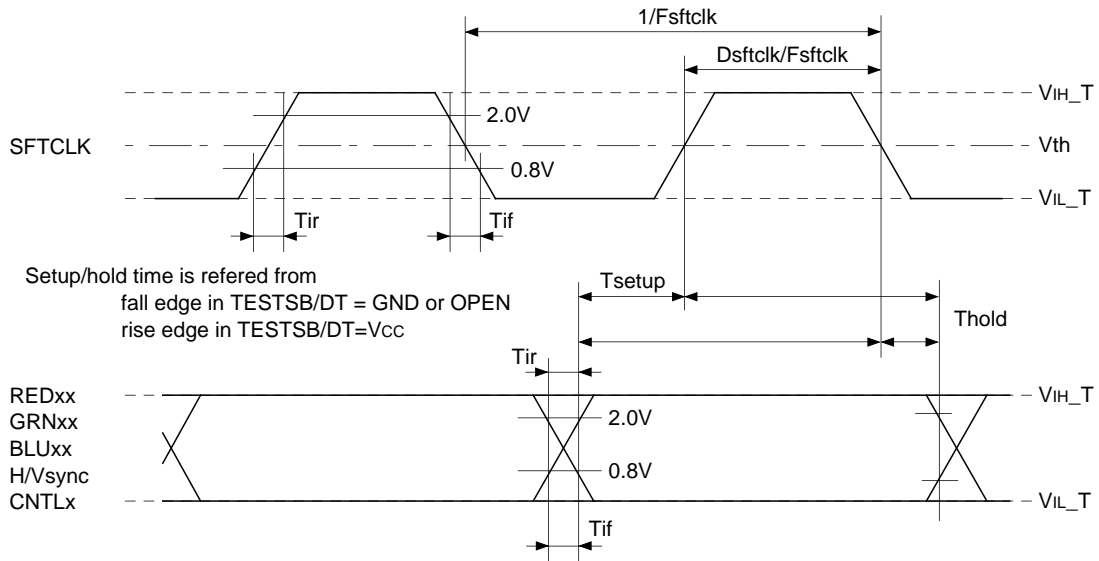


Fig. 4. TTL input timing

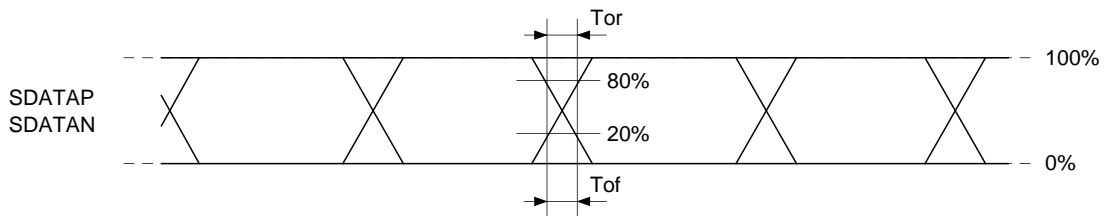


Fig. 5. Serial output timing

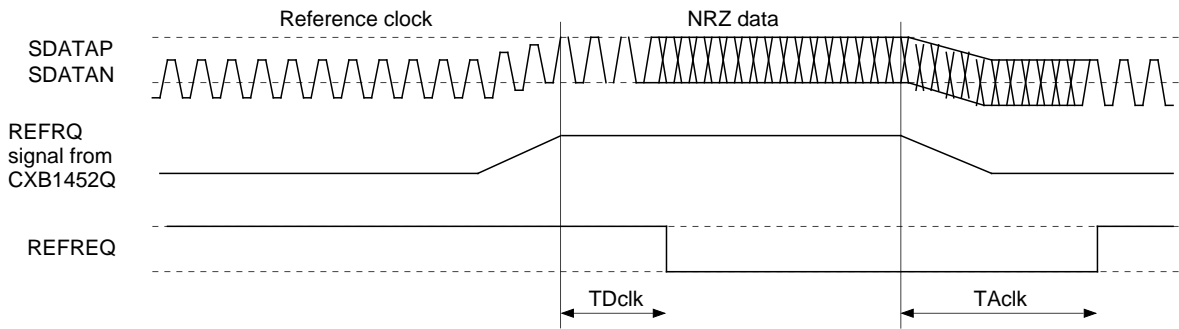


Fig. 6. Refclk request timing

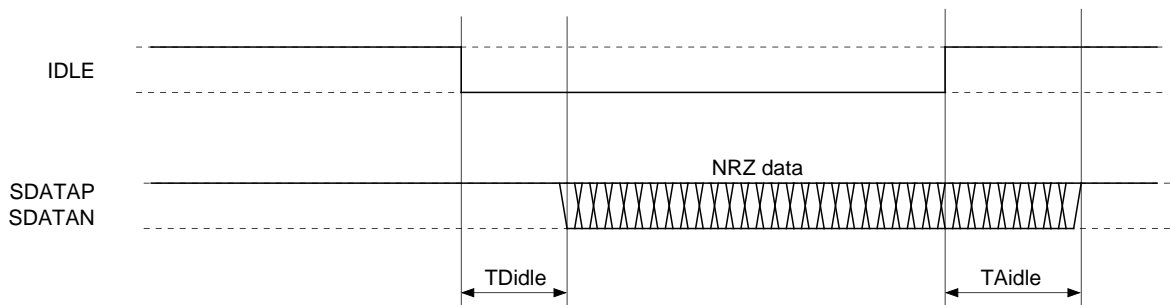


Fig. 7. Idle mode timing

Operation mode

CXB1451Q supports 3 panel mode and 2 clock mode switched by the PANEL (1, 0) and CKMODE pin according to the Tab. 5 & 6. The supporting clock rate are summarized in Tab. 7. These pins are open High TTL inputs.

Tab. 5. Panel Mode select

PANEL1	PANEL0	Supporting panel size & color
L	L	VGA (640 × 480) 18bit color
L	H	SVGA (800 × 600) 18bit color
H	L	XGA (1024 × 768) 18bit color
H	H	not supported

Tab. 6. Clock Mode select

CKMODE	Supporting clock mode
L	2 pixel/ShiftClock (2ppc)
H	1 pixel/ShiftClock (1ppc)

Tab. 7. Operation Mode

Panel Mode	Clock Mode	Color	Shift Clock	Dot Clock	Serial rate
VGA	1 pixel/SftClk	18bit	25MHz	25MHz	600Mbps
	2 pixel/SftClk	18bit	12.5MHz	25MHz	600Mbps
SVGA	1 pixel/SftClk	18bit	40MHz	40MHz	960Mbps
	2 pixel/SftClk	18bit	20MHz	40MHz	960Mbps
XGA	1 pixel/SftClk	18bit	65MHz	65MHz	1560Mbps
	2 pixel/SftClk	18bit	32.5MHz	65MHz	1560Mbps

TESTSB/TESTDT pins select the trigger edge of SFTCLK and test mode according to Tab. 8.

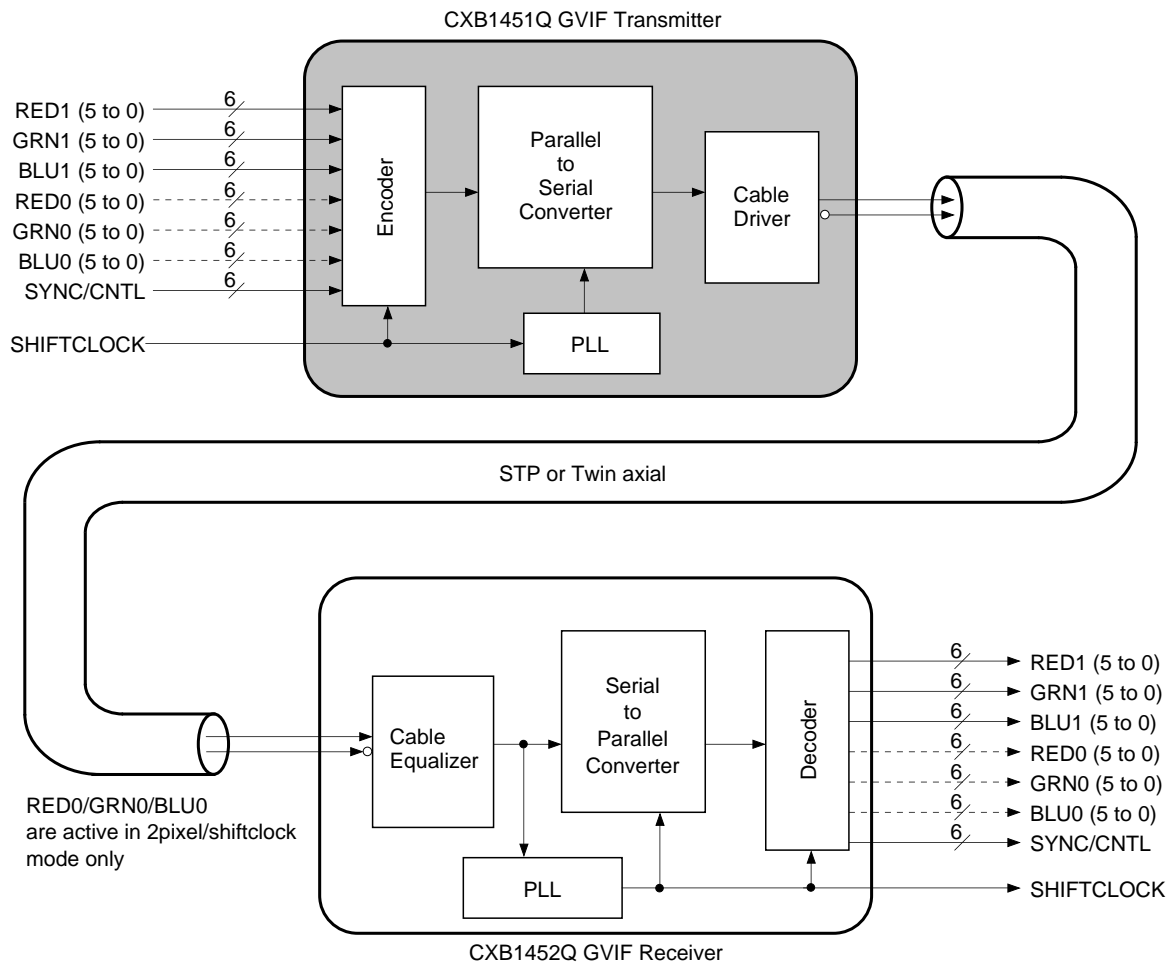
Tab. 8. SFTCLK polarity & TEST mode

		TESTSB		
		GND	OPEN	Vcc
TESTDT	GND	Transmitter operation trigger = falling edge		Fabricator reserved TEST mode
	OPEN			
	Vcc	SDATAP = H SDATAN = L	SDATAP = L SDATAN = H	Trigger = rising edge

IDLE pin disable differential signal transmission from SDATAP/N pins. It's open High TTL input. Transmission is disabled when IDLE = High.

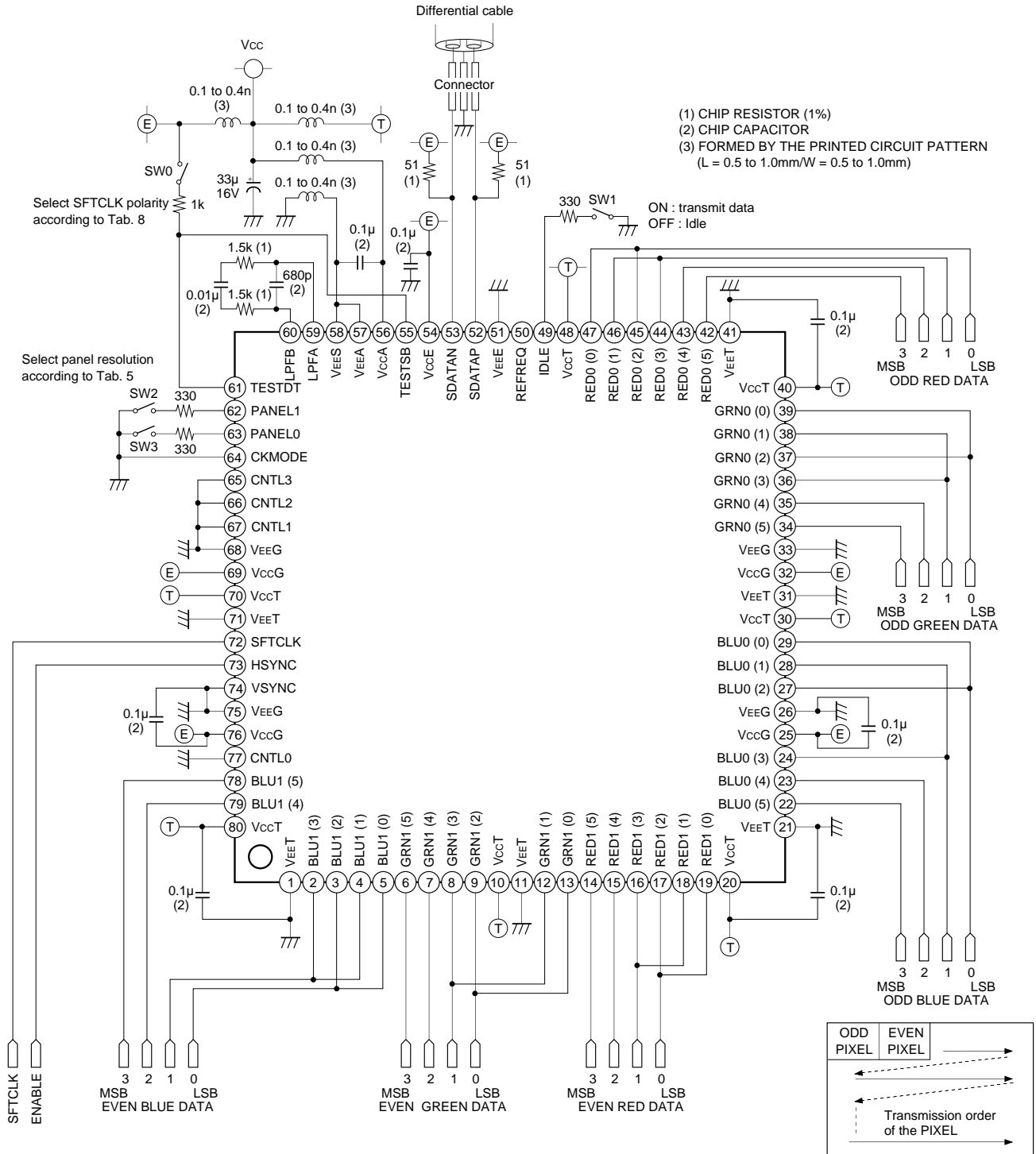
Applications

CXB1451Q GVIF transmitter is applied to the digital RGB signal transmission for
 P/C with LCD monitor
 Video on demand system
 Monitoring system
 Graphical controller
 Projector
 Digital TV monitor
 with GVIF receiver, CXB1452Q.



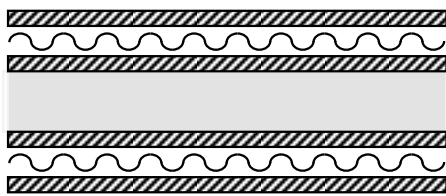
Application Circuit (B)

Clock mode: 2 pixel/sftclk
 Picture sync: ENABLE only
 Color depth: 12bit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Recommended Printed Circuit Board Structure



- L1: Cu plate (18µm) + solder coat
- I1: Adhesive Sheet (0.3mm ± 0.09mm)
- L2: Cu plate (36µm)
- I2: Fiber-glass epoxy core (0.8mm)
- L3: Cu plate (36µm)
- I3: Adhesive Sheet (0.3mm)
- L4: Cu plate (18µm) + solder coat

Recommended Printed Circuit Board Pattern

SDATAP/SDATAN pins to the connector path
other path

W = 0.50mm (Z0 = 50Ω)

W = 0.25mm

POWER and special signal routing example

