SONY

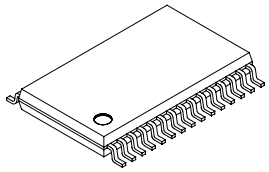
CXB1595AN

Fibre Channel Repeater

Description

The CXB1595AN is a clock and data recovery IC for fibre channel 1.0625Gbaud with a built-in PLL. This IC incorporates a port bypass circuit and is suitable for disk array and FC-AL HUB, etc.

30 pin SSOP (Plastic)



Structure

Bipolar silicon monolithic IC

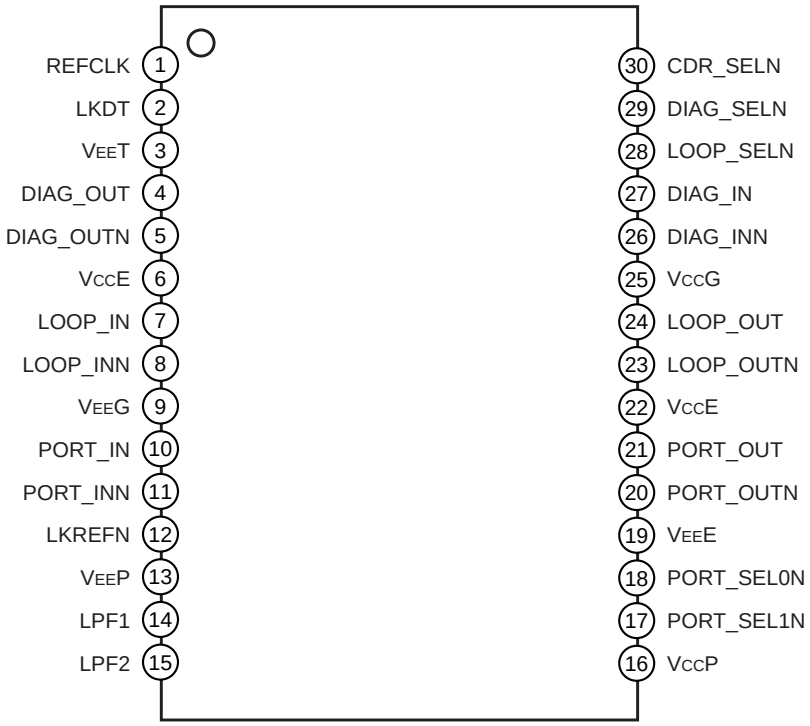
Features

- Conforms to ANSI X3T11 Fibre Channel standard
- Single 3.3V power supply
- Low power consumption: 380mW (Typ.)
- Low jitter
- PLL lock detection circuit
- Port bypass circuit
- Small plastic package (30-pin SSOP)

Applications

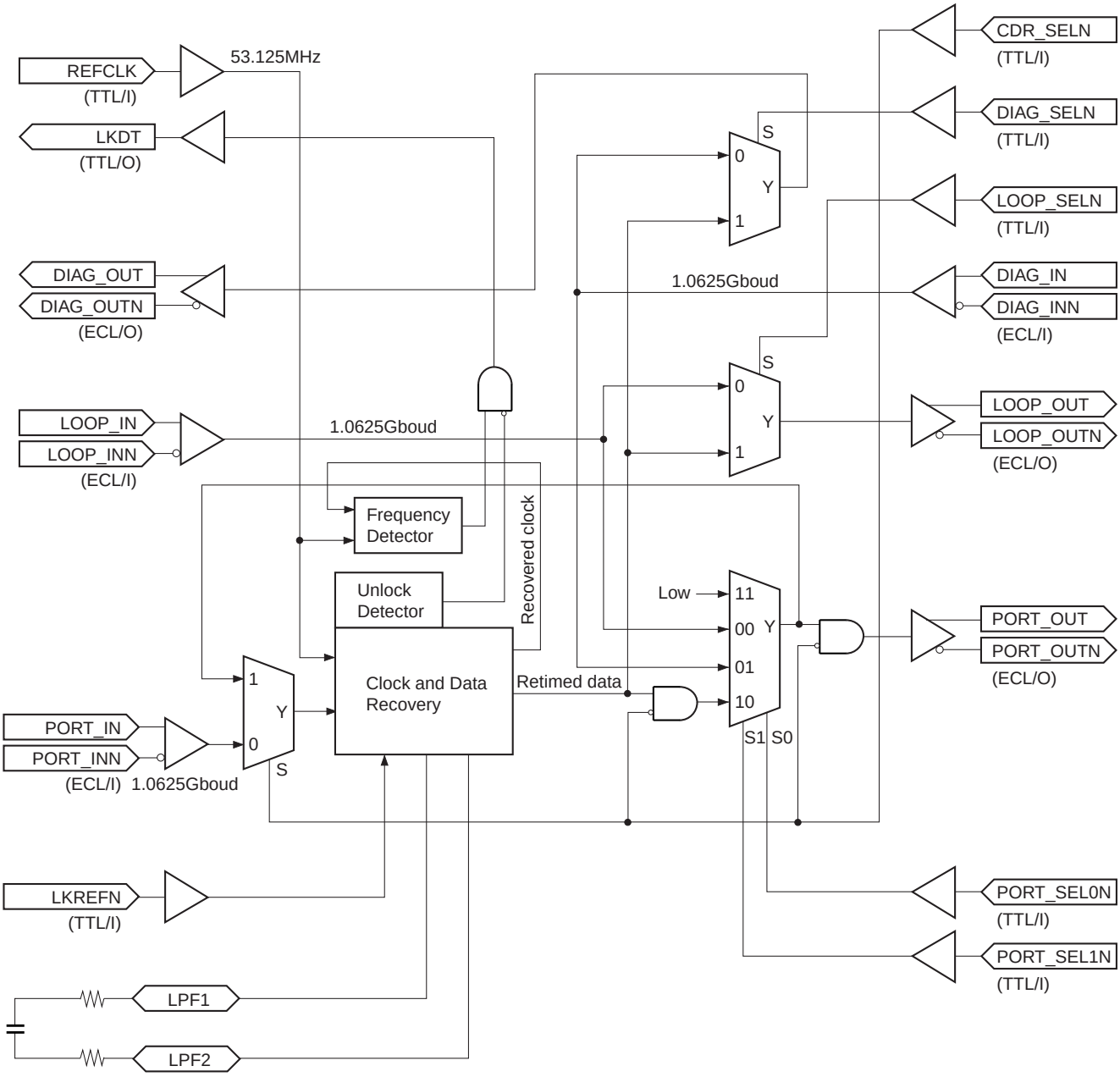
- Fibre channel arbitrated loop 1.0625Gbaud HUB
- Disk array

Pin Configuration

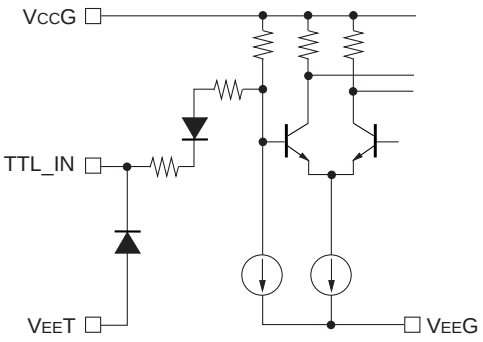
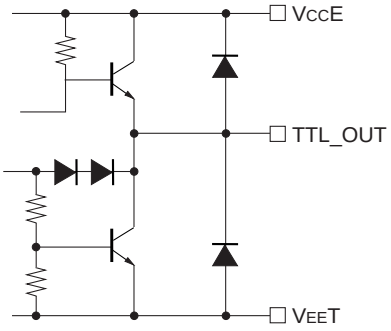
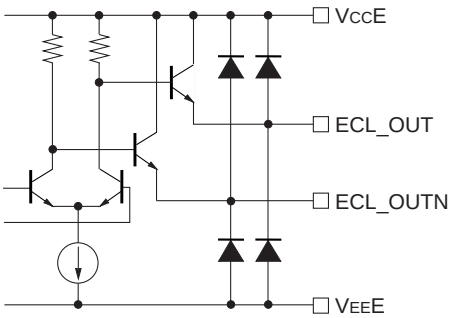
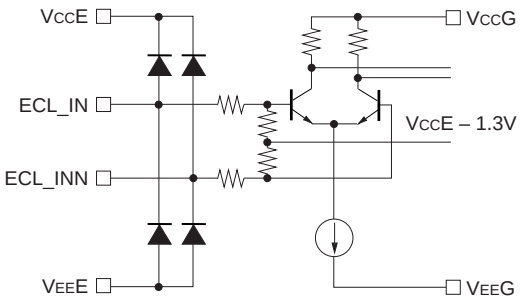


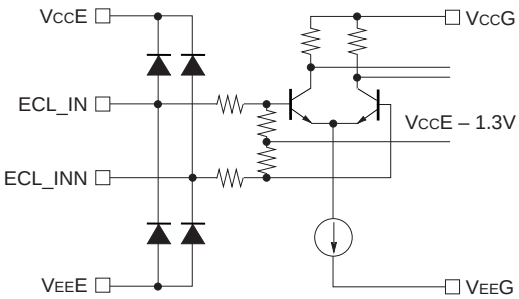
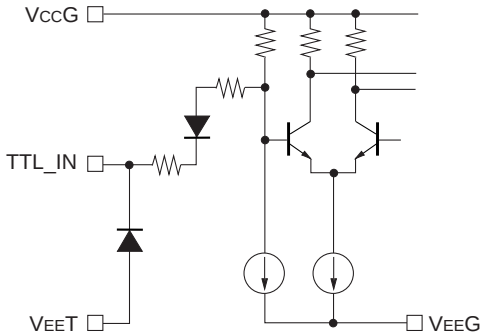
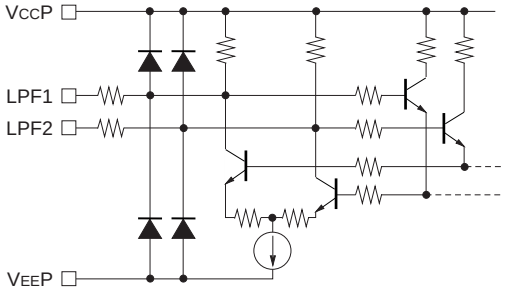
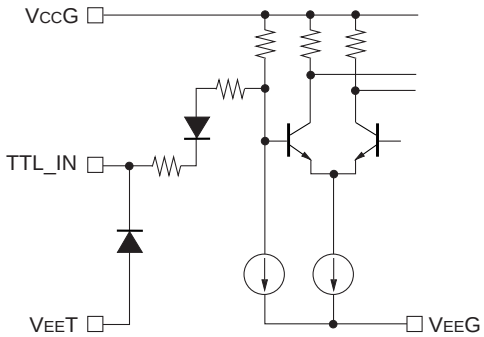
E99632-PS

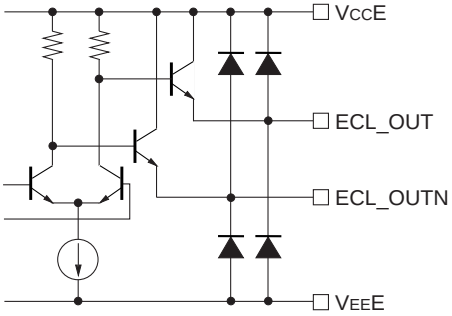
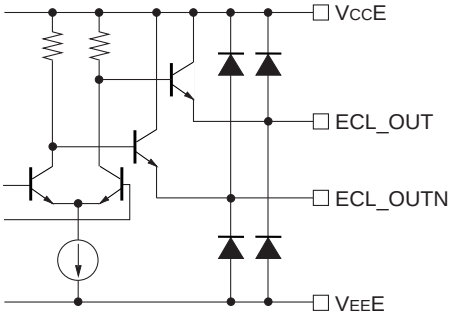
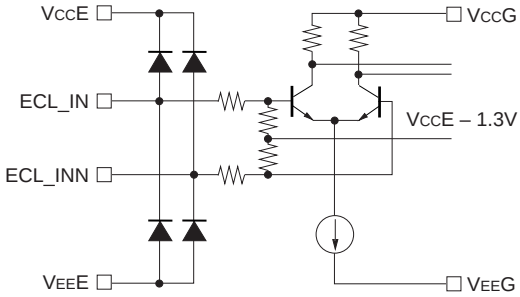
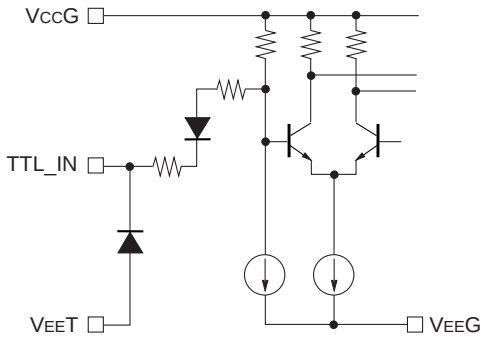
Block Diagram



Pin Description

Pin No.	Symbol	Type	Equivalent circuit	Description
1	REFCLK	Input TTL		Reference clock. This pin is used for the PLL to take the frequency. Input 53.125MHz to this pin.
2	LKDT	Output TTL		PLL lock detection signal output. Outputs high level when PLL is locked to the serial data. Outputs low level when LKREFN is in the low level or the serial data isn't locked to the serial input data.
3	VEET	Ground		Ground for TTL I/O: 0V.
4 5	DIAG_OUT DIAG_OUTN	Output ECL		Differential serial data output.
6	VCCE	Power supply		Power supply for ECL I/O: 3.3V ± 5%.
7 8	LOOP_IN LOOP_INN	Input ECL		Differential serial data input.

Pin No.	Symbol	Type	Equivalent circuit	Description
9	$V_{EE}G$	Ground		Ground for internal logic Gate: 0V.
10 11	PORT_IN PORT_INN	Input ECL		Differential serial data input.
12	LKREFN	Input TTL		Lock to reference. An active low input. LKREFN causes the PLL lock to the REFCLK.
13	$V_{EE}P$	Ground		Ground for PLL: 0V.
14 15	LPF1 LPF2	External circuit node		Connect to external loop filter.
16	$V_{CC}P$	Power supply		Power supply for PLL: 3.3V ± 5%.
17 18	PORT_SEL1N PORT_SEL0N	Input TTL		Selection for PORT_OUT.

Pin No.	Symbol	Type	Equivalent circuit	Description
19	$V_{EE}E$	Ground		Ground for ECL I/O: 0V.
20 21	PORT_OUTN PORT_OUT	Output ECL		Differential serial data output.
22	$V_{CC}E$	Power supply		Power supply for ECL I/O: 3.3V ± 5%.
23 24	LOOP_OUTN LOOP_OUT	Output ECL		Differential serial data output.
25	$V_{CC}G$	Power supply		Power supply for internal logic gate: 3.3V ± 5%.
26 27	DIAG_INN DIAG_IN	Input ECL		Differential serial data input.
28	LOOP_SELN	Input TTL		Selection for LOOP_OUT. See table 9.
29	DIAG_SELN			Selection for DIAG_OUT. See table 9.
30	CDR_SELN			Selection for CDR input. See table 9.

Electrical Characteristics

Table 1. Absolute Maximum Ratings ($V_{EE}E$, $V_{EE}T$, $V_{EE}G$, $V_{EE}P$ = GND)

Item	Symbol	Min.	Typ.	Max.	Unit	Comments
Power supply voltage	V_{CC}	–0.3		4	V	
TTL DC input voltage	V_I_T	–0.5		5.5	V	
ECL DC input voltage	V_I_E	V_{CC} – 2		V_{CC}	V	
ECL input voltage between differential signal	I_I_E	–4		4	V	
TTL output current (High)	I_{OH}_T	–20		0	mA	
TTL output current (Low)	I_{OL}_T	0		20	mA	
ECL output current	I_O_E	–30		0	mA	
Storage temperature	Tstg	–65		150	°C	

Table 2. Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Comments
Power supply voltage	V_{CC}	3.135	3.3	3.465	V	
Ambient temperature	Ta	0		70	°C	

Table 3. DC Characteristics (Over recommended operating conditions)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input high voltage (TTL)	V_{IH}_T		2.8		5.5	V
Input low voltage (TTL)	V_{IL}_T		0		0.8	V
Input high current (TTL)	I_{IH}_T	$V_{IN} = V_{CC}$			20	µA
Input low current (TTL)	I_{IL}_T	$V_{IN} = 0$	–400			µA
Output high voltage (TTL)	V_{OH}_T	I_{OH} = –0.4mA	2.2		V_{CC}	V
Output low voltage (TTL)	V_{OL}_T	I_{OL} = 2mA	0		0.5	V
Differential input voltage swing	V_{IS}_E	AC coupling input	200		1000	mV
Differential output voltage peak-to-peak	V_{OS}_E	50Ω to Vcc – 2V	1200		2000	mV
Supply current	I_{CC}	Outputs open			154	mA
Power dissipation	P_D	Outputs open			534	mW

Table 4. AC Characteristics (Over recommended operating conditions)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input TTL rise time of REFCLK	Tir_RC	0.8 to 2.0V			4.8	ns
Input TTL fall time of REFCLK	Tif_RC	2.0 to 0.8V			4.8	ns
Output TTL rise time	Tor_T	0.8 to 2.0V, CL = 10pF			3.5	ns
Output TTL fall time	Tof_T	2.0 to 0.8V, CL = 10pF			3.5	ns
Output ECL rise time	Tor_E	20 to 80%, CL = 2pF			400	ps
Output ECL fall time	Tof_E	20 to 80%, CL = 2pF			400	ps
Serial data rate	SDR	1.0UI = 941ps		1062.5		MBd
REFCKL frequency tolerance	RC_TOL	53.125MHz REFCLK	–100		100	PPM
REFCKL duty cycle tolerance	RC_DC				10	%
Total Jitter tolerance peak-to-peak, 10E-12BER	TJT	*1	0.7			UI
Deterministic jitter output peak-to-peak	DJgen	±K28.5 serial data, 637kHz HPF *1			0.07	UI
Random jitter output, rms	RJgen	00110011 serial data, 637kHz HPF *1			0.0125	UIrms
Jitter transfer peaking	JXFR_PK	00110011 input *1			0.2	dB
Jitter transfer 3dB bandwidth	JXFR_3dB	00110011 input *1		640		kHz
Bit sync time	Tbs	FC Idle pattern *1, *2			2500	bit
Frequency acquisition time	Tfa	*1			800	µs
Lock detect range	LDR	Frequency difference between recovered Clock and REFCLK	–2		2	%

*1 The values of LPF R/2 is 200Ω and LPF C is 0.022µF.

*2 CXB1595AN starts Bit synchronization in 10µs after LKREFN changed to high.

Table 5. Function of LOOP_OUT

LOOP_SELN	LOOP_OUT
H	Recovered Data
L	LOOP_IN

Table 6. Function of DIAG_OUT

DIAG_SELN	DIAG_OUT
H	Recovered Data
L	DIAG_IN

Table 7. Function of PORT_OUT

PORT_SEL0N	PORT_SEL1N	PORT_OUT
H	H	Low
L	H	Recovered Data
H	L	DIAG_IN
L	L	LOOP_IN

Table 8. Function of Recovered data

PORT_SEL0N	PORT_SEL1N	CDR_SELN	Recovered Data
H	H	H	Low
L	H	H	—
H	L	H	DIAG_IN
L	L	H	LOOP_IN
H	H	L	PORT_IN
L	H	L	PORT_IN
H	L	L	PORT_IN
L	L	L	PORT_IN

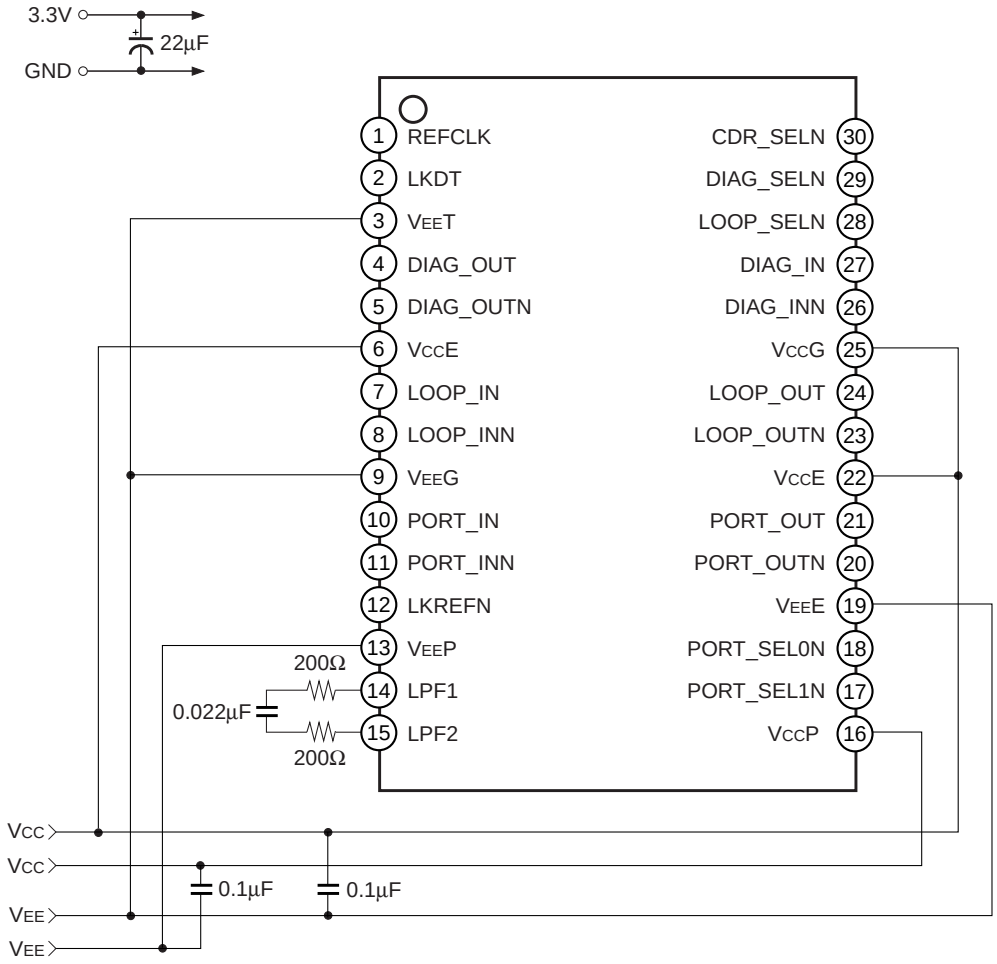
Table 9. Selection of Signal

PORT_SEL0N	PORT_SEL1N	LOOP_SELN	DIAG_SELN	CDR_SELN	PORT_OUT	LOOP_OUT	DIAG_OUT
1	1	1	1	1	Low	Low	Low
0	1	1	1	1	Low	Low	Low
1	0	1	1	1	Low	**DIAG_IN**	**DIAG_IN**
0	0	1	1	1	Low	**LOOP_IN**	**LOOP_IN**
1	1	0	1	1	Low	LOOP_IN	Low
0	1	0	1	1	Low	LOOP_IN	Low
1	0	0	1	1	Low	LOOP_IN	**DIAG_IN**
0	0	0	1	1	Low	LOOP_IN	**LOOP_IN**
1	1	1	0	1	Low	Low	DIAG_IN
0	1	1	0	1	Low	Low	DIAG_IN
1	0	1	0	1	Low	**DIAG_IN**	DIAG_IN
0	0	1	0	1	Low	**LOOP_IN**	DIAG_IN
1	1	0	0	1	Low	LOOP_IN	DIAG_IN
0	1	0	0	1	Low	LOOP_IN	DIAG_IN
1	0	0	0	1	Low	LOOP_IN	DIAG_IN
0	0	0	0	1	Low	LOOP_IN	DIAG_IN
1	1	1	1	0	Low	**PORT_IN**	**PORT_IN**
0	1	1	1	0	**PORT_IN**	**PORT_IN**	**PORT_IN**
1	0	1	1	0	DIAG_IN	**PORT_IN**	**PORT_IN**
0	0	1	1	0	LOOP_IN	**PORT_IN**	**PORT_IN**
1	1	0	1	0	Low	LOOP_IN	**PORT_IN**
0	1	0	1	0	**PORT_IN**	LOOP_IN	**PORT_IN**
1	0	0	1	0	DIAG_IN	LOOP_IN	**PORT_IN**
0	0	0	1	0	LOOP_IN	LOOP_IN	**PORT_IN**
1	1	1	0	0	Low	**PORT_IN**	DIAG_IN
0	1	1	0	0	**PORT_IN**	**PORT_IN**	DIAG_IN
1	0	1	0	0	DIAG_IN	**PORT_IN**	DIAG_IN
0	0	1	0	0	LOOP_IN	**PORT_IN**	DIAG_IN
1	1	0	0	0	Low	LOOP_IN	DIAG_IN
0	1	0	0	0	**PORT_IN**	LOOP_IN	DIAG_IN
1	0	0	0	0	DIAG_IN	LOOP_IN	DIAG_IN
0	0	0	0	0	LOOP_IN	LOOP_IN	DIAG_IN

* Boldface type is recovered data.

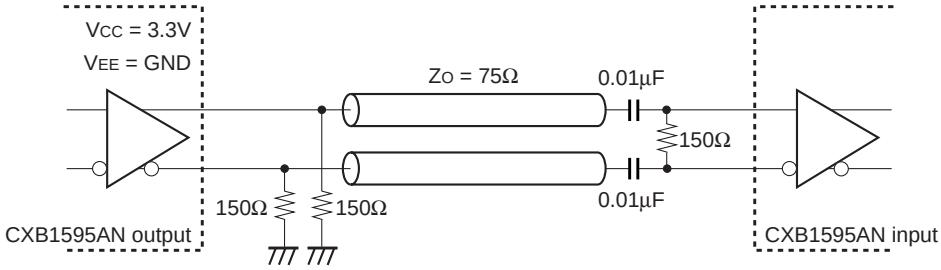
Application Circuit

1. Power and loop filter



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

2. Serial input and output



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Description of Operation

1. Clock and data recovery

The PLL in the clock and data recovery block must be frequency locked to the external REFCLK before locking to the data.

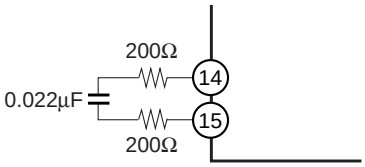
The LKREFN pin is used to lock the frequency. When the LKREFN pin is low, the PLL frequency is locked to the external REFCLK and when high, it is locked to the input serial data. Up to 800µs is required to lock the frequency.

2. Frequency detector

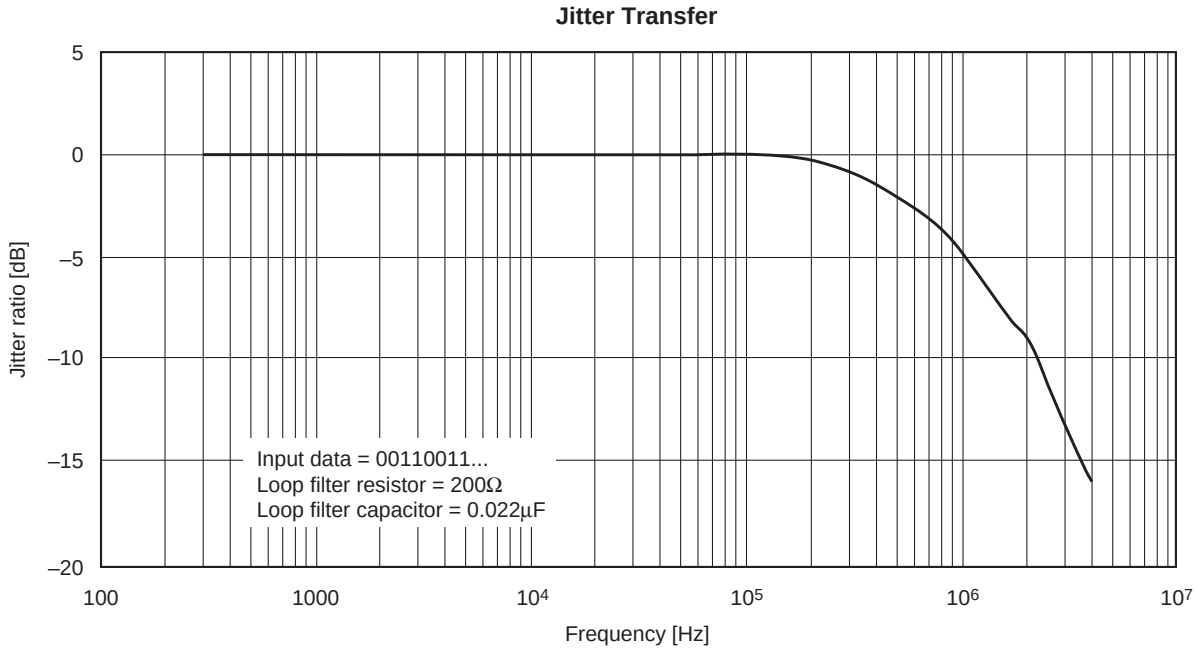
The frequency detector constantly monitors the offset between the clock obtained by 1/20 frequency-dividing the recovered clock and the external REFCLK. It outputs high when this offset is less than 1.6%, and low when this offset is 1.6% or more.

Note on Operation

The following values are recommended for the external resistors and capacitor used as the loop filter.

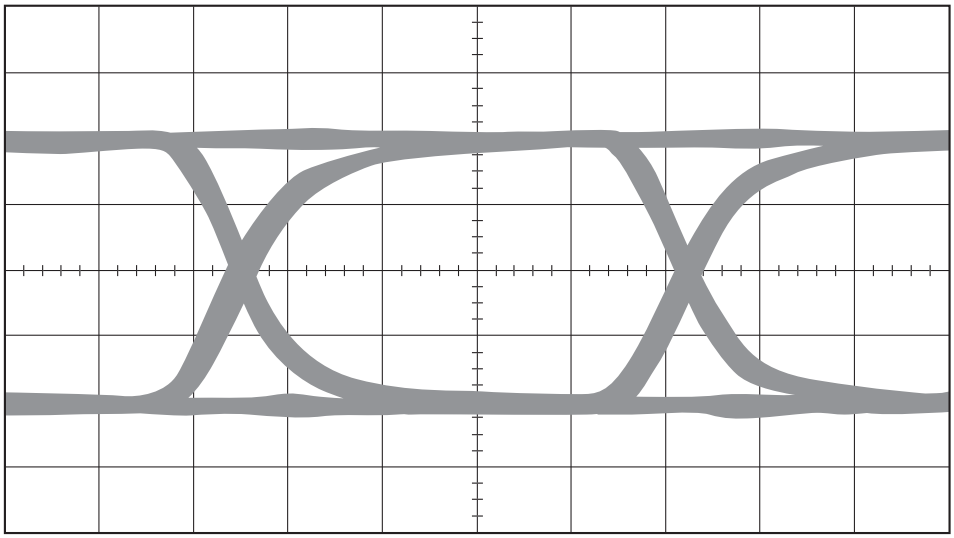


Example of Jitter Transfer Measurement



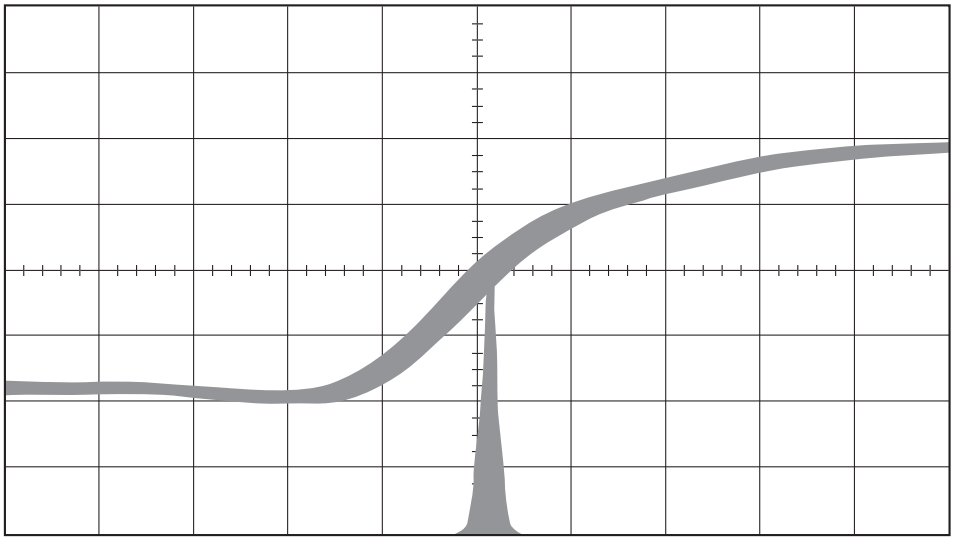
Example of Representative Characteristics

PORT-OUT Output Eye Pattern
(1.0625Gbps Retimed data)



X: 200ps/div
Y: 200mV/div

Example of Random Jitter Measurement

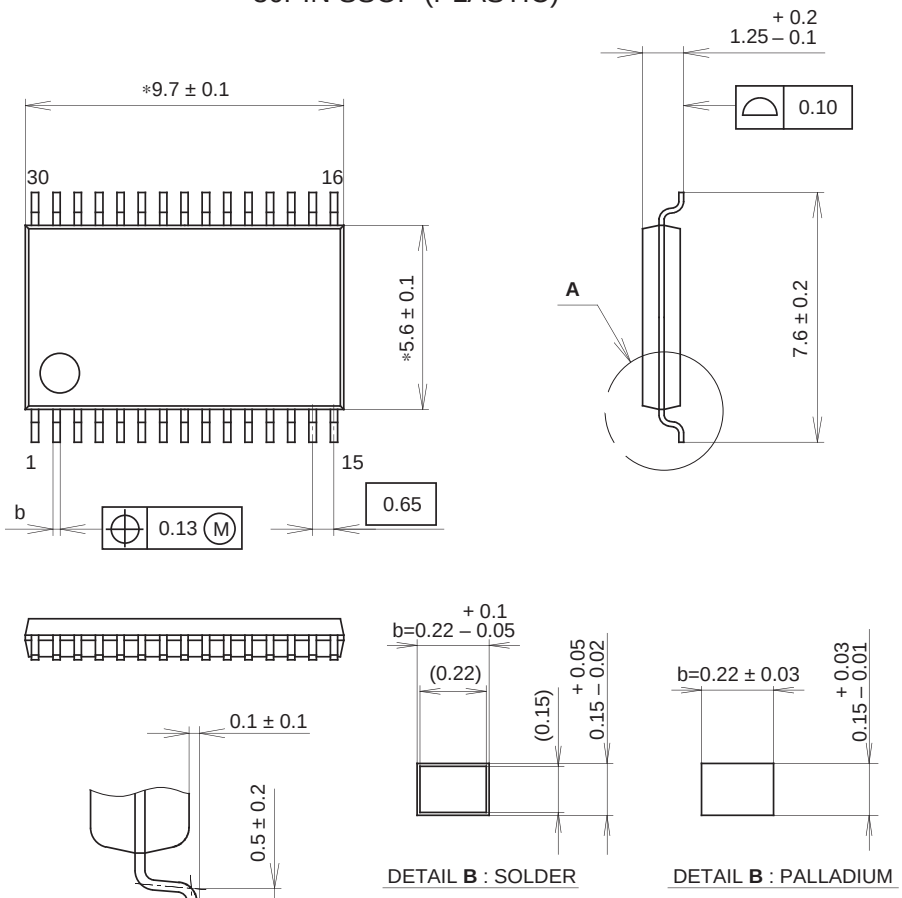


X: 100ps/div
Y: 200mV/div

Input data = 010101...
Random Jitter = 9.1ps (rms)

Package Outline Unit: mm

30PIN SSOP (PLASTIC)



NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	SSOP-30P-L01
EIAJ CODE	SSOP030-P-0056
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.1g