

February 1996

8-Bit, 40 MSPS High Speed D/A Converter

Features

- 40 MSPS Throughput Rate
- 8-Bit Resolution
- 0.25 LSB Integral Linearity Error
- Low Glitch Noise
- Single +5V Supply Operation
- Low Power Consumption 80mW (Max)

Applications

- Wireless Telecommunications
- NTSC, PAL, or SECAM
- Signal Reconstruction
- Direct Digital Synthesis
- Imaging
- Presentation and Broadcast Video
- Graphics Displays
- Signal Generators

Description

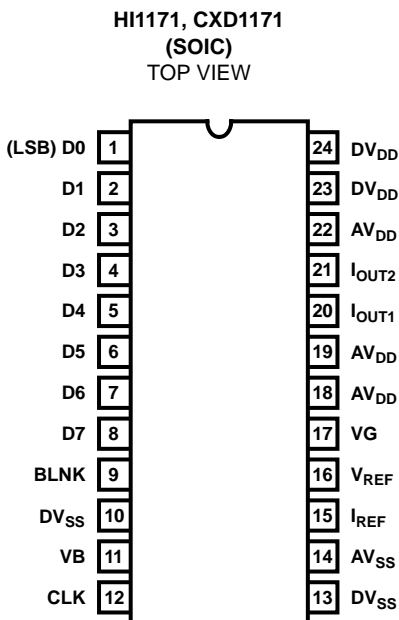
The HI1171, CXD1171 is an 8-bit 40MHz high speed D/A converter. The converter incorporates an 8-bit input data register with blanking capability, and current outputs. The HI1171, CXD1171 features low glitch outputs. The architecture is a current cell arrangement to provide low linearity errors.

The HI1171, CXD1171 is available in a Commercial temperature range and is offered in a 24 lead (200 mil) SOIC plastic package.

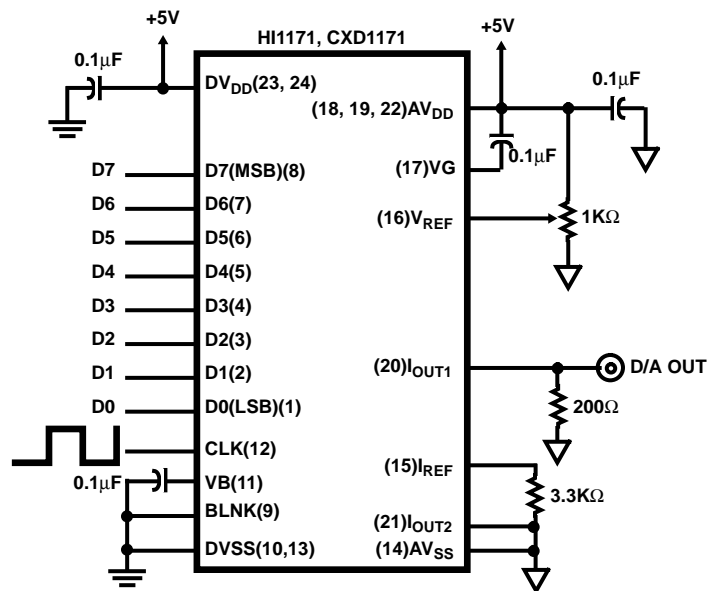
Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI1171JCB, CXD1171M	-20°C to 75°C	24 Lead Plastic SOIC (200 mil)

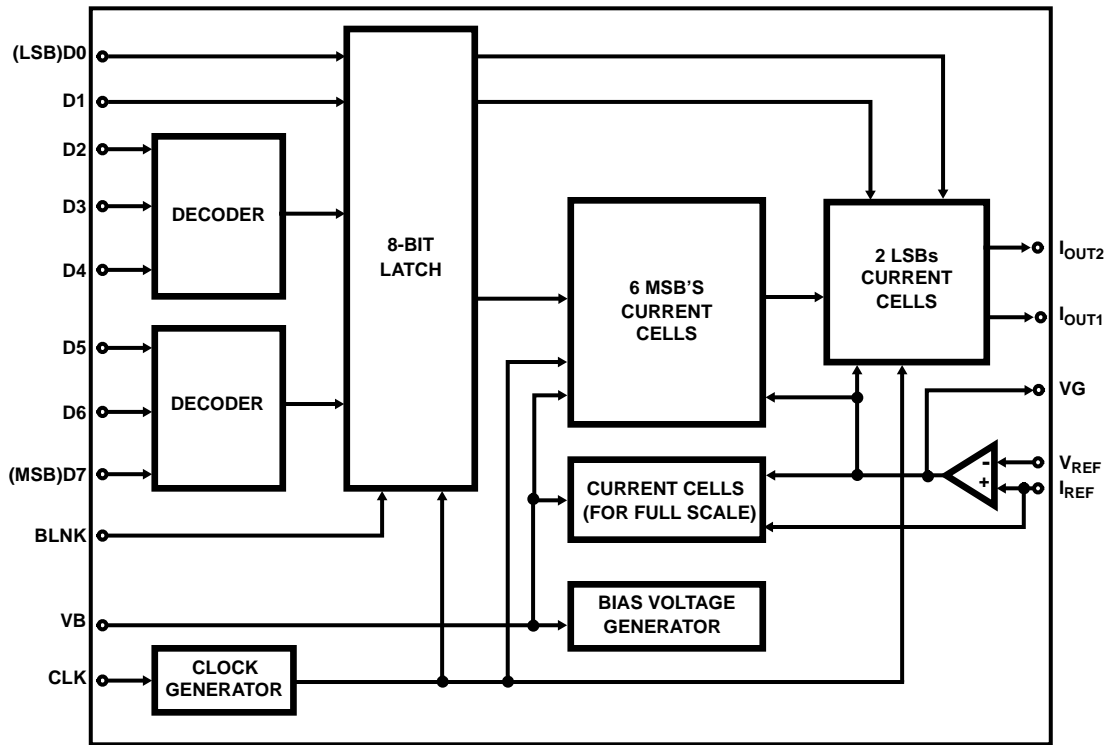
Pinout



Typical Applications Circuit



Functional Block Diagram



AV_{DD} AV_{SS} DV_{DD} DV_{SS}

Specifications HI1171, CXD1171

Absolute Maximum Ratings

Digital Supply Voltage DV_{DD} to DV_{SS} +7.0V
 Analog Supply Voltage AV_{DD} to AV_{SS} +7.0V
 Input Voltage V_{DD} to V_{SS} V
 Output Current 0mA to 15mA
 Storage Temperature Range -65°C to +150°C
 Lead Temperature (Soldering 10s)(Lead Tips Only) +300°C

Thermal Information

Thermal Resistance (Typ, Note 1) θ_{JA}
 SOIC Package 98°C/W
 Maximum Power Dissipation
 HI1171JCB, CXD1171M 160mW
 Operating Temperature Range -20°C to +75°C
 Junction Temperature +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $AV_{DD} = +4.75$ to $+5.25V$, $DV_{DD} = +4.75$ to $+5.25V$, $V_{REF} = +2.0V$, $f_S = 40MHz$,
 CLK Pulse Width = 12.5ns, $T_A = +25^\circ C$ (Note 4).

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
SYSTEM PERFORMANCE					
Resolution		8	-	-	Bits
Integral Linearity Error, INL	$f_S = 40MHz$ (End Point)	-0.5	-	1.3	LSB
Differential Linearity Error, DNL	$f_S = 40MHz$	-	-	± 0.25	LSB
Offset Error, V_{OS}	(Note 2)	-	-	0.125	LSB
Full Scale Error, FSE (Adjustable to Zero)	(Note 2)	-	-	± 13	LSB
Full Scale Output Current, I_{FS}		-	10	15	mA
Full Scale Output Voltage, V_{FS}		1.9	2.0	2.1	V
Output Voltage Range, V_{FSR}		0.5	2.0	2.1	V
DYNAMIC CHARACTERISTICS					
Throughput Rate	See Figure 7	40.0	-	-	MSPS
Glitch Energy, GE	$R_{OUT} = 75\Omega$	-	30	-	pV-s
Differential Gain, ΔA_V (Note 3)		-	1.2	-	%
Differential Phase, $\Delta\phi$ (Note 3)		-	0.5	-	Degree
REFERENCE INPUT					
Voltage Reference Input Range		0.5	-	2.0	V
Reference Input Resistance	(Note 3)	1.0	-	-	M Ω
DIGITAL INPUTS					
Input Logic High Voltage, V_{IH}	(Note 3)	3.0	-	-	V
Input Logic Low Voltage, V_{IL}	(Note 3)	-	-	1.5	V
Input Logic Current, I_{IL} , I_{IH}	(Note 3)	-	-	± 5.0	μA
Digital Input Capacitance, C_{IN}	(Note 3)	-	5.0	-	pF
TIMING CHARACTERISTICS					
Data Setup Time, t_{SU}	See Figure 1	5	-	-	ns
Data Hold Time, t_{HLD}	See Figure 1	10	-	-	ns
Propagation Delay Time, t_{PD}	See Figure 9	-	10	-	ns
Settling Time, t_{SET} (to 1/2 LSB)	See Figure 1	-	10	15	ns
CLK Pulse Width, T_{PW1} , T_{PW2}	See Figure 1	12.5	-	-	ns
POWER SUPPLY CHARACTERISTICS					
$I_{AV_{DD}}$	14.3MHz, at Color Bar Data Input	-	10.9	11.5	mA
$I_{DV_{DD}}$	14.3MHz, at Color Bar Data Input	-	4.2	4.8	mA
Power Dissipation	200 Ω load at $2V_{P,P}$ Output	-	-	80	mW

NOTES:

1. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board
2. Excludes error due to external reference drift.
3. Parameter guaranteed by design or characterization and not production tested.
4. Electrical specifications guaranteed only under the stated operating conditions.

Timing Diagram

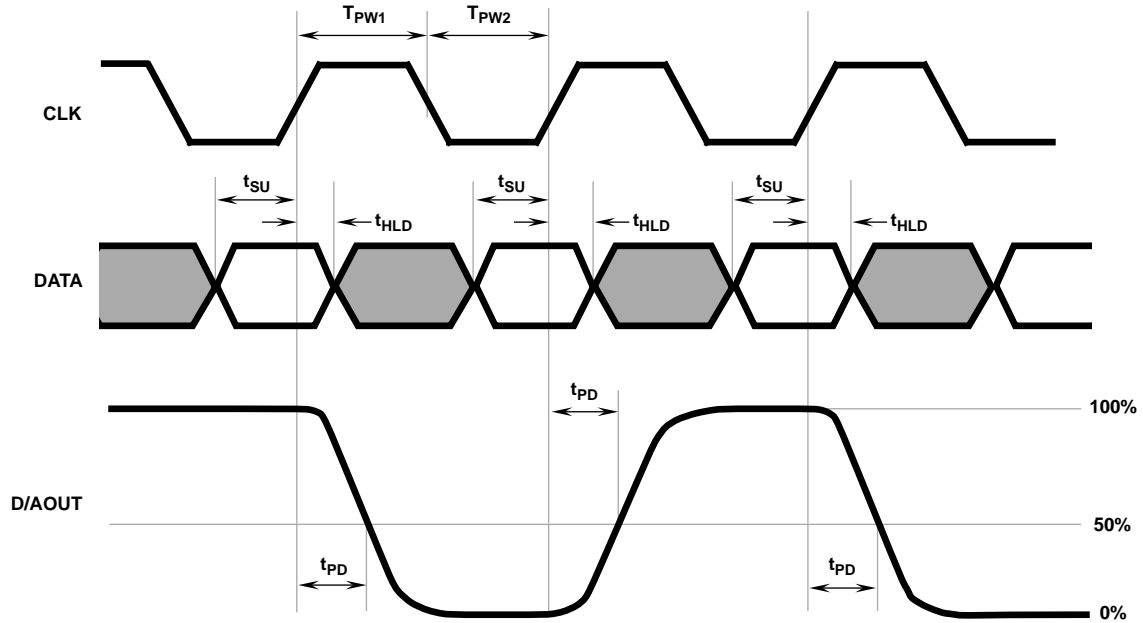


FIGURE 1.

Typical Performance Curves

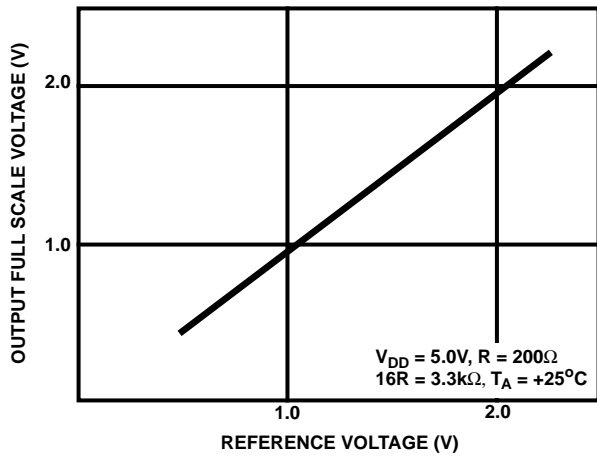


FIGURE 4. OUTPUT FULL SCALE VOLTAGE vs REFERENCE VOLTAGE

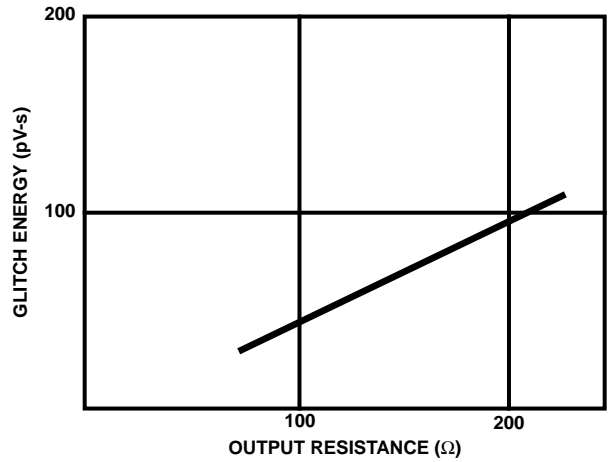


FIGURE 5. OUTPUT RESISTANCE vs GLITCH ENERGY

Typical Performance Curves

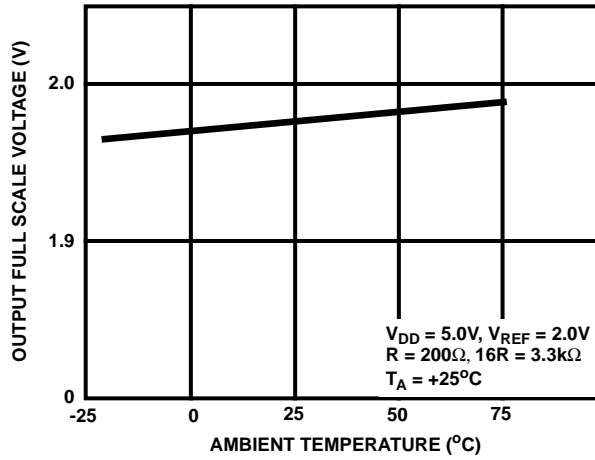


FIGURE 6. OUTPUT FULL SCALE VOLTAGE vs AMBIENT TEMPERATURE

Pin Description

24 PIN SOIC	PIN NAME	PIN DESCRIPTION
1-8	D0(LSB) thru D7(MSB)	Digital Data Bit 0, the Least Significant Bit thru Digital Data Bit 7, the Most Significant Bit
9	BLNK	Blanking Line, used to clear the internal data register to the zero condition when High, normal operation when Low.
10, 13	DV _{SS}	Digital Ground
11	VB	Voltage Bias, connect a 0.1μF capacitor to DV _{SS}
12	CLK	Data Clock Pin 100kHz to 40MHz
14	AV _{SS}	Analog Ground
15	I _{REF}	Current Reference, used to set the current range. Connect a resistor to AV _{SS} that is 16 times greater than the resistor on I _{OUT1} . (See Typical Applications Circuit)
16	V _{REF}	Input Reference Voltage used to set the output full scale range.
17	VG	Voltage Ground, connect a 0.1μF capacitor to AV _{DD} .
18, 19, 22	AV _{DD}	Analog Supply 4.75V to 7V
20	I _{OUT1}	Current Output Pin.
21	I _{OUT2}	Current Output pin used for a virtual ground connection. Usually connected to AV _{SS}
23, 24	DV _{DD}	Digital Supply 4.75V to 7V

Detailed Description

The HI1171, CXD1171 is an 8-bit, current out D/A converter. The DAC can convert at 40 MSPS and run on a single +5V supply. The architecture is an encoded, switched current cell arrangement.

Voltage Output Mode

The output current of the HI1171, CXD1171 can be converted into a voltage by connecting an external resistor to I_{OUT1} . To calculate the output resistor use the following equation:

$$R_{OUT} = V_{FS} / I_{FS}$$

where V_{FS} can range from +0.5V to +2.0V and I_{FS} can range from 0mA to 15mA

In setting the output current the I_{REF} pin should have a resistor connected to it that is 16 times greater than the output resistor.

$$R_{REF} = 16 \times R_{OUT}$$

As the values of both R_{OUT} and R_{REF} increase, power consumption is decreased, but glitch energy and output settling time is increased.

Clock Phase Relationship

The internal latch is closed when the clock line is high. The latch can be cleared by the BLNK line. When BLNK is set (HIGH) the contents of the internal data latch will be cleared. When BLNK is low data is updated by the CLK.

Noise Reduction

To reduce power supply noise separate analog and digital power supplies should be used with 0.1µF ceramic capacitors placed as close to the body of the HI1171, CXD1171 as possible. The analog (AV_{SS}) and digital (DV_{SS}) ground returns should be connected together back at the power supply to ensure proper operation from power up.

Test Circuits

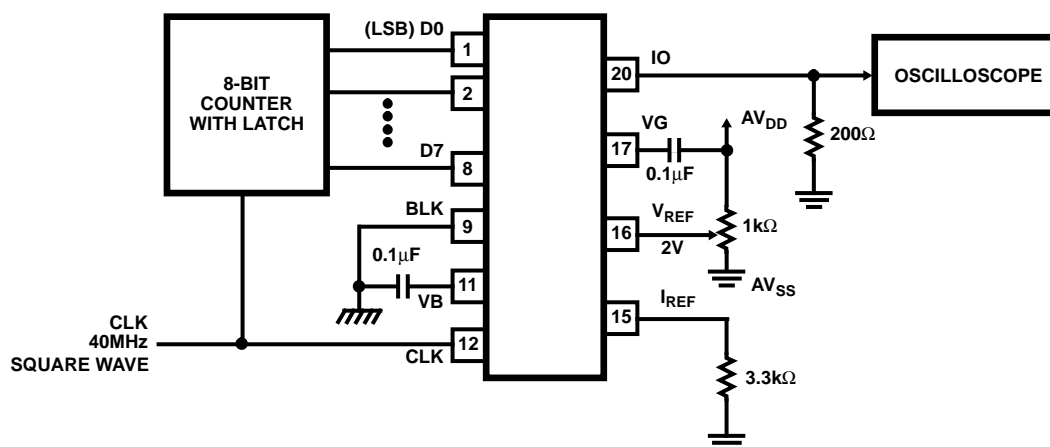


FIGURE 7. MAXIMUM CONVERSION SPEED TEST CIRCUIT

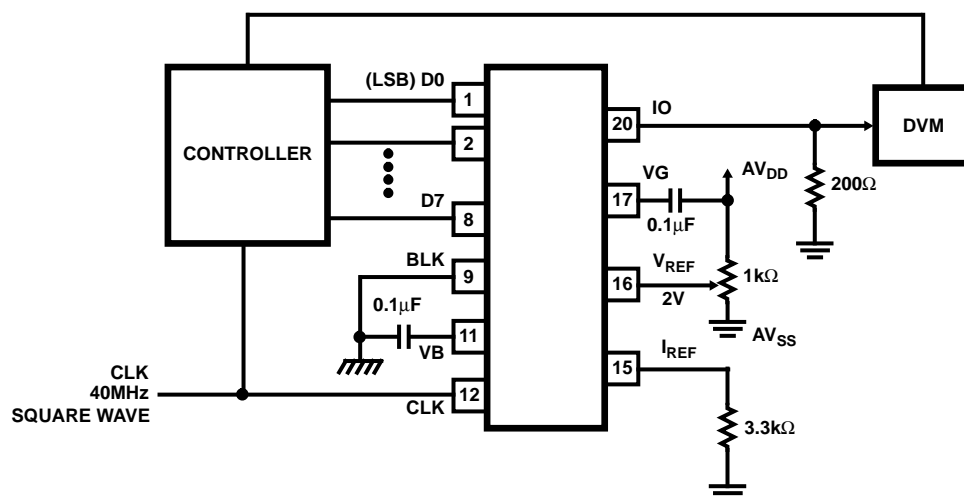


FIGURE 8. DC CHARACTERISTICS TEST CIRCUIT

Test Circuits (Continued)

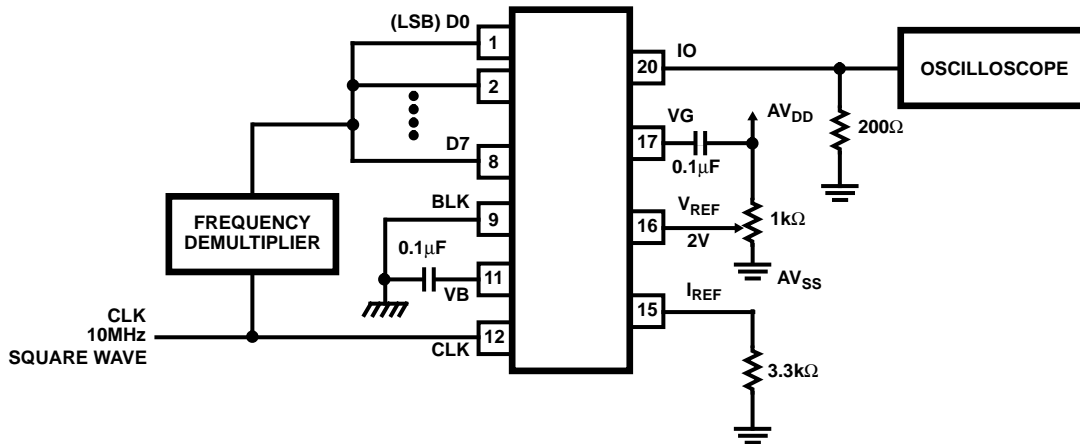


FIGURE 9. PROPAGATION DELAY TIME TEST CIRCUIT

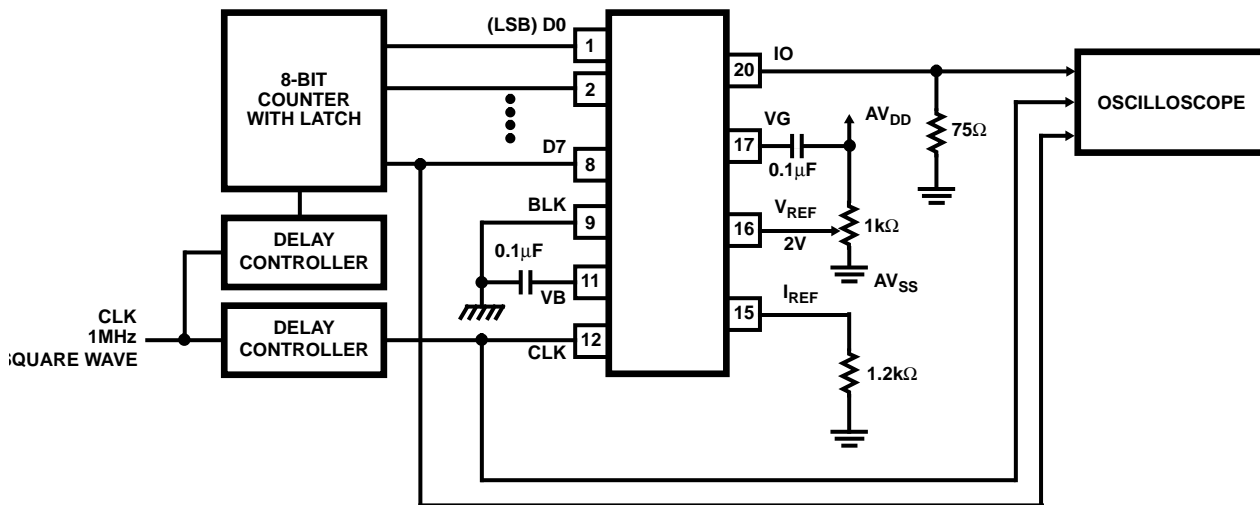
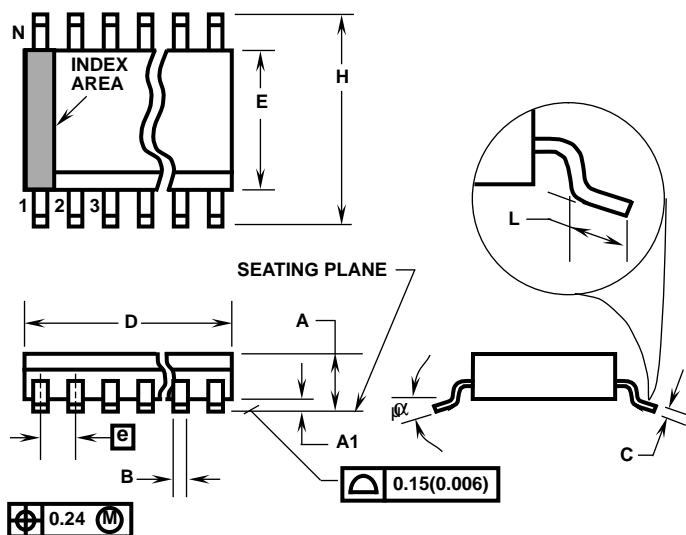


FIGURE 10. SET UP HOLD TIME AND GLITCH ENERGY TEST CIRCUIT

Small Outline Plastic Packages (SOIC)



M24.2-S
24 LEAD SMALL OUTLINE PLASTIC PACKAGE (200 MIL)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.067	0.088	1.70	2.25	-
A1	0.002	0.011	0.05	0.30	-
B	0.014	0.021	0.35	0.55	-
C	0.006	0.011	0.15	0.30	-
D	0.587	0.606	14.9	15.4	1
E	0.205	0.220	5.2	5.6	2
e	0.050 BSC		1.27 BSC		-
H	0.296	0.326	7.5	8.3	-
L	0.012	0.027	0.30	0.70	3
N	24		24		4
α	0°	10°	0°	10°	-

Rev. 1 4/95

NOTES:

1. Dimension "D" does not include mold flash, protrusions or gate burrs.
2. Dimension "E" does not include interlead flash or protrusions.
3. "L" is the length of terminal for soldering to a substrate.
4. "N" is the number of terminal positions.
5. Terminal numbers are shown for reference only.
6. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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