SONY

CXD1961Q

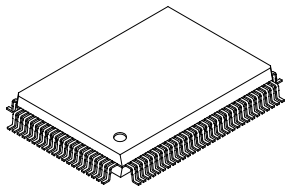
DVB-S Front-end IC (QPSK demodulator + FEC) *Preliminary*

Description

The CXD1961Q is a single chip DVB Satellite Broadcasting Front-end IC, including dual ADC for analog I/O inputs, QPSK demodulator, Viterbi decoder, de-interleaver, Reed-Solomon decoder and Energy Dispersal descrambler.

It is suitable for use in a DVB Integrated Receiver Decoder.

100 pin QFP (Plastic)



Features

- Dual 6 bit A/D converters
- QPSK demodulator
  - Multi-symbol rate operation
  - Nyquist roll off filter (α = 0.35)
  - Clock recovery circuit
  - Carrier recovery circuit
  - AGC control circuit
- Viterbi decoder
  - Constraint length K =7
  - Punctured rate R = 1/2 –7/8
  - Truncation length 144
  - Punctured rate search function
  - BER monitor
- De-interleaver
  - Packet synchronization
  - Convolutional de-interleaver
- Reed-Solomon decoder (204, 188)
- Energy dispersal descrambler
- CPU interface
  - I^2C bus interface/8 bit CPU bus
  - TTL interface level (5V input capability)
- JTAG(IEEE std 1149.1–1990) test mode
- Package : QFP-100pin
- Single +3.3V Power Supply
- Symbol rate max:32MSPS min:TBD
- Power consumption TBD
- 0.4um CMOS Technology

Applications

- DVB-S Set Top Box (Satellite)

Absolute Maximum Ratings (Ta=25°C, GND=0V)

• Supply voltage	V_{DD}	–0.5 to 4.6	V
• Input voltage	V_{IN}	–0.5 to V_{DD}+0.5	V
• Output voltage	V_{OUT}	–0.5 to V_{DD}+0.5	V
• I/O voltage	$V_{I/O}$	–0.5 to V_{DD}+0.5	V
• CPU I/F pin	V_{CPUIF}	–0.5 to 5.5	V
• Operating temperature	Topr	0 to +75	°C
• Storage temperature	Tstg	–55 to +150	°C

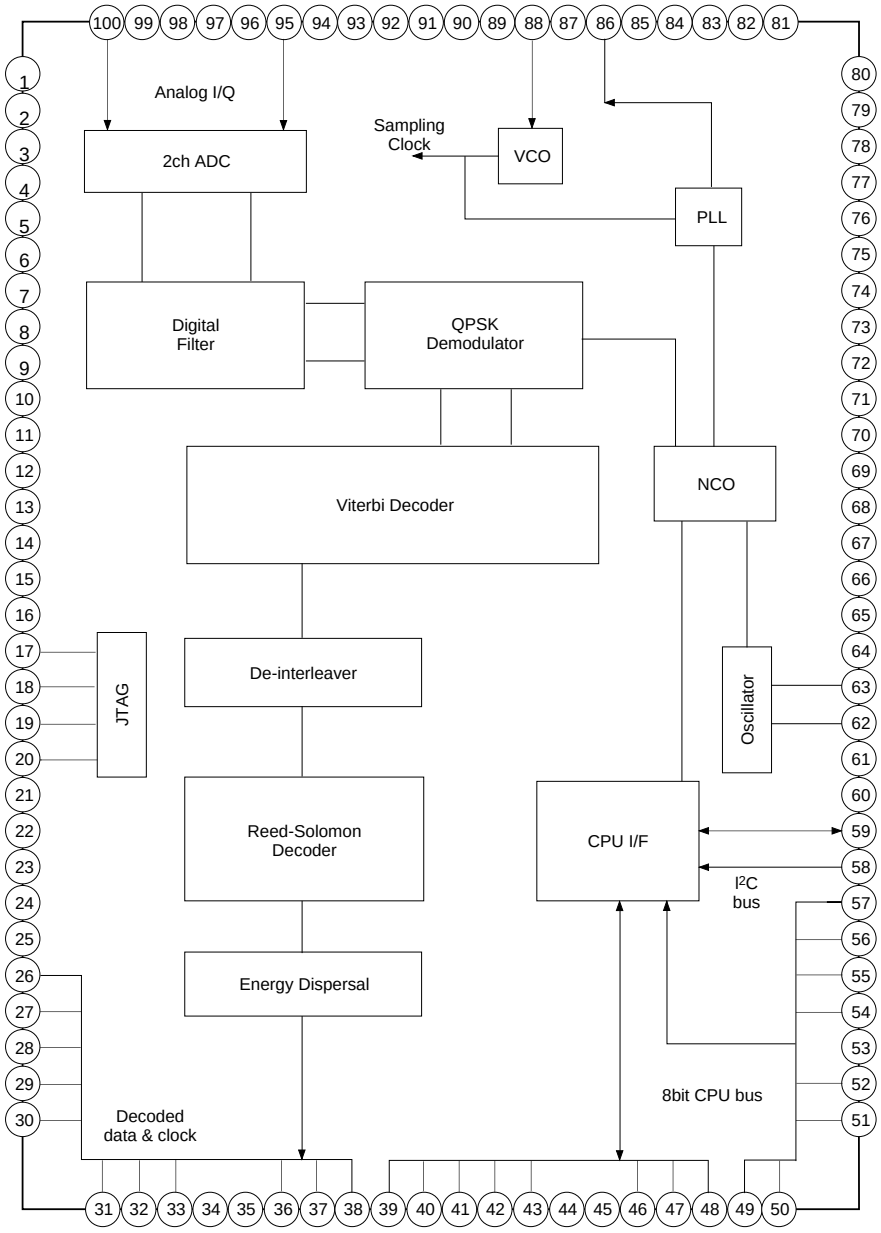
DC Recommended Operating Conditions

(Ta=0°C to 75°C, GND=0 V)

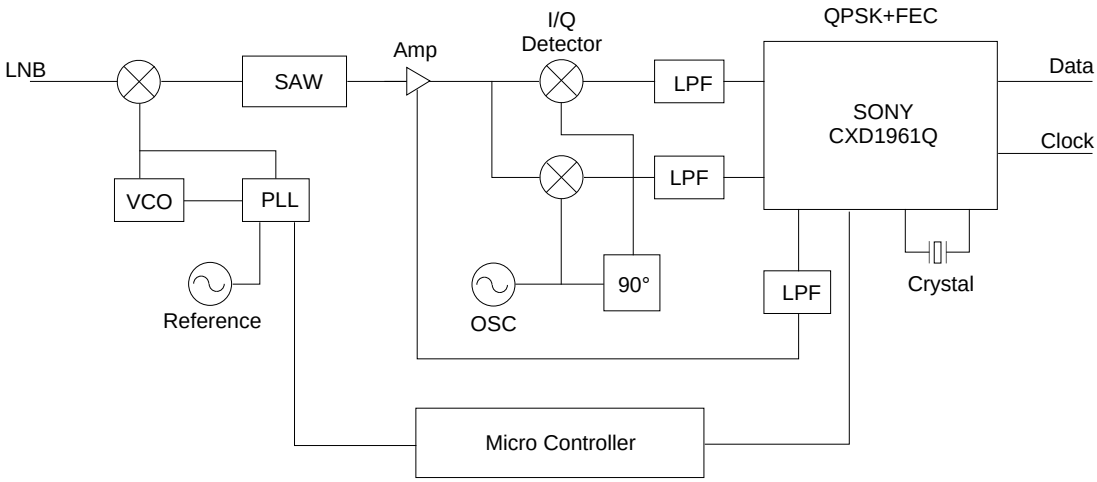
• Supply voltage	V_{DD}	3.15 to 3.45	V
• Input Hi-level	V_{IH}	V_{DD}–0.7 to V_{DD}+0.5	V
• Input Lo-level	V_{IL}	0.3 to V_{DD} +0.2	V

PE96417-TE

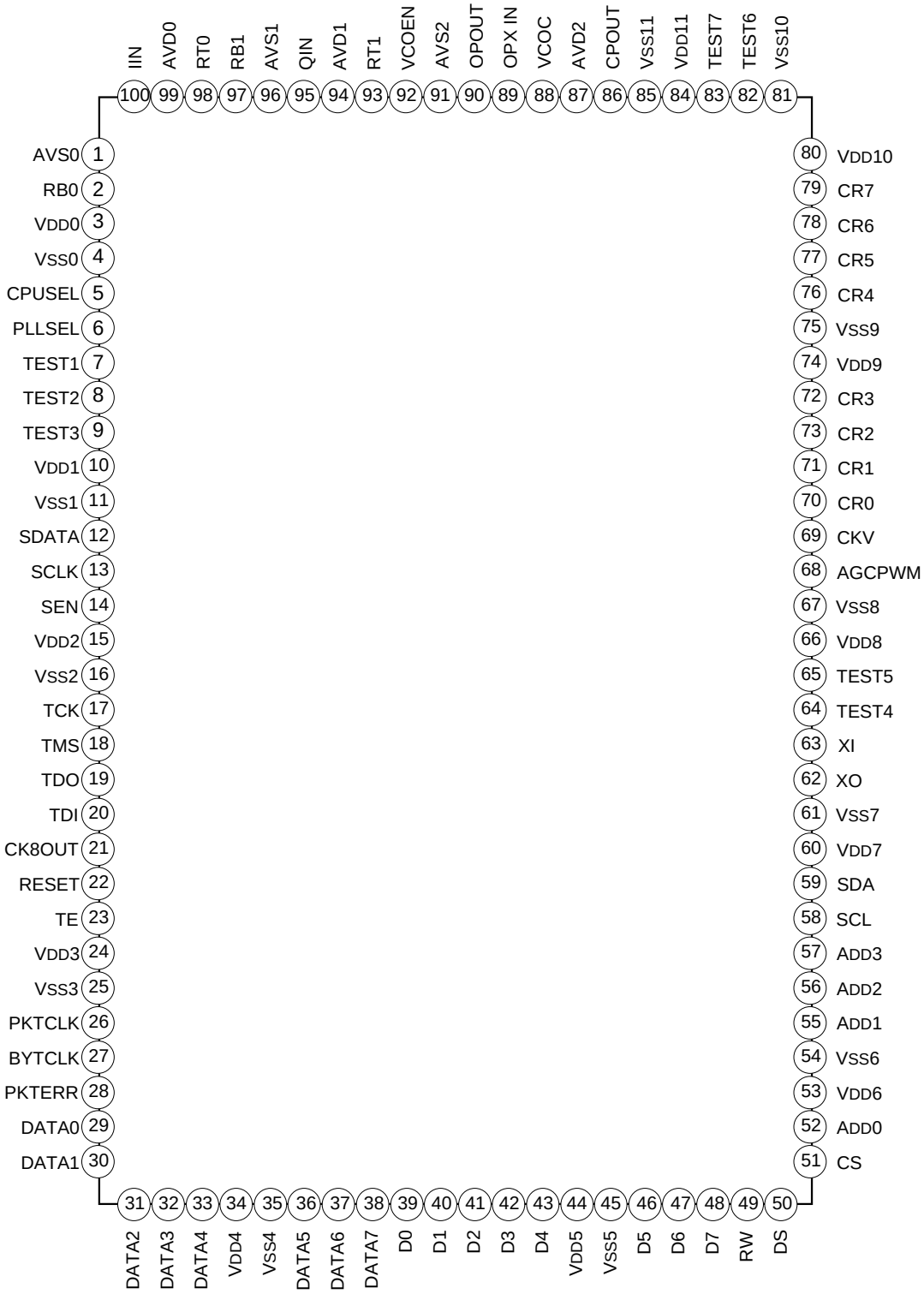
Block Diagram



Typical Application Block Diagram



Pin Configuration



Pin Description

No.	Symbol	I/O	Description
1	AVS0	—	Analog Ground
2	RB0	—	ADC0 bottom reference voltage
3	$V_{DD}0$	—	Digital Power Supply (+3.3 V)
4	$V_{SS}0$	—	Digital Ground
5	CPUSEL	I	CPU interface select (L : I^2C bus)
6	PLLSEL	I	Connect Digital Ground
7–9	TEST1–3	I	Test input (connect Digital Ground)
10	$V_{DD}1$	—	Digital Power Supply (+3.3 V)
11	$V_{SS}1$	—	Digital Ground
12	SDATA	O	SONY internal use
13	SCLK	O	SONY internal use
14	SEN	O	SONY internal use
15	$V_{DD}2$	—	Digital Power Supply (+3.3 V)
16	$V_{SS}2$	—	Digital Ground
17	TCK	I	JTAG test clock
18	TMS	I	JTAG test mode select
19	TDO	O	JTAG test data output
20	TDI	I	JTAG test data input
21	CK8OUT	O	Divide by 8 clock of Crystal clock
22	RESET	I	Reset input (L : reset)
23	TE	I	Test Enable (H : test enable)
24	$V_{DD}3$	—	Digital Power Supply (+3.3 V)
25	$V_{SS}3$	—	Digital Ground
26	PKTCLK	O	R/S Packet clock
27	BYTCLK	O	R/S Byte clock
28	PKTERR	O	R/S uncorrectable Packet flag
29–33	DATA0–4	O	R/S data output (DATA0 : LSB)
34	$V_{DD}4$	—	Digital Power Supply (+3.3 V)
35	$V_{SS}4$	—	Digital Ground
36–38	DATA5–7	O	R/S data output (DATA7 : MSB)
39–43	D0–D4	I/O	8 bit CPU bus data I/O (D0 : LSB)
44	$V_{DD}5$	—	Digital Power Supply (+3.3 V)
45	$V_{SS}5$	—	Digital Ground
46–48	D5–D7	I/O	8 bit CPU bus data I/O (D7 : MSB)
49	RW	I	8 bit CPU bus Read/Write (H : Read)
50	DS	I	8 bit CPU bus Data strobe
51	CS	I	8 bit CPU bus Chip Select
52	$A_{DD}0$	I	8 bit CPU bus Address0 (LSB)
53	$V_{DD}6$	—	Digital Power Supply (+3.3 V)
54	$V_{SS}6$	—	Digital Ground

No.	Symbol	I/O	Description
55–57	ADD1–3	I	8 bit CPU bus Address1–3 (ADD3 : MSB)
58	SCL	I	I²C bus serial clock
59	SDA	I/O	I²C bus serial data
60	V_{DD}7	—	Digital Power Supply (+3.3 V)
61	V_{SS}7	—	Digital Ground
62	XO	O	Oscillator output (for Crystal)
63	XI	I	Oscillator input (for Crystal)
64, 65	TEST4, 5	O	Test output (V_{SS} level)
66	V_{DD}8	—	Digital Power Supply (+3.3 V)
67	V_{SS}8	—	Digital Ground
68	AGCPWM	O	PWM output for AGC
69	CKV	O	Sampling Clock monitor output
70–73	CR0–3	O	Clock Recovery data 0–3 (CR0 : LSB)
74	V_{DD}9	—	Digital Power Supply (+3.3 V)
75	V_{SS}9	—	Digital Ground
76–79	CR4–7	O	Clock Recovery data 4–7 (CR7 : MSB)
80	V_{DD}10	—	Digital Power Supply (+3.3 V)
81	V_{SS}10	—	Digital Ground
82, 83	TEST6, 7	O	Test output (V_{SS} level)
84	V_{DD}11	—	Digital Power Supply (+3.3 V)
85	V_{SS}11	—	Digital Ground
86	CPOUT	O	PLL Charge pump output
87	AVD2	—	Analog Power Supply (+3.3 V)
88	VCOC	I	VCO control voltage input
89	OPXIN	I	Embedded OP-Amp Negative input
90	OPOUT	O	Embedded OP-Amp output
91	AVS2	—	Analog Ground
92	VCOEN	I	VCO enable (H : enable)
93	RT1	—	ADC1 top reference voltage
94	AVD1	—	Analog Power Supply (+3.3 V)
95	QIN	I	Analog Q input (ADC1 input)
96	AVS1	—	Analog Ground
97	RB1	—	ADC1 bottom reference voltage
98	RT0	—	ADC0 top reference voltage
99	AVD0	—	Analog Power Supply (+3.3 V)
100	IIN	I	Analog input (ADC0 input)

Note)

Apply 0.1 µF capacitor to every power supply terminal.

Apply 0.1µF capacitor to RB0, RT0, RB1, RT1 for stable A to D conversion.

CPU Interface Register

Sub address	R/W	MSB 7	6	5	4	3	2	1	LSB 0
0	R	ADC_IN7	ADC_IN6	ADC_IN5	ADC_IN4	ADC_IN3	ADC_IN2	ADC_IN1	ADC_IN0
1	R	BECNT15	BECNT14	BECNT13	BECNT12	BECNT11	BECNT10	BECNT9	BECNT8
2	R	BECNT7	BECNT6	BECNT5	BECNT4	BECNT3	BECNT2	BECNT1	BECNT0
3	R	QSYNC	AFC3	AFC2	AFC1	AFC0	VSYNC	RSYNC	BEM_END
4	W	AGC7	AGC6	AGC5	AGC4	AGC3	AGC2	AGC1	AGC0
5	W	VS_N4	VS_N3	VS_N2	VS_N1	VS_N0	RATE2	RATE1	RATE0
6	W	QS_N3	QS_N2	QS_N1	QS_N0	AC2	AC1	BC2	BC1
7	W	AK2	AK1	S_INV	AGC_INV	AGC_MOD	TIMER2	TIMER1	TIMER0
8	W	PLL_CTL	MON_SW	VS_T3	VS_T2	VS_T1	VS_T0	CE_LEV1	CE_LEV0
9	W	DF_SKIP	DOUT_INV	RS_SKIP	SSEL	AFC_MOD	BER_T2	BER_T1	BER_T0
A	W	SFD18	SFD17	SFD16	SFD15	SFD14	SFD13	SFD12	SFD11
B	W	SFD10	SFD9	SFD8	SFD7	SFD6	SFD5	SFD4	SFD3
C	W	SFD2	SFD1	SFD0	PCD2	PCD1	PCD0	REF_SEL	REF_LSB
D	W	NC023	NC022	NC021	NC020	NC019	NC018	NC017	NC016
E	W	NC015	NC014	NC013	NC012	NC011	NC010	NC09	NC08
F	W	NC07	NC06	NC05	NC04	NC03	NC02	NC01	NC00

Note)

1. Above Registers are shared by I²C bus interface and 8 bit CPU bus interface.
2. To select CPU interface, use CPUSEL (Pin 5) ; H : 8 bit CPU bus / L : I²C bus.
3. I²C bus interface slave address;

MSB 6	5	4	3	2	1	LSB 0	R/W
1	1	0	1	1	1	0	

Write mode : DC (Hex)
Read mode : DD (Hex)

CPU Interface Register Brief Explanation

ADD 0	ADC_IN (7 : 0)	ADC input level (I^2+Q^2 at QPSK demodulator)
ADD 1, 2	BECNT (15 : 0)	Bit Error Count at QPSK demodulator output
ADD 3	QSYNC	QPSK Synchronization Flag (H : in sync.)
	AFC (3 : 0)	Auto Frequency Control data
	VSYNC	Viterbi dec. Synchronization Flag (H : in sync)
	RSYNC	Reed-Solomon dec. Synchronization Flag (H : in sync)
	BEM_END	Bit Error Monitor enable Flag (H : enable)
ADD 4	AGC (7 : 0)	(when AGC mode is H) AGC Gain control data
		(when AGC mode is L) Reference data for self AGC
ADD 5	VS_N (4 : 0)	V sync threshold Bit Error Count (see Fig. 1)
	RATE (2 : 0)	Punctured rate (see Fig. 2)
ADD 6	QS_N (3 : 0)	Threshold data for QPSK sync. judgement (see Fig. 3)
	AC (2 : 1), BC (2 : 1)	Parameter for Carrier recovery loop filter (see Fig. 4)
ADD 7	AK (2 : 1)	Parameter for Clock recovery loop filter (see Fig. 4)
	S_INV	I/Q exchange (H : enable)
	AGC_INV	AGC control voltage polarity (H : positive)
	AGC_MOD	H : controlled by CPU (slave) L : self AGC mode (master)
	TIMER (2 : 0)	Timer for AGC master mode (see Fig. 5)
ADD 8	PLL_CTL	For SONY internal use (input 0 for norma use)
	MON_SW	For SONY internal use (input 0 for norma use)
	VS_T (3 : 0)	Monitor period for Viterbi sync. (see Fig. 6)
	CE_LEV (1 : 0)	Clock recovery Error feed back level (see Fig. 7)
ADD 9	DF_SKIP	Digital Filter skip mode (H : enable)
	DOUT_INV	Data output timing invert (H : falling edge)
	RS_SKIP	R/S decode skip mode (H : enable)
	SSEL	For SONY internal use (input 0 for normal use)
	AFC_MOD	For SONY internal use (input 0 for normal use)
	BER_T (2 : 0)	Monitor period for Bit error Count (see Fig. 8)
ADD A	HS_PLL	For SONY internal use (input 0 for normal use)
ADD A, B, C	SFD (17 : 11)	For SONY internal use (input 0 for normal use)
ADD C	PCD (2 : 0)	For SONY internal use (input 0 for normal use)
	REF_SEL	For SONY internal use (input 0 for normal use)
	REF_LSB	For SONY internal use (input 0 for normal use)
ADD D, E, F	NC0 (23 : 0)	Sampling Frequency 2*Fs=NC0 (0 : 23)*8*Fxtal/2^{24}
		(Fxtal=Crystal Frequency)

Fig. 1 V sync threshold (Error Counter Preset data)

Register	VS_N4	VS_N3	VS_N2	VS_N1	VS_N0
Limit	$\times 2^9$	$\times 2^8$	$\times 2^7$	$\times 2^6$	$\times 2^5$

max. : 992
min. : 32

(ex. VS_N (4 : 0)=(1, 1, 0, 0, 1) Limit=$0\times 2^9+0\times 2^8+1\times 2^7+1\times 2^6+0\times 2^5=192$)

Fig. 2 Punctured Rate

Punc. rate	1/2	2/3	3/4	4/5	5/6	6/7	7/8	Auto
RATE2	0	0	0	1	1	1	1	0
RATE1	0	1	1	0	0	0	1	0
RATE0	1	0	1	0	1	0	1	0

Fig. 3 QPSK Synchronization monitor

QSYNC Threshold	$(QS\_N3)\times2^7+(QS\_N2)\times2^6+(QS\_N1)\times2^5+(QS\_N0)\times2^4$
QSYNC Monitor Period	256 (fix)

Fig. 4 Costas Loop Filter co-efficiency

Parameter	(0, 0)	(0, 1)	(1, 0)	(1, 1)	Item
(AC2, AC1)	×1	1/2	1/4	1/8	Carrier recovery IIR filter
(BC2, BC1)	×1	×2	×4	×8	Carrier recovery tracking range
(AK2, AK1)	×1	1/2	1/4	1/8	Clock recovery IIR filter

Fig. 5 Timer period (Sampling Frequency = 60 MHz)

TIMER2	1	1	1	1	0	0	0	0
TIMER1	1	1	0	0	1	1	0	0
TIMER0	1	0	1	0	1	0	1	0
Period (ms)	140	70	35	17.5	8.75	4.38	2.19	1.09
Frequency (kHz)	7.14	14.3	28.6	57.1	114	229	457	914

Fig. 6 V sync monitor period (measurement period counter preset data)

Register	VS_T3	VS_T2	VS_T1	VS_T0
Period (viterbi clock)	$\times2^{12}$	$\times2^{11}$	$\times2^{10}$	$\times2^9$

max. : 6656
min. : 512
(viterbi clock)

(ex. VS_T (3:0)=(0, 1, 1, 1) → Limit=$1\times2^{12}+0\times2^{11}+0\times2^{10}+0\times2^9$=4096)

Fig. 7 Clock recovery error data (8 bit) feed back level

CE_LEV \ NCO	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(1, 1)															←						→			
(1, 0)																←						→		
(0, 1)																	←						→	
(0, 0)																		←						→

Fig. 8 Bit Error Monitor period (Viterbi clock)

BER_T2	1	1	1	1	0	0	0	0
BER_T1	1	1	0	0	1	1	0	0
BER_T0	1	0	1	0	1	0	1	0
Period	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^6

Functional Description

(1) CPU Interface

CXD1961Q has two CPU interface, an 8 bit CPU bus and an I²C bus interface. Fix CPUSEL (Pin 5) to DC L or H level depending on the choice of bus.

CPUSEL=L : I²C bus / H : 8 bit bus

I²C bus Interface

The CXD1961Q's slave address is "1101110", and the read/write operation is based on Philips standard.

<Write Data>

In write operation, the second byte is input as the sub-address of the start position. The 3rd byte then forms the data to be written to the start register.

Successive data bytes are written to successive sub-address register.

S T A	Slave Address 1101110		0	A C K	Sub- Address Nhex	A C K	Input data for "N"	A C K	Input data for "N+1"	A C K	• • •	A C K	S T P

STA : Start condition

ACK : Acknowledgment by CXD1961Q

STP : Stop Condition

Note)

Registers of Sub-Address 0hex to 3hex are read only

<Read Data>

Before read operation, the sub-address of the start register to be read is input by using write operation, and terminated by a stop condition.

Read operation then begins with the second byte which is the data of the start register. Data of successive sub-address registers are read successively following by the second byte.

S T A	Slave Address 1101110		0	A C K	Sub- Address Nhex	A C K	S T P

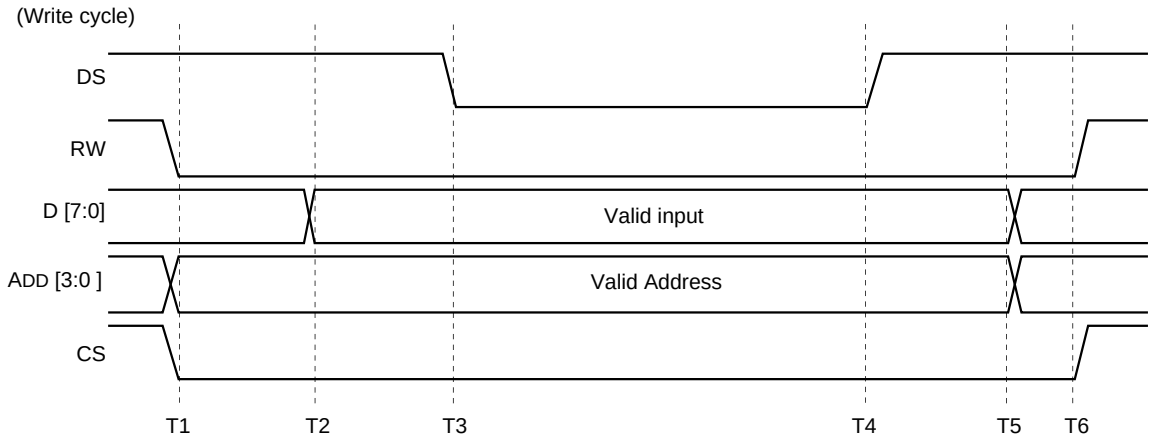
S T A	Slave Address 1101110		1	A C K	Output data from "N"	A C K	Output data from "N+1"	A C K	• • •	A C K	S T P

Note)

Registers of Sub-Address 4hex to Fhex are write only

8 bit CPU bus Interface

(Write cycle)

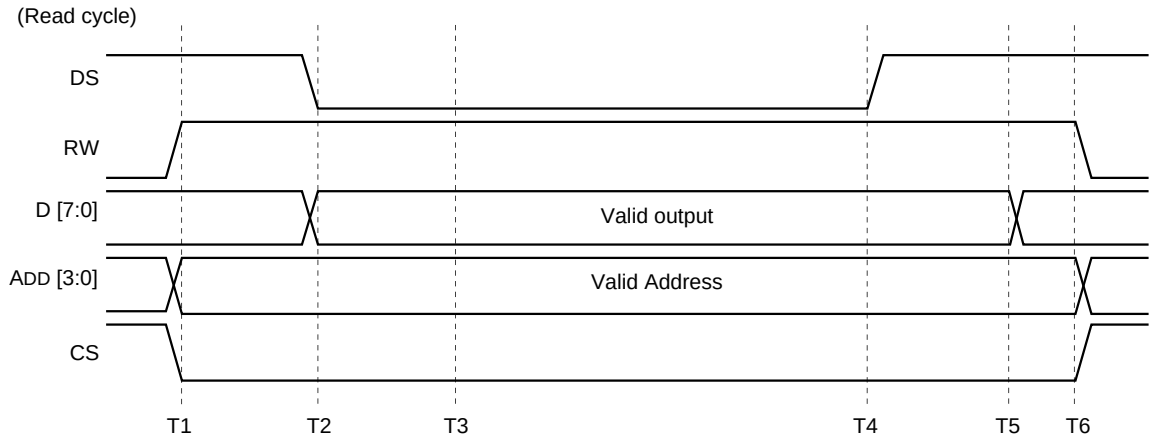


Timing	Description	Min (nsec)	Max (nsec)
T2–T1	Address, CS to Data valid	25	
T3–T1	R/W to DS	24	
T3–T2	Data valid to DS	10	
T4–T3	DS pulse width	70	
T5–T4	Data hold time	21	
T6–T4	Address, CS, R/W hold time	24	

Note)

Registers of Address 0hex to 3 hex are read only

(Read cycle)



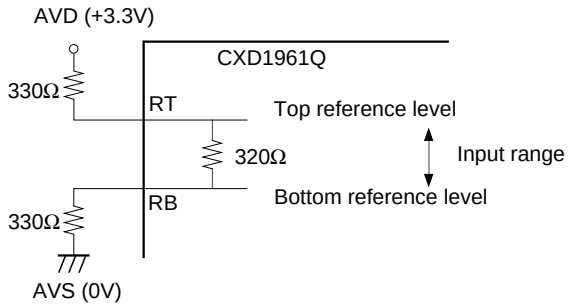
Timing	Description	Min (nsec)	Max (nsec)
T2–T1	Address, CS, R/W to DS	24	
T3–T2	DS to Data valid		75
T4–T2	DS pulse width	105	
T5–T4	Data hold time		24
T6–T4	Address, CS, R/W hold time	24	

Note)

Registers of Address 4hex to Fhex are write only

(2) Analog to Digital Converters

The Dual 6 bit A to D converters quantize the analog I/Q input data. The input range of the ADC's is determined by external resistors. RT0 (RT1) is the top reference voltage, and RB0 (RB1) is the bottom reference voltage. RT0 (RT1) and RB0 (RB1) are connected internally with a 320 Ω (Typical value) resistor. In the example shown in the following figure, input range is approximately 1.1 V, and center voltage 1.65 V.



(3) AGC

Input signal level of the A to D Converter is estimated by calculating I^2+Q^2 in 16 bit precision, and the upper 8 bits of the estimated data are sent via the CPU I/F as ADC_IN [7:0]. CXD1961Q has two AGC modes that can be selected by AGC_MOD. In AGC slave mode, ADC_IN[7:0] is checked and an appropriate gain level AGC[7:0] is returned by the micro controller. This value is converted into 8 bit PWM format and output from AGCPWM (Pin 68).

In AGC master mode, reference level AGC[7:0] is set via the CPU I/F and compared to ADC_IN[7:0] internally. The updated gain level is then output at the AGCPWM pin. In normal operation, ADC_IN[7:0] becomes almost equal to reference level. In AGC master mode, AGC control interval is set by TIMER[2:0]. In both modes, AGCPWM output should be low pass filtered, and if needed, the level should be converted to satisfy the AGC gain control range. Depending on AGC_INV, the polarity can be inverted. (H:positive / L:negative)

CPU Register

ADC_IN [7 : 0] → ADD 0h AGC [7 : 0] → ADD 4h AGC_INV → ADD 7h

AGC_MOD → ADD 7h TIMER [2 : 0] → ADD 7h

Reference level ADC_IN [7 : 0]	Input signal level to ADC input range ratio
0F	0.25
3F	0.5
7F	0.7
FF	1.0 or over range

Note)

ADC input range is subject to temperature and V_{DD} level.

(4)Clock Recovery

Initial sampling clock frequency is set by a 24 bit word via the CPU I/F. This 24 bit word is written to the NCO(Numerically Controlled Oscillator).

The sampling frequency is:

$$Fsample = 8*NCO[23:0]*Fxtal/2^{24}$$

where: NCO [23:0] is the parameter for sampling frequency, "8" is the divider gain of the PLL, Fxtal is the reference crystal frequency, whose value should be more than 30MHz (32MHz is recommended).

The internal digital clock recovery loop feeds clock error data to the above NCO to provide sampling timing correction .

AK [2:1] is the Loop Filter coefficient and CE_LEV [1:0] is the Loop Gain.

This value limits clock recovery range and resolution. (see the CPU Interface Register Brief Explanation Fig.7)

Sampling clock is output from CKV (pin 69).

CPU I/F Register

AK [2:1] → ADD 7h CE_LEV [1:0] → ADD 8h NCO [23:0] → ADD D, E, Fh

(Example)

CE_LEV [1:0]=(0,1), NCO [23:0]=(001110000000000000000000), Fxtal=32 MHz

Sampling Frequency	$= 8*(2^{21}+2^{20}+2^{19})*32*10^6/2^{24}$		
	$= 2^3*7*10^6 = 56*10^6$	→	56 MHz
Clock recovery range	$= 2^9/(2^{21}+2^{20}+2^{19})$		
	$= 1/2^{10}/7 = 139.5..*10^{-6}$	→	±140 ppm
Clock recovery resolution	$= 8*2^1*32*10^6/2^{24} = 30.5...$	→	31 Hz

(5)Carrier Recovery

The Analog I/Q inputs have a carrier offset frequency, which is not corrected by the tuner's PLL Synthesizer. The offset is compensated by a Costas Loop, using a frequency multiplier, loop filter and the NCO. AC [2:1] is the coefficient of the loop filter and BC [2:1] is the loop gain parameter. QPSK synchronization(QSYNC) is determined by monitoring the output of loop filter. The internal sync detector monitors 256 cycles, and checks the value with the threshold set by QS_N [3:0]. In QPSK synchronization, AFC [3:0] indicates the offset proportional value which remains at that point. This value is the average data of the loop filter output. If AFC3(=MSB) is high, tuner PLL has a negative offset to the carrier frequency , and vice versa if AFC3 is low. By feeding the AFC [3:0] to the tuner's PLL Synthesizer, carrier offset can be corrected with the PLL step size.

CPU I/F Register

QSYNC,AFC [3:0] → ADD 3h QS_N [3:0], AC [2:1], BC [2:1] → ADD 6h

(6) Viterbi decoder

By using QPSK demodulated data and Viterbi decoded data, the existence of errors is detected. Bit error measured over a certain period is used to determine the correct punctured rate and phase synchronization as well as bit error rate (BER). VS_N[4:0] is used to set the error count threshold, and VS_T[3:0] is used to set the error count duration. (see Fig.1 and Fig. 6 of CPU Interface Register Brief Explanation)

For example)

VS_N[4:0]=(1, 1, 0, 0, 1) → Error Count threshold =192

VS_T[3:0] =(1, 0, 1, 1) → Error Count duration = 2048

In this case, bit error is checked for 2048 cycles. If the error count is less than 192, CXD1961Q judges that punctured decoding is in sync and VSYNC goes high.

Punctured rate is set by RATE[2:0]. When a certain rate is set by RATE[2:0], only punctured phase search is performed. Punctured rate and phase search is performed if RATE[2:0] is set to (0, 0, 0).

CXD1961Q has 2^{16} (= 65536) bit counter for BER estimation. BER monitor period is set by BER_T[2:0] (see Fig. 8), and the error count is read by CPU I/F as BECNT[15:0]. If BEM_END is low, punctured rate or phase search is not finished and the error count is not reliable at that moment.

CPU I/F Register

BERCNT[15:0]	→ ADD 1, 2h	VSYNC	→ ADD 3h	BEM_END	→	ADD 3h
VS_N[4:0]	→ ADD 5h	VS_T[3:0]	→ ADD 8h	BER_T[2:0]	→	ADD 9h

(7) Packet synchronization and De-inter leaver

2 dimensional sync protection starts once sync word 47 hex or inverted sync word B 8 hex is detected. In this algorithm, sync status changes with hysteresis depending on sync or non-sync detection every 204 byte, so that the probability of false-LOCK or Sync-loss is minimized.

When the packet synchronization is achieved,the convolutional de-inter leaver

(Forney, depth=12) starts operating.

(8) Reed - Solomon decoder

The Galois Field is generated by $F(x) = x^8+x^4+x^3+x^2+1$

Code is generated by $G(x) = (x-\alpha^0)(x-\alpha^1)(x-\alpha^2) \bullet \bullet (x-\alpha^{15})$

If RS_SKIP is high, no correction is performed.

CPU I/F Register

RS_SKIP → ADD 9h

(9) Energy Dispersal

Energy dispersal descrambling is represented by the polynomial $x^{15}+ x^{14} +1$. Initial sequence is loaded when inverted sync word B8hex is detected. 1 dimensional sync protection circuit checks the inverted sync word every 8 packets. When it is in sync, RSYNC goes high. Even if the sync is lost, the initial sequence continues to be loaded at previous time step.

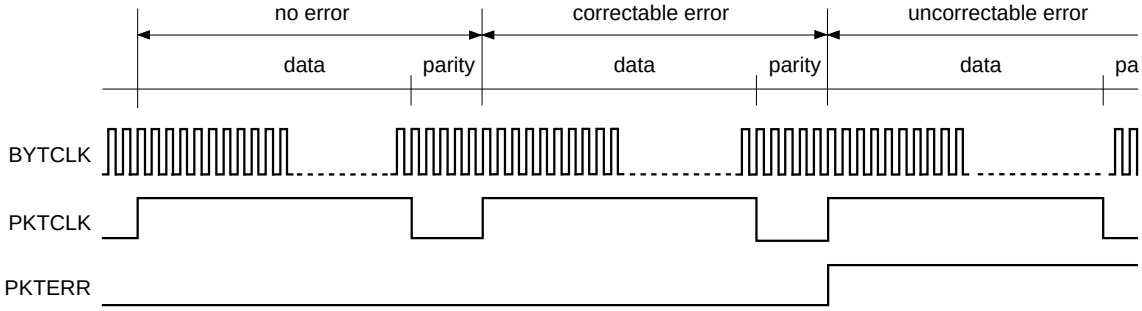
CPU I/F Register

RSYNC → ADD 3h

(10) Output Data Format

The following figure shows the output format of BYTCLK, PKTCLK, PKTERR. BYTCLK is generated by dividing the internal viterbi clock by 8. Data output DATA[7:0] is output in sync with BYTCLK. DOUT_INV determines whether DATA[7:0] is output on the rising edge or the falling edge of BYTCLK. PKTCLK High-Time is equal to 188 data bytes period and PKTCLK Low-Time is equal to 16 parity bytes period. PKTERR goes H if an uncorrectable error packet is encountered.

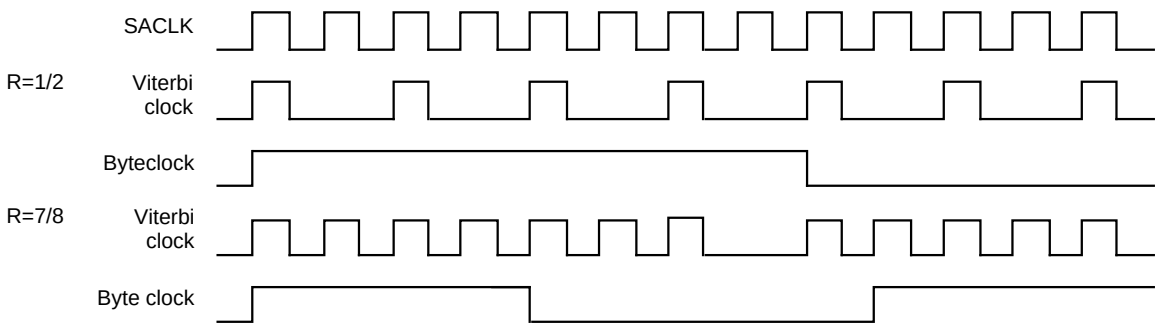
CPU I/F Register
DOUT_INV → ADD 9h



BYTCLK and PKTCLK have varying forms, depending on the punctured rate. The following figure shows Minimum and Maximum values for each rate.
One unit represents 1 sampling clock (=2*Symbol rate) cycles.

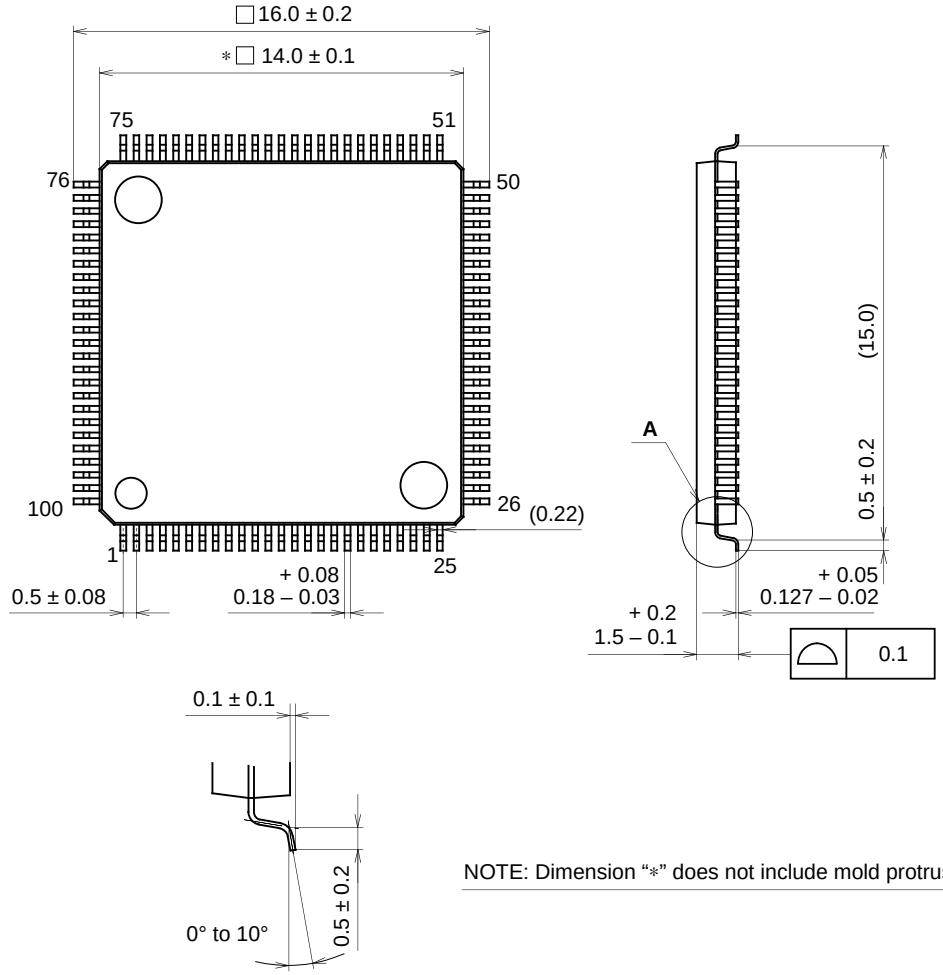
	BYTCLK						PKTCLK					
	Period		High-Time		Low-Time		Period		High-Time		Low-Time	
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
R=1/2	16	16	8	8	8	8	3264	3264	3008	3008	256	256
R=2/3	12	12	6	6	6	6	2448	2448	2256	2256	192	192
R=3/4	10	11	5	6	5	6	2176	1276	2005	2006	170	171
R=4/5	10	10	5	5	5	5	2040	2040	1880	1880	160	160
R=5/6	9	10	4	5	4	5	1948	1949	1804	1805	153	154
R=6/7	9	10	4	5	4	5	1904	1904	1754	1755	149	150
R=7/8	9	10	4	5	4	5	1865	1866	1718	1719	146	147

(For example)



Package Outline Unit : mm

100PIN LQFP (PLASTIC)



NOTE: Dimension "∗" does not include mold protrusion.

DETAIL **A**

SONY CODE	LQFP-100P-L01
EIAJ CODE	∗QFP100-P-1414-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY/PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	————