SONY

# CXD2956AGL-1

## GPS Baseband LSI

### Description

The CXD2956AGL-1 is a dedicated LSI for the GPS (Global Positioning System), satellite-based location measurement system.

Compared with conventional methods, position detection time and sensitivity are substantially improved with the use of an advanced signal processing scheme.

Although package sizes differ, the CXD2956AGL-1 has realized compatibility with a foot pattern to the CXD2963GH.

This LSI used together with the Sony GPS RF down converter IC enables the configuration of a 2-chip system capable of measuring its position anywhere on the globe. The CXD2956AGL-1 is ideal for use in automotive, cellular handset, handheld navigation, mobile computing and other location-based applications.

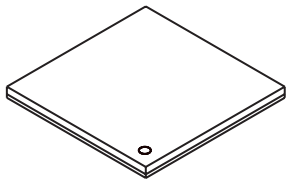
### Features

- 12-channel GPS receiver capable of simultaneously receiving 12 satellites
- Reception frequency: 1575.42MHz
  (L1 band, CA code)
- Reference clock (TCXO) frequency:
  18.414MHz (GPS, Sony compatible),
- 32-bit RISC CPU (ARM7TDMI)
- 288K-byte Program ROM
- 72K-byte Data RAM
  Power is supplied only to 8K-byte Data RAM while in backup mode.
- System power management
- 1-channel UART
- Internal RTC (Real Time Clock)
- 10-bit successive approximation system A/D converter
- All-in-view positioning
- Communication format: Supports NMEA-0183
- Supports DGPS (optional)
  Conforms to RTCM SC-104 Ver. 2.1 and DARC
- 1 PPS output
- Supports assisted-GPS for cellular (optional)

### Structure

Silicon gate CMOS IC

183 pin VFLGA (Plastic)



### Absolute Maximum Ratings

| | | | |
|---|---|---|---|
| • Supply voltage I/O | $IOV_{DD}$ | –0.5 to +4.6 | V |
| • Supply voltage core | $CV_{DD}$ | –0.5 to +2.5 | V |
| • Input voltage | $V_I$ | –0.5 to +6 | V |
| • Output voltage | $V_O$ | –0.5 to +6 | V |
| • Operating temperature | Topr | –40 to +85 | °C |
| • Storage temperature | Tstg | –50 to +150 | °C |

### Recommended Operating Conditions

| | | | |
|---|---|---|---|
| • Supply voltage I/O | $IOV_{DD}$ | 3.0 to 3.6 | V |
| * Under operation with internal ROM, using no external expansion bus: $IOV_{DD}$ 2.6 to 3.6V | | | |
| * Under operation in backup mode: $BKUPIOV_{DD}$ 2.5 (Min.) V | | | |
| • Supply voltage core | $CV_{DD}$ | 1.62 to 1.98 | V |
| • Operating temperature | Topr | –40 to +85 | °C |

### Input/Output Pin Capacitance

| | | | |
|---|---|---|---|
| • Input capacitance | $C_{IN}$ | 9 (Max.) | pF |
| • Output capacitance | $C_{OUT}$ | 11 (Max.) | pF |
| • I/O capacitance | $C_{I/O}$ | 11 (Max.) | pF |





E04729A5Z

**Performance**

- Tracking sensitivity: –152dBm (average) or less
- Acquisition sensitivity: –139dBm (average) or less in normal mode
  –150dBm (average) or less in high sensitivity mode

  * Reference data using the Sony's reference board when using both an antenna of 25dBi gain and a RF amplifier with NF ≤ 2dB, 25dB gain.
- TTFF (Time to First Fix):

  Time until initial position measurement after power-on with the following conditions:

  Cold Start (without both ephemeris and almanac time): 50s (average) / 60s (95% possibility)

  Warm Start (without ephemeris but with almanac time): 35s (average) / 40s (95% possibility)

  Hot Start (with both ephemeris and almanac time): 2s (minimum) / 6s (95% possibility)

  * Reference data with elevation angle of 5° or more and no interception environment with satellite powers ≥ –130dBm. (Not in high sensitivity mode)

  **Note)** "95% possibility" means "position time with 95% possibility".
- Positioning accuracy:

  2DRMS: approx. 5m

  * Reference data with elevation angle of 5° or more and no interception environment with satellite powers ≥ –130dBm.
- Measurement data update time: 1s
- Current consumption:

  40mW (average) while position calculating with tracking satellites in low power mode

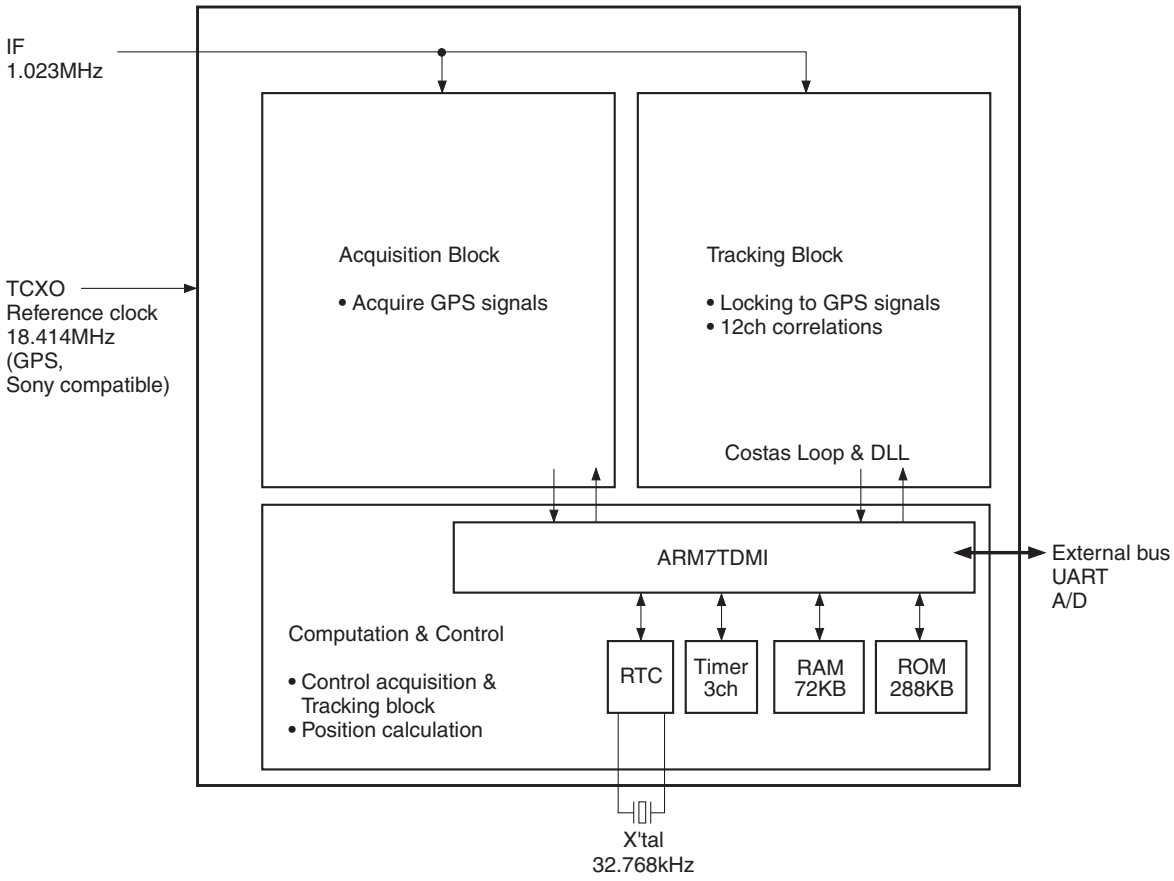
  90mW (average) while position calculating with acquiring and tracking satellites

  * Reference data using the Sony's reference board when the reference clock input is 18.414MHz, and its amplitude is 3.3V swing.
- 1PPS output

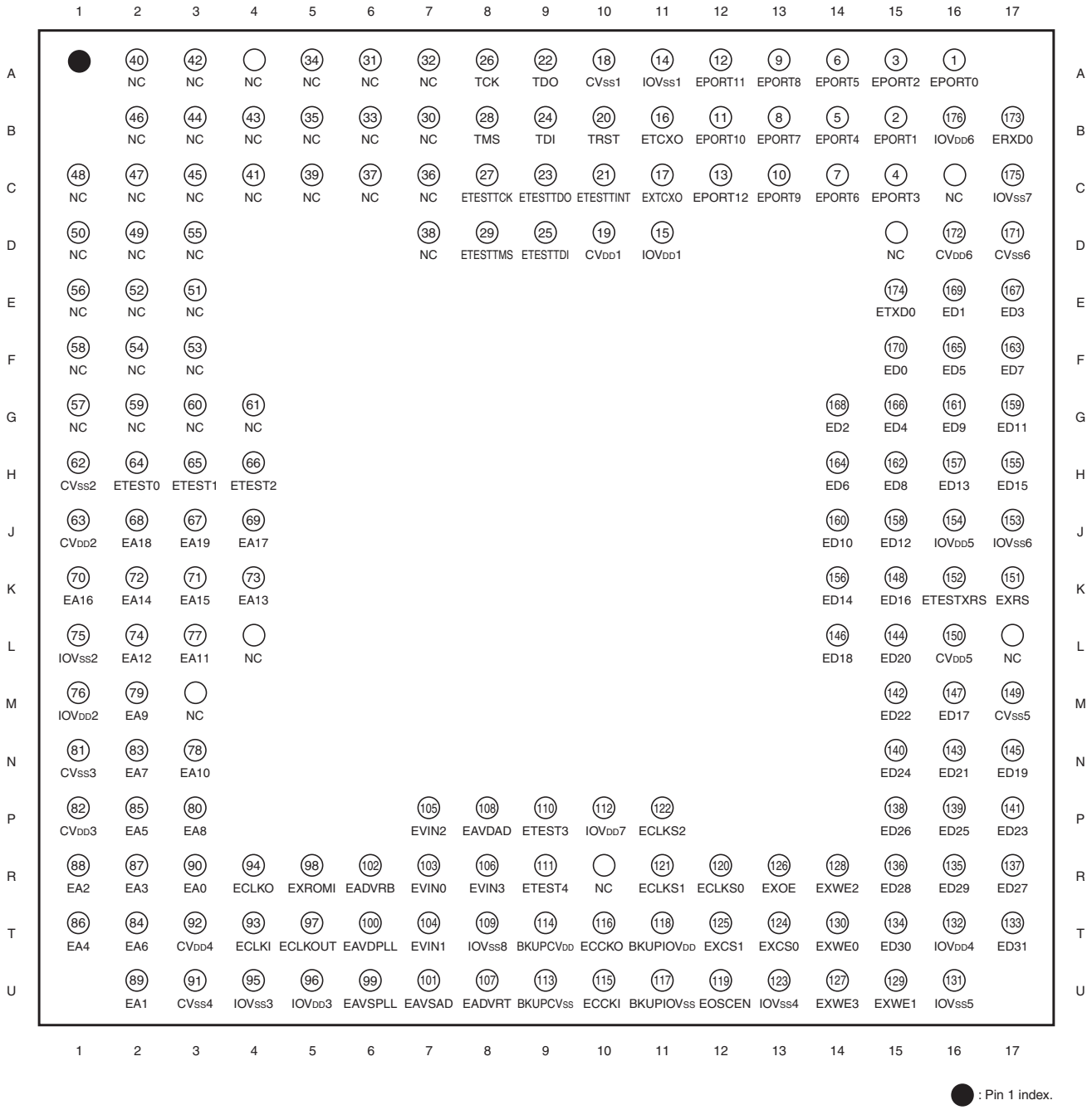
  1µs or less precision, 1PPS outputs from ECLKOUT (Pin 97).

**Note)** These values are not guaranteed, depending on the conditions.

## Block Diagram



## **Pin Configuration** (Top View)



| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | ● | 40 NC | 42 NC | ○ NC | 34 NC | 31 NC | 32 NC | 26 TCK | 22 TDO | 18 CVSS1 | 14 IOVSS1 | 12 EPORT11 | 9 EPORT8 | 6 EPORT5 | 3 EPORT2 | 1 EPORT0 | |
| B | | 46 NC | 44 NC | 43 NC | 35 NC | 33 NC | 30 NC | 28 TMS | 24 TDI | 20 TRST | 16 ETCXO | 11 EPORT10 | 8 EPORT7 | 5 EPORT4 | 2 EPORT1 | 176 IOVDD6 | 173 ERXD0 |
| C | 48 NC | 47 NC | 45 NC | 41 NC | 39 NC | 37 NC | 36 NC | 27 ETESTTCK | 23 ETESTTDO | 21 ETESTTINT | 17 EXTCXO | 13 EPORT12 | 10 EPORT9 | 7 EPORT6 | 4 EPORT3 | ○ NC | 175 IOVSS7 |
| D | 50 NC | 49 NC | 55 NC | | | | 38 NC | 29 ETESTTMS | 25 ETESTTDI | 19 CVDD1 | 15 IOVDD1 | | | | ○ NC | 172 CVDD6 | 171 CVSS6 |
| E | 56 NC | 52 NC | 51 NC | | | | | | | | | | | | 174 ETXD0 | 169 ED1 | 167 ED3 |
| F | 58 NC | 54 NC | 53 NC | | | | | | | | | | | | 170 ED0 | 165 ED5 | 163 ED7 |
| G | 57 NC | 59 NC | 60 NC | 61 NC | | | | | | | | | | 168 ED2 | 166 ED4 | 161 ED9 | 159 ED11 |
| H | 62 CVSS2 | 64 ETEST0 | 65 ETEST1 | 66 ETEST2 | | | | | | | | | | 164 ED6 | 162 ED8 | 157 ED13 | 155 ED15 |
| J | 63 CVDD2 | 68 EA18 | 67 EA19 | 69 EA17 | | | | | | | | | | 160 ED10 | 158 ED12 | 154 IOVDD5 | 153 IOVSS6 |
| K | 70 EA16 | 72 EA14 | 71 EA15 | 73 EA13 | | | | | | | | | | 156 ED14 | 148 ED16 | 152 ETESTXRS | 151 EXRS |
| L | 75 IOVSS2 | 74 EA12 | 77 EA11 | ○ NC | | | | | | | | | | 146 ED18 | 144 ED20 | 150 CVDD5 | ○ NC |
| M | 76 IOVDD2 | 79 EA9 | ○ NC | | | | | | | | | | | | 142 ED22 | 147 ED17 | 149 CVSS5 |
| N | 81 CVSS3 | 83 EA7 | 78 EA10 | | | | | | | | | | | | 140 ED24 | 143 ED21 | 145 ED19 |
| P | 82 CVDD3 | 85 EA5 | 80 EA8 | | | | 105 EVIN2 | 108 EAVDAD | 110 ETEST3 | 112 IOVDD7 | 122 ECLKS2 | | | | 138 ED26 | 139 ED25 | 141 ED23 |
| R | 88 EA2 | 87 EA3 | 90 EA0 | 94 ECLKO | 98 EXROMI | 102 EADVRB | 103 EVIN0 | 106 EVIN3 | 111 ETEST4 | ○ NC | 121 ECLKS1 | 120 ECLKS0 | 126 EXOE | 128 EXWE2 | 136 ED28 | 135 ED29 | 137 ED27 |
| T | 86 EA4 | 84 EA6 | 92 CVDD4 | 93 ECLKI | 97 ECLKOUT | 100 EAVDPLL | 104 EVIN1 | 109 IOVSS8 | 114 BKUPCVDD | 116 ECCKO | 118 BKUPIOVDD | 125 EXCS1 | 124 EXCS0 | 130 EXWE0 | 134 ED30 | 132 IOVDD4 | 133 ED31 |
| U | | 89 EA1 | 91 CVSS4 | 95 IOVSS3 | 96 IOVDD3 | 99 EAVSPLL | 101 EAVSAD | 107 EADVRT | 113 BKUPCVSS | 115 ECCKI | 117 BKUPIOVSS | 119 EOSCEN | 123 IOVSS4 | 127 EXWE3 | 129 EXWE1 | 131 IOVSS5 | |

● : Pin 1 index.

**Pin Description**

| Pin No. | Symbol | I/O | Description |
|---|---|---|---|
| 1 | EPORT0 | I/O/Z | I/O port 0<br>(with a software controllable pull-down resistor, Pull-up.) |
| 2 | EPORT1 | I/O/Z | I/O port 1<br>(with a software controllable pull-down resistor, See software application note.) |
| 3 | EPORT2 | I/O/Z | I/O port 2<br>(with a software controllable pull-down resistor, See software application note.) |
| 4 | EPORT3 | I/O/Z | I/O port 3<br>(with a software controllable pull-down resistor, See software application note.) |
| 5 | EPORT4 | I/O/Z | I/O port 4<br>(with a software controllable pull-down resistor, IF signal input.) |
| 6 | EPORT5 | I/O/Z | I/O port 5<br>(with a software controllable pull-down resistor, See software application note.) |
| 7 | EPORT6 | I/O/Z | I/O port 6<br>(with a software controllable pull-down resistor, See software application note.) |
| 8 | EPORT7 | I/O/Z | I/O port 7<br>(with a software controllable pull-down resistor, See software application note.) |
| 9 | EPORT8 | I/O/Z | I/O port 8<br>(with a software controllable pull-down resistor, See software application note.) |
| 10 | EPORT9 | I/O/Z | I/O port 9<br>(with a software controllable pull-down resistor, See software application note.) |
| 11 | EPORT10 | I/O/Z | I/O port 10<br>(with a software controllable pull-down resistor, See software application note.) |
| 12 | EPORT11 | I/O/Z | I/O port 11<br>(with a software controllable pull-down resistor, See software application note.) |
| 13 | EPORT12 | I/O/Z | I/O port 12<br>(with a software controllable pull-down resistor, See software application note.) |
| 14 | $IOV_{SS}1$ | | GND |
| 15 | $IOV_{DD}1$ | | 3.3V |
| 16 | ETCXO | I | TCXO oscillator (Frequency selectable, See software application note.) |
| 17 | EXTCXO | O | |
| 18 | $CV_{SS}1$ | | GND |
| 19 | $CV_{DD}1$ | | 1.8V |
| 20 | TRST | I | Test (Open, with a pull-down resistor) |
| 21 | ETESTTINT | O | Test |
| 22 | TDO | O | Test |
| 23 | ETESTTDO | O | Test |
| 24 | TDI | I | Test (Open, with a pull-up resistor) |
| 25 | ETESTTDI | I | Test (Open, with a pull-up resistor) |
| 26 | TCK | I | Test (Open, with a pull-down resistor) |
| 27 | ETESTTCK | I | Test (Open, with a pull-down resistor) |
| 28 | TMS | I | Test (Open, with a pull-up resistor) |

| Pin No. | Symbol | I/O | Description |
|---|---|---|---|
| 29 | ETESTTMS | I | Test (Open, with a pull-up resistor) |
| 30 | NC | | |
| 31 | NC | | |
| 32 | NC | | |
| 33 | NC | | |
| 34 | NC | | |
| 35 | NC | | |
| 36 | NC | | |
| 37 | NC | | |
| 38 | NC | | |
| 39 | NC | | |
| 40 | NC | | |
| 41 | NC | | |
| 42 | NC | | |
| 43 | NC | | |
| 44 | NC | | |
| 45 | NC | | |
| 46 | NC | | |
| 47 | NC | | |
| 48 | NC | | |
| 49 | NC | | |
| 50 | NC | | |
| 51 | NC | | |
| 52 | NC | | |
| 53 | NC | | |
| 54 | NC | | |
| 55 | NC | | |
| 56 | NC | | |
| 57 | NC | | |
| 58 | NC | | |
| 59 | NC | | |
| 60 | NC | | |
| 61 | NC | | |
| 62 | $CV_{SS}2$ | | GND |
| 63 | $CV_{DD}2$ | | 1.8V |

| Pin No. | Symbol | I/O | Description |
|---|---|---|---|
| 64 | ETEST0 | I | Test (Connect to GND.) |
| 65 | ETSET1 | I | |
| 66 | ETEST2 | I | |
| 67 | EA19 | O/Z | External expansion address 19 |
| 68 | EA18 | O/Z | External expansion address 18 |
| 69 | EA17 | O/Z | External expansion address 17 |
| 70 | EA16 | O/Z | External expansion address 16 |
| 71 | EA15 | O/Z | External expansion address 15 |
| 72 | EA14 | O/Z | External expansion address 14 |
| 73 | EA13 | O/Z | External expansion address 13 |
| 74 | EA12 | O/Z | External expansion address 12 |
| 75 | $IOV_{SS}2$ | | GND |
| 76 | $IOV_{DD}2$ | | 3.3V |
| 77 | EA11 | O/Z | External expansion address 11 |
| 78 | EA10 | O/Z | External expansion address 10 |
| 79 | EA9 | O/Z | External expansion address 9 |
| 80 | EA8 | O/Z | External expansion address 8 |
| 81 | $CV_{SS}3$ | | GND |
| 82 | $CV_{DD}3$ | | 1.8V |
| 83 | EA7 | O/Z | External expansion address 7 |
| 84 | EA6 | O/Z | External expansion address 6 |
| 85 | EA5 | O/Z | External expansion address 5 |
| 86 | EA4 | O/Z | External expansion address 4 |
| 87 | EA3 | O/Z | External expansion address 3 |
| 88 | EA2 | O/Z | External expansion address 2 |
| 89 | EA1 | O/Z | External expansion address 1 |
| 90 | EA0 | O/Z | External expansion address 0 |
| 91 | $CV_{SS}4$ | | GND |
| 92 | $CV_{DD}4$ | | 1.8V |
| 93 | ECLKI | I | CPU clock oscillator |
| 94 | ECLKO | O | |
| 95 | $IOV_{SS}3$ | | GND |
| 96 | $IOV_{DD}3$ | | 3.3V |
| 97 | ECLKOUT | O/Z | 1PPS output (Effective 1s late after reset release) |
| 98 | EXROMI | I | Boot selection (Low: Internal ROM, High: External Memory/EXCS0) |
| 99 | EAVSPLL | | PLL GND |
| 100 | EAVDPLL | | PLL 3.3V |

| Pin No. | Symbol | I/O | Description |
|---|---|---|---|
| 101 | EAVSAD | | A/D converter GND |
| 102 | EADVRB | I | A/D converter Reference input Bottom |
| 103 | EVIN0 | I | A/D converter Analog input 0 |
| 104 | EVIN1 | I | A/D converter Analog input 1 |
| 105 | EVIN2 | I | A/D converter Analog input 2 |
| 106 | EVIN3 | I | A/D converter Analog input 3 |
| 107 | EADVRT | I | A/D converter Reference input Top |
| 108 | EAVDAD | | A/D converter 3.3V |
| 109 | $IOV_{SS}8$ | | GND |
| 110 | ETEST3 | I/O/Z | Test (Connect to GND with a resistor.) |
| 111 | ETEST4 | I/O/Z | Test (Connect to GND with a resistor.) |
| 112 | $IOV_{DD}7$ | | 3.3V |
| 113 | $BKUPCV_{SS}$ | | Backup core power supply GND |
| 114 | $BKUPCV_{DD}$ | | Backup core power supply 1.8V |
| 115 | ECCKI | I | RTC oscillator (32.768kHz, includes feedback resistor.) |
| 116 | ECCKO | O | |
| 117 | $BKUPIOV_{SS}$ | | Backup I/O power supply GND |
| 118 | $BKUPIOV_{DD}$ | | Backup I/O power supply 3.3V |
| 119 | EOSCEN | I | Oscillator enable (H-Active), See backup mode section. |
| 120 | ECLKS0 | I | Test (Connect to GND.) |
| 121 | ECLKS1 | I | Test (Connect to GND.) |
| 122 | ECLKS2 | I | Test (Connect to GND.) |
| 123 | $IOV_{SS}4$ | | GND |
| 124 | EXCS0 | O/Z | External expansion chip selection 0 (Program boot is enable if EXROMI is high.) |
| 125 | EXCS1 | O/Z | External expansion chip selection 1 |
| 126 | EXOE | O/Z | External expansion read signal |
| 127 | EXWE3 | O/Z | External expansion write signal |
| 128 | EXWE2 | O/Z | External expansion write signal |
| 129 | EXWE1 | O/Z | External expansion write signal |
| 130 | EXWE0 | O/Z | External expansion write signal |
| 131 | $IOV_{SS}5$ | | GND |
| 132 | $IOV_{DD}4$ | | 3.3V |
| 133 | ED31 | I/O | External expansion data 31 (with a pull-down resistor) |
| 134 | ED30 | I/O | External expansion data 30 (with a pull-down resistor) |
| 135 | ED29 | I/O | External expansion data 29 (with a pull-down resistor) |
| 136 | ED28 | I/O | External expansion data 28 (with a pull-down resistor) |
| 137 | ED27 | I/O | External expansion data 27 (with a pull-down resistor) |
| 138 | ED26 | I/O | External expansion data 26 (with a pull-down resistor) |

| Pin No. | Symbol | I/O | Description |
|---|---|---|---|
| 139 | ED25 | I/O | External expansion data 25 (with a pull-down resistor) |
| 140 | ED24 | I/O | External expansion data 24 (with a pull-down resistor) |
| 141 | ED23 | I/O | External expansion data 23 (with a pull-down resistor) |
| 142 | ED22 | I/O | External expansion data 22 (with a pull-down resistor) |
| 143 | ED21 | I/O | External expansion data 21 (with a pull-down resistor) |
| 144 | ED20 | I/O | External expansion data 20 (with a pull-down resistor) |
| 145 | ED19 | I/O | External expansion data 19 (with a pull-down resistor) |
| 146 | ED18 | I/O | External expansion data 18 (with a pull-down resistor) |
| 147 | ED17 | I/O | External expansion data 17 (with a pull-down resistor) |
| 148 | ED16 | I/O | External expansion data 16 (with a pull-down resistor) |
| 149 | $CV_{SS}5$ | | GND |
| 150 | $CV_{DD}5$ | | 1.8V |
| 151 | EXRS | I | Reset (L-Active) |
| 152 | ETESTXRS | I | Test (Open, with a pull-up resistor) |
| 153 | $IOV_{SS}6$ | | GND |
| 154 | $IOV_{DD}5$ | | 3.3V |
| 155 | ED15 | I/O | External expansion data 15 (with a pull-down resistor) |
| 156 | ED14 | I/O | External expansion data 14 (with a pull-down resistor) |
| 157 | ED13 | I/O | External expansion data 13 (with a pull-down resistor) |
| 158 | ED12 | I/O | External expansion data 12 (with a pull-down resistor) |
| 159 | ED11 | I/O | External expansion data 11 (with a pull-down resistor) |
| 160 | ED10 | I/O | External expansion data 10 (with a pull-down resistor) |
| 161 | ED9 | I/O | External expansion data 9 (with a pull-down resistor) |
| 162 | ED8 | I/O | External expansion data 8 (with a pull-down resistor) |
| 163 | ED7 | I/O | External expansion data 7 (with a pull-down resistor) |
| 164 | ED6 | I/O | External expansion data 6 (with a pull-down resistor) |
| 165 | ED5 | I/O | External expansion data 5 (with a pull-down resistor) |
| 166 | ED4 | I/O | External expansion data 4 (with a pull-down resistor) |
| 167 | ED3 | I/O | External expansion data 3 (with a pull-down resistor) |
| 168 | ED2 | I/O | External expansion data 2 (with a pull-down resistor) |
| 169 | ED1 | I/O | External expansion data 1 (with a pull-down resistor) |
| 170 | ED0 | I/O | External expansion data 0 (with a pull-down resistor) |
| 171 | $CV_{SS}6$ | | GND |
| 172 | $CV_{DD}6$ | | 1.8V |
| 173 | ERXD0 | I | UART (CH0) reception data (with a pull-down resistor during reset interval) |
| 174 | ETXD0 | O/Z | UART (CH0) transmission data (with Hi-Z during reset interval) |
| 175 | $IOV_{SS}7$ | | GND |
| 176 | $IOV_{DD}6$ | | 3.3V |

**A/D Converter Operating Conditions**

| Item | Symbol | Pin name | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{AD}$ | EAVDAD*1 | 3.0 | 3.3 | 3.6 | V |
| Operating temperature | Ta | — | –40.0 | | +85.0 | °C |

**A/D Converter Characteristics** ($V_{AD}$ = 3.0 to 3.6V, Ta = –40 to +85°C)

| Item | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Resolution | | | | | 10 | Bit |
| Channel | | | | | 4 | Ch |
| Differential linearity error (DLE) | | $V_{AD}$ = 3.0V, $V_{RT}$ = 3.0V, $V_{RB}$ = 0.3V | –1.0 | | +1.0 | LSB |
| Integral linearity error (ILE) | | | –2.0 | | +2.0 | LSB |
| Sampling time | | TCXO = 18.414MHz | 3 | | | µs |
| Conversion time | | | | | 11 | µs |
| Reference input voltage (Top) | $V_{RT}$*2 | | 2.0 | | $V_{AD}$ | V |
| Reference input voltage (Bottom) | $V_{RB}$*3 | | 0 | | 0.7 | V |
| Analog input voltage | $V_{IN}$*4 | | $V_{RB}$ | | $V_{RT}$ | V |
| Current consumption | | $V_{AD}$ = 3.0V | | 1.6 | | mA |

**Applicable pins**

*1 EAVDAD (Pin 108)

*2 EADVRT (Pin 107)

*3 EADVRB (Pin 102)

*4 EVIN[0:3] (Pins 103 to 106)

**DC Characteristics** ($IOV_{DD}$ = 3.0 to 3.6V, $CV_{DD}$ = 1.62 to 1.98V, Ta = –40 to +85°C)

| Item | | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage*1 | High level | $V_{IH}$ | | 0.7$IOV_{DD}$ | | 5.5 | V |
| | Low level | $V_{IL}$ | | | | 0.2$IOV_{DD}$ | V |
| Output voltage*2 | High level | $V_{OH1}$ | $I_{OH}$ = 4mA | 2.4 | | | V |
| | Low level | $V_{OL1}$ | $I_{OL}$ = 4mA | | | 0.4 | V |
| Output voltage*3 | High level | $V_{OH2}$ | $I_{OH}$ = 8mA | 2.4 | | | V |
| | Low level | $V_{OL2}$ | $I_{OL}$ = 8mA | | | 0.4 | V |
| Pull-up resistor*4 | | $R_U$ | | 56 | | 110 | kΩ |
| Pull-down resistor*5 | | $R_D$ | | 51 | | 100 | kΩ |
| Current consumption during normal operation (via $IOV_{DD}$ and $CV_{DD}$)*6 | | $I_{OPE}$ | TCXO = 18.414MHz, Ta = 25°C | | 45 | | mA |
| Current consumption during backup operation (via $BKUPIOV_{DD}$)*7 | | $I_{STB1}$ | $BKUPIOV_{DD}$ = 3.6V, Ta = 25°C | | 0.2 | 1.0 | µA |
| | | | $BKUPIOV_{DD}$ = 3.6V, Ta = 85°C | | 0.2 | 1.0 | µA |
| Current consumption during backup operation (via $BKUPCV_{DD}$)*8 | | $I_{STB2}$ | $BKUPCV_{DD}$ = 1.98V, Ta = 25°C | | 7.5 | 15 | µA |
| | | | $BKUPCV_{DD}$ = 1.98V, Ta = 85°C | | 50 | 120 | µA |

**Applicable pins**

*1 Pins 1 to 13, 20, 24 to 29, 64 to 66, 98, 119, 120 to 122, 133 to 148, 151, 152, 155 to 170, 173

*2 Pins 1 to 13, 21 to 23, 97, 174

*3 Pins 67 to 74, 77 to 80, 83 to 90, 124 to 130, 133 to 148, 155 to 170

*4 Pins 24, 25, 28, 29, 152

*5 Pins 1 to 13, 20, 26, 27, 133 to 148, 155 to 170, 173

*6 Pins 15, 76, 96, 132, 154, 176 (3.3V)
Pins 19, 63, 82, 92, 150, 172 (1.8V)

*7 Pin 118

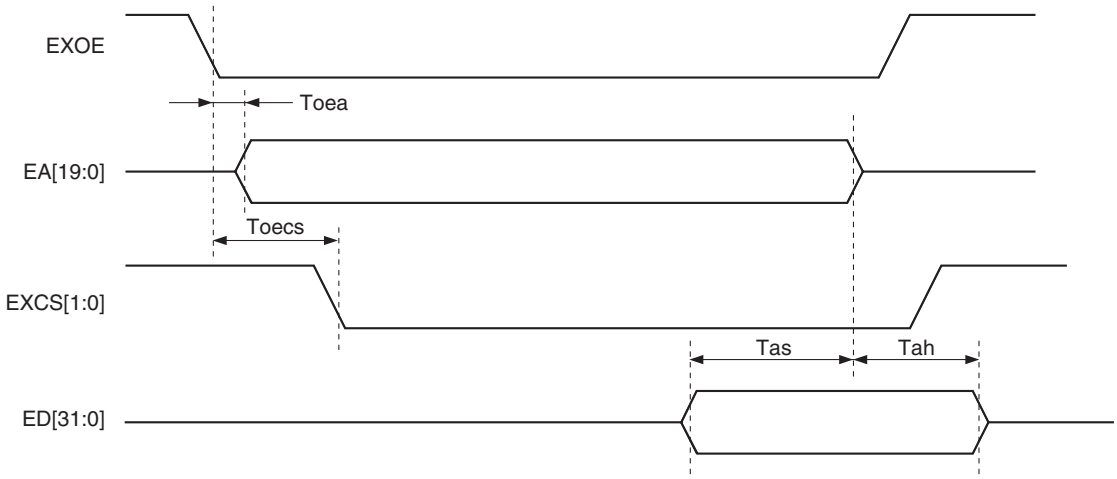
*8 Pin 114

## AC Characteristics

### • External RAM I/F (Read/32-bit mode)

($CV_{DD}$ = 1.62 to 1.98V, $IOV_{DD}$ = 3.0 to 3.6V, $C_L$ = 25pF, Topr = –40 to +85°C)

| Item | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| EXOE ↓ to address valid | Toea | | 3 | ns |
| EXOE ↓ to EXCS ↓ | Toecs | | 1 | ns |
| Data setup | Tas | | 15 | ns |
| Data hold | Tah | | 0 | ns |

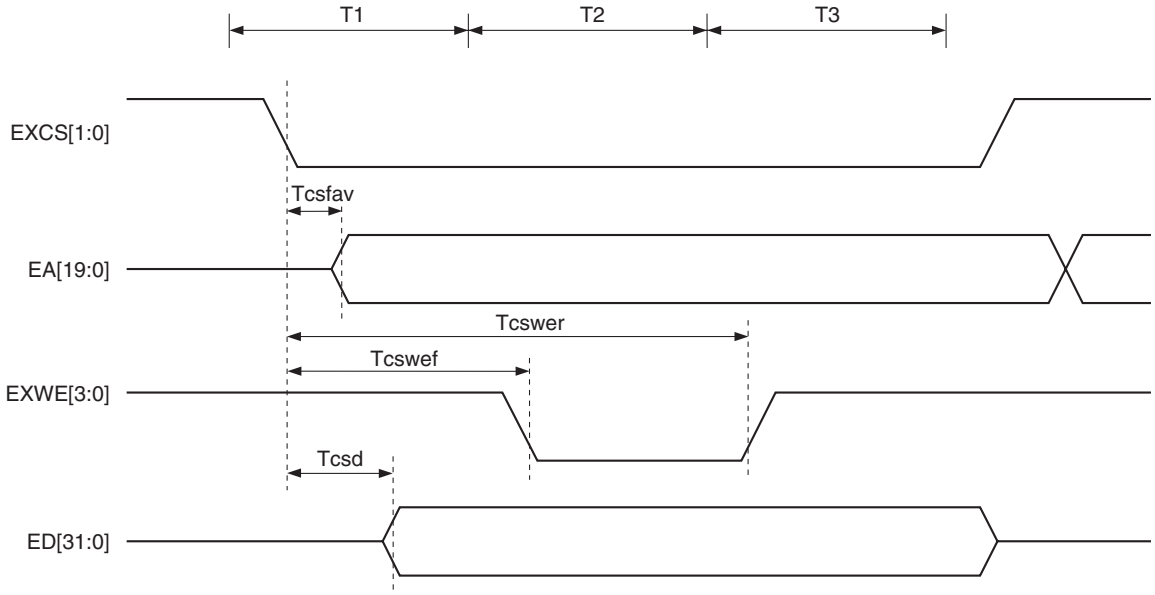


**• External RAM I/F (Write/32-bit mode (1-wait))**

($CV_{DD}$ = 1.62 to 1.98V, $IOV_{DD}$ = 3.0 to 3.6V, $C_L$ = 25pF, Topr = –40 to +85°C)

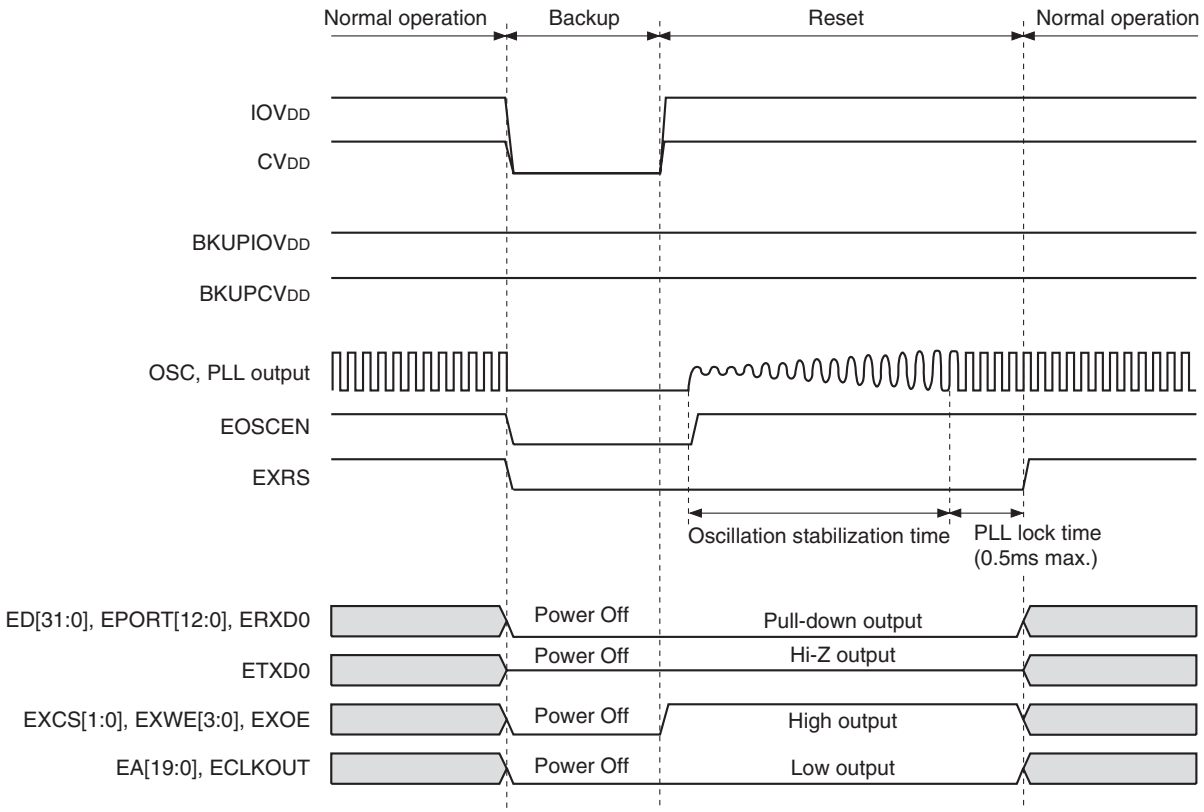
| Item | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| EXCS ↓ to address valid | Tcsfav | | 2 | ns |
| EXCS ↓ to EXWE ↓ | Tcswef | | Tsys – 1 | ns |
| EXCS ↓ to EXWE ↑ | Tcswer | | Tsys × 3 – 2 | ns |
| EXCS ↓ to data valid | Tcsd | | 15 | ns |

* Tsys: ARM clock cycle



**Backup Mode**

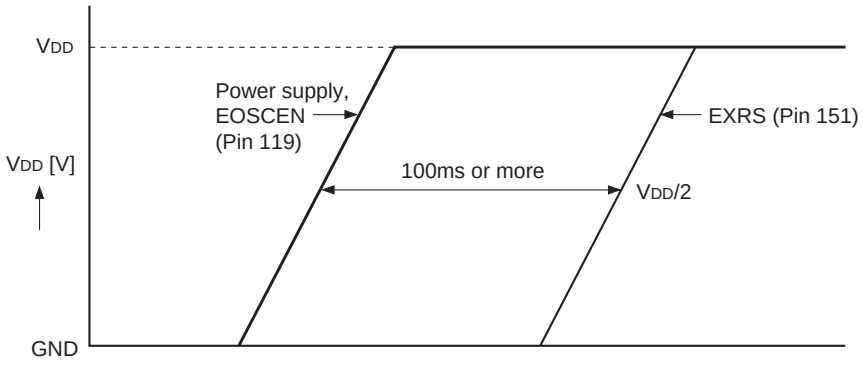
The backup mode is established by setting both EOSCEN and EXRS low. In this mode, the low power consumption can be achieved by stopping all oscillators except for RTC oscillator during the reset interval. Although all registers are initialized, the SRAM contents in backup area are held.
In order to cancel this mode (reset cancellation), please set EOSCEN high at first and then set EXRS high after the oscillation stabilization time and PLL lock time have passed. It needs 100ms or more.
See Initialization section.



**Initialization**

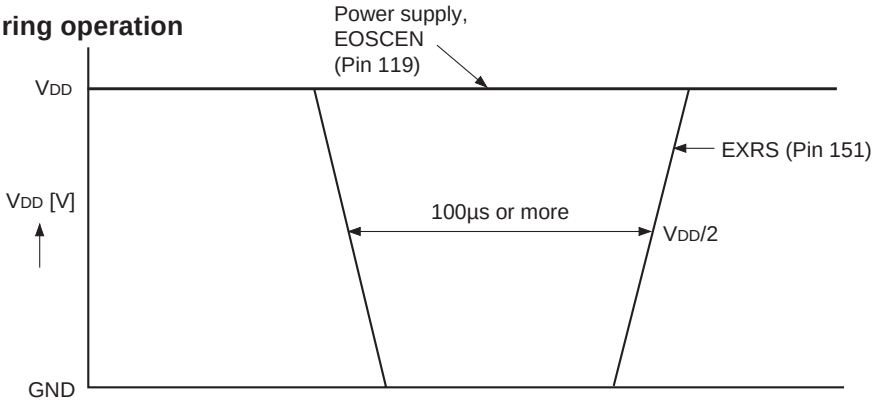
The CXD2956AGL-1 is initialized by setting the reset signal EXRS (Pin 151) to the low level. Note that internal RAM is not initialized by the operation. Satisfy the conditions shown below for the timing and others.

**1. When turning the power on (Power-on reset)**




Since there is a possibility that overcurrent may flow, please be sure to add power supply to the LSI before activate functional pin of this LSI. Additionally, the power supply both 3.3V and 1.8V should turn on simultaneously, and EOSCEN (Pin 119) should also rise simultaneously with the power supply turning on. EXRS (Pin 151) should rise 100ms or more after the power supply and EOSCEN rise.

**2. Initialization during operation**




For initialization during operation, the interior circuit except internal RAM is initialized by setting the EXRS (Pin 151) signal to the low level for 100µs or more. Note that internal RAM is not also initialized by the operation. At this time, the EOSCEN (Pin 119) signal should keep the high level.

## RTC Crystal and TCXO

In order to operate CXD2956AGL-1 appropriately, the recommended characteristics of RTC crystal and TCXO is shown below.

### Recommended characteristics of RTC crystal

| | |
|---|---|
| Operating temperature | –40 to +85°C |
| Nominal frequency | 32.768kHz |
| Frequency tolerance | ±20ppm |
| Frequency temperature coefficient | –0.04ppm/°C$^2$ (Max.) |
| Frequency peak temperature | +25 ± 5°C |
| Frequency aging | ±3ppm/year |

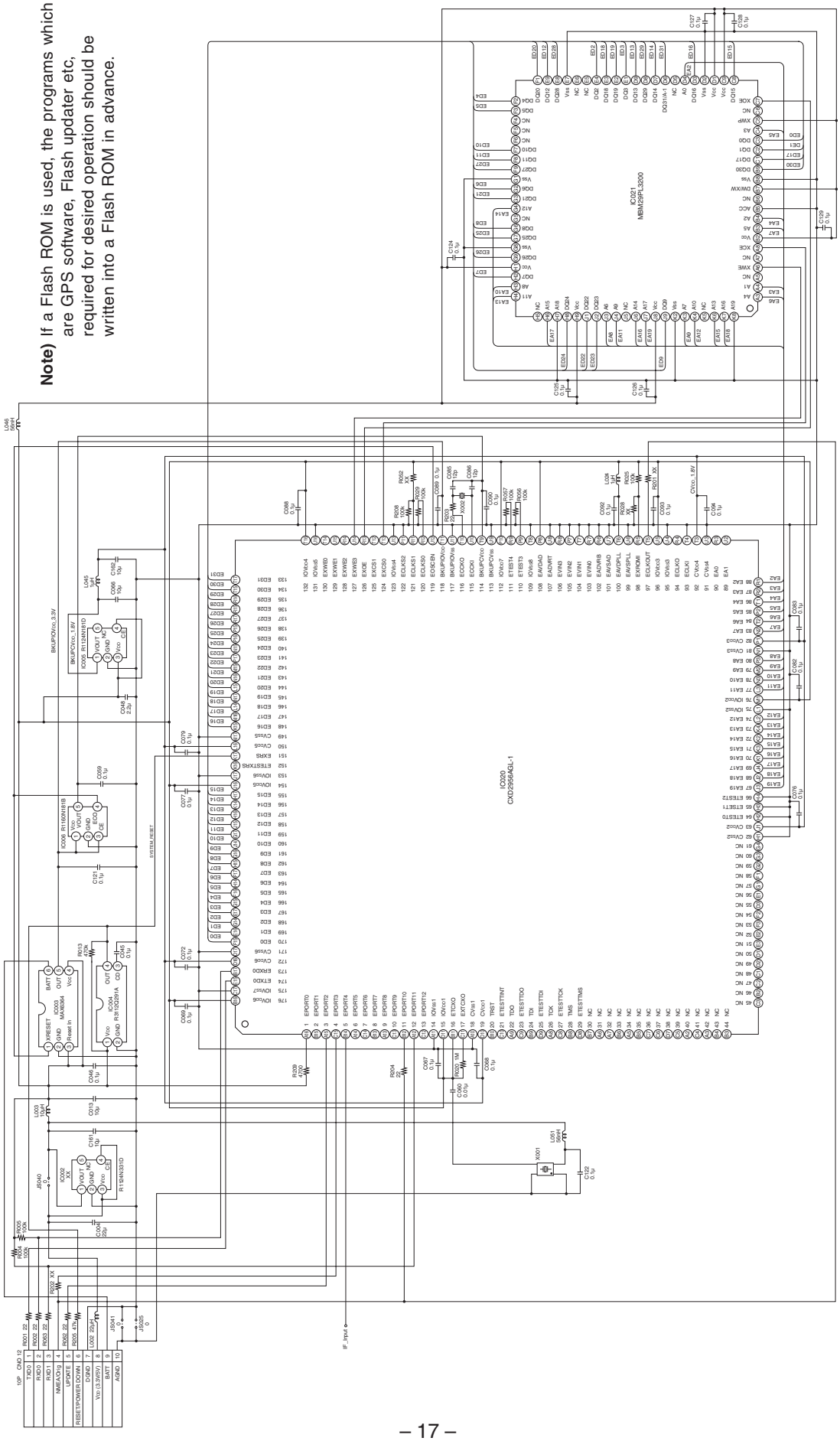
### Recommended characteristics of TCXO

| | |
|---|---|
| Operating temperature | –40 to +85°C |
| Frequency tolerance | ±2.0ppm |
| Frequency vs. temperature | ±2.5ppm |
| Frequency vs. supply voltage | ±0.2ppm |
| Frequency vs. load | ±0.2ppm |
| Frequency aging | ±1ppm/year |

### Recommended parts

| | |
|---|---|
| RTC crystal | EPSON FC-255 |
| TCXO | NDK SNA3088B (NT5032 Series) |

## Application Circuit

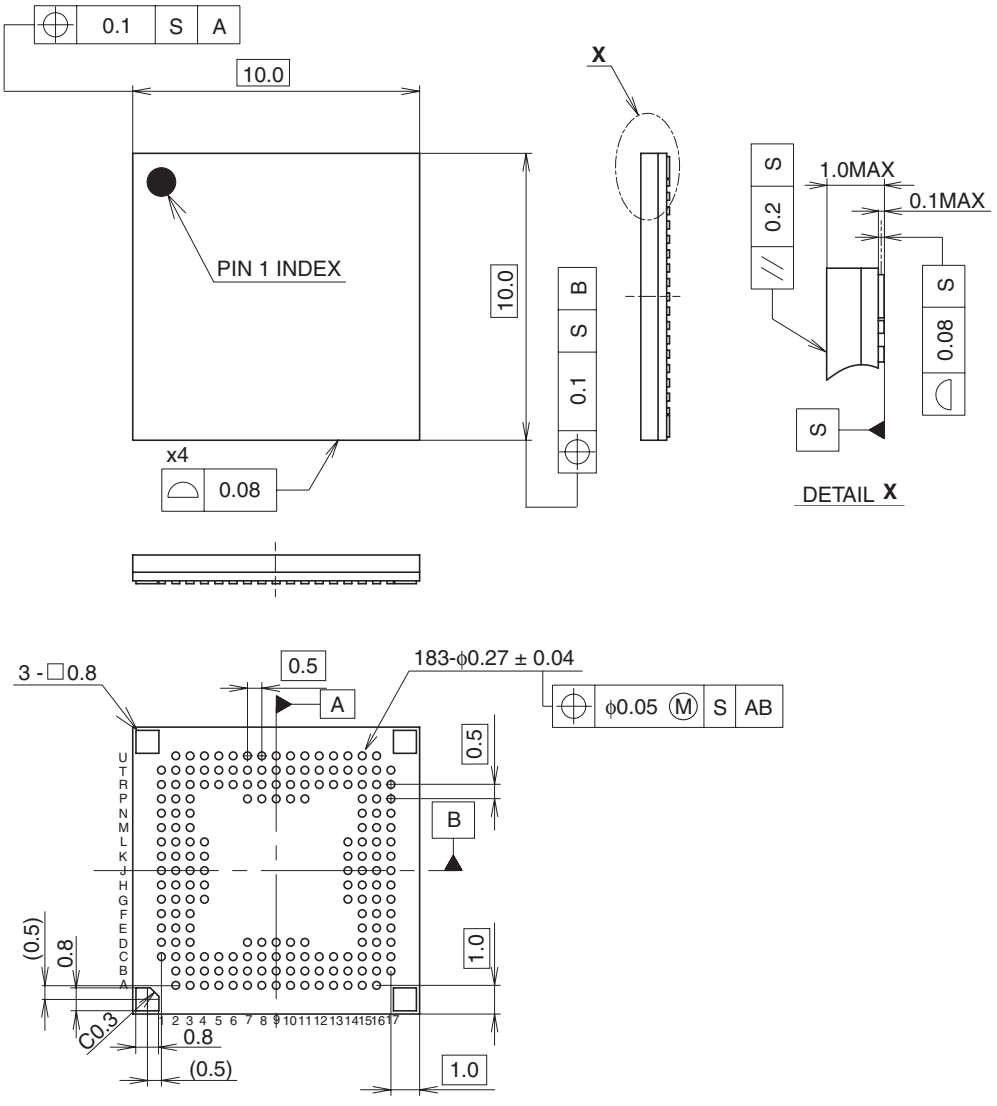


**Note)** If a Flash ROM is used, the programs which are GPS software, Flash updater etc, required for desired operation should be written into a Flash ROM in advance.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

**Package Outline** Unit: mm

183PIN VFLGA (PLASTIC)




| | |
|---|---|
| SONY CODE | VFLGA-183P-051 |
| EIAJ CODE | P-VFLGA183-10X10-0.5 |
| JEDEC CODE | ———— |

| | |
|---|---|
| PACKAGE MATERIAL | ORGANIC SUBSTRATE |
| TERMINAL TREATMENT | NICKEL & GOLD PLATING |
| TERMINAL MATERIAL | COPPER |
| PACKAGE MASS | 0.3g |