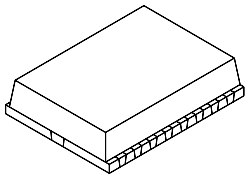
SONY

CXG1122EN

SP5T GSM Triple-Band/GPRS Antenna Switch

16 pin VSON (Plastic)



Description

The CXG1122EN is one of a range of low insertion loss, high power MMIC antenna switches for GSM/GPRS triple-band, dual-band (CXG1121TN) and applications. The low insertion loss on transmit means increased talk time as the Tx power amplifier can be operated at a lower output level. On-chip logic reduces the component count and simplifies the PCB layout by allowing the direct connection of the switch to digital baseband control lines with the CMOS logic levels.

This switch is an SP5T, one antenna can be routed to either of the 2 Tx or 3 Rx ports. It requires 3 CMOS control lines (CTL1, CTL2 and Tx ON).

The Sony's GaAs JFET process is used for low insertion loss. An evaluation PCB is available.

Features

- Insertion loss: (Tx) 0.5dB typ. at 34dBm (GSM900)
- 3 CMOS compatible control lines
- Low second harmonic: –40dBm typ. at 34dBm (GSM900)
- Small package size: 16-pin VSON (2.7mm × 3.5mm × 0.9mm)

Applications

Triple-band handsets using the combinations of followings:

- GSM900/DCS1800/PCS1900
- GPRS
- DECT

Structure

GaAs J-FET MMIC

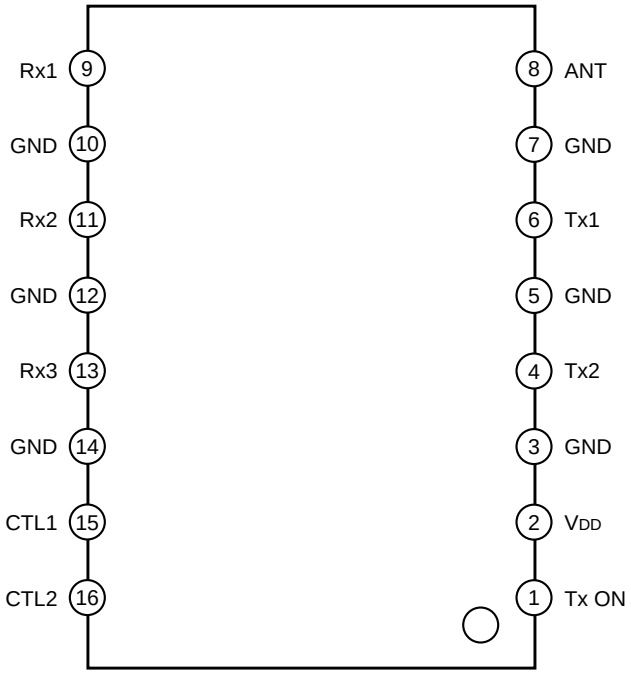
Absolute Maximum Ratings (Ta = 25°C)

• Bias voltage	V_{DD}	7	V
• Control voltage	V_{CTL}	5	V
• Operating temperature	Topr	–20 to +80	°C

GaAs MMICs are ESD sensitive devices. Special handling precautions are required.

E01Z20-PS

Pin Configuration



Truth Table

On Pass	CTL1	CTL2	Tx ON
ANT – Tx1 GSM900	H	Don't care	H
ANT – Tx2 DCS1800 & PCS1900	L	Don't care	H
ANT – Rx1 GSM900/DCS1800/PCS1900	H	L	L
ANT – Rx2 GSM900/DCS1800/PCS1900	L	L	L
ANT – Rx3 GSM900/DCS1800/PCS1900	L	H	L

Electrical characteristics (Ta = 25°C)

Item	Symbol	Path	Condition	Min.	Typ.	Max.	Unit
Insertion loss	IL	Tx1, Tx2 – ANT	*1		0.5	0.7	dB
		Tx1, Tx2 – ANT	*2		1.0	1.2	dB
		Rx1 – ANT	*3		0.65	0.85	dB
		Rx2 – ANT	*4		1.2	1.4	dB
		Rx3 – ANT	*5		1.2	1.4	dB
Isolation	ISO	ANT – Tx1, Tx2	*3	18	20		dB
			*4, *5	14	16		dB
		Tx – Rx1, Rx2, Rx3	*1	23	25		dB
		Tx – Rx1, Rx2, Rx3	*2	18	20		dB
VSWR	VSWR				1.2		
Harmonics*	2fo	Tx1, Tx2 – ANT	*1, *2		–40	–36	dBm
	3fo				–34	–30	dBm
P_{1dB} compression input power	P_{1dB}	Tx1, Tx2 – ANT	*1, *2		36		dBm
Control current	I_{CTL}		V_{CTL} = 3.0V		80	120	µA
Supply current for Tx and Rx modes	I_{TX}/I_{RX}		V_{DD} = 3.3V		0.3	1	mA

Electrical characteristics are measured with all the RF ports terminated in 50Ω.

* Harmonics measured with Tx inputs harmonically matched. It is recommended that the harmonic matching is used to ensure the optimum performance.

*1 Power incident on GSM Tx, Pin = 34dBm, 880 to 915MHz, V_{DD} = 3.3V, GSM Tx enabled

*2 Power incident on DCS/PCS Tx, Pin = 32dBm, 1710 to 1910MHz, V_{DD} = 3.3V, DCS/PCS Tx enabled

*3 Power incident on ANT, Pin = 10dBm, 925 to 960MHz, V_{DD} = 3.3V, GSM Rx enabled

*4 Power incident on ANT, Pin = 10dBm, 1805 to 1880MHz, V_{DD} = 3.3V, DCS Rx enabled

*5 Power incident on ANT, Pin = 10dBm, 1930 to 1990MHz, V_{DD} = 3.3V, PCS Rx enabled

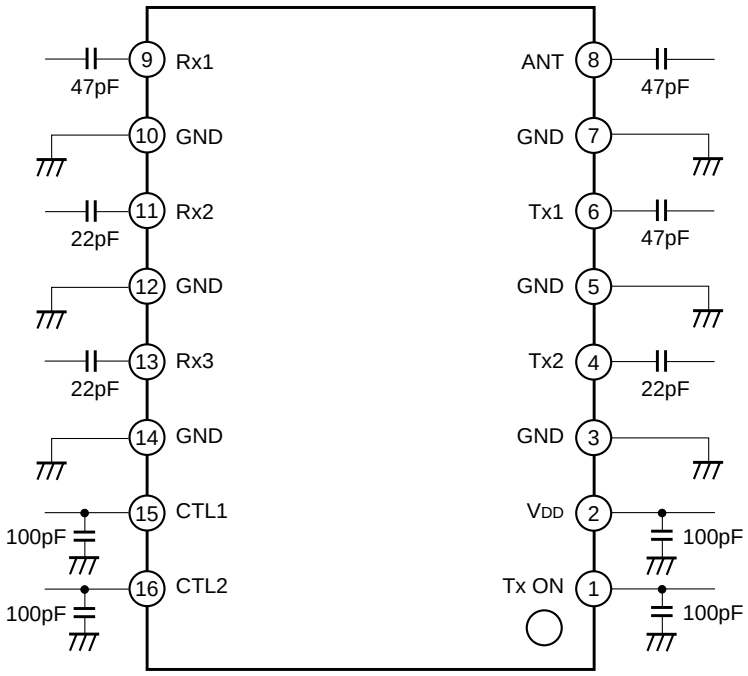
Supply Voltage Value (V_{DD})

Mode	Min.	Typ.	Max.	Unit
GSM/DCS Tx	3.0	3.3	3.5	V
GSM/DCS/PCS Rx	2.7	3.0	3.5	V

CMOS Logic Value

Logic	Min.	Typ.	Max.	Unit
High	2.4	2.8	3.2	V
Low	0		0.4	V

DC Block Capacitors and Decoupling Capacitors

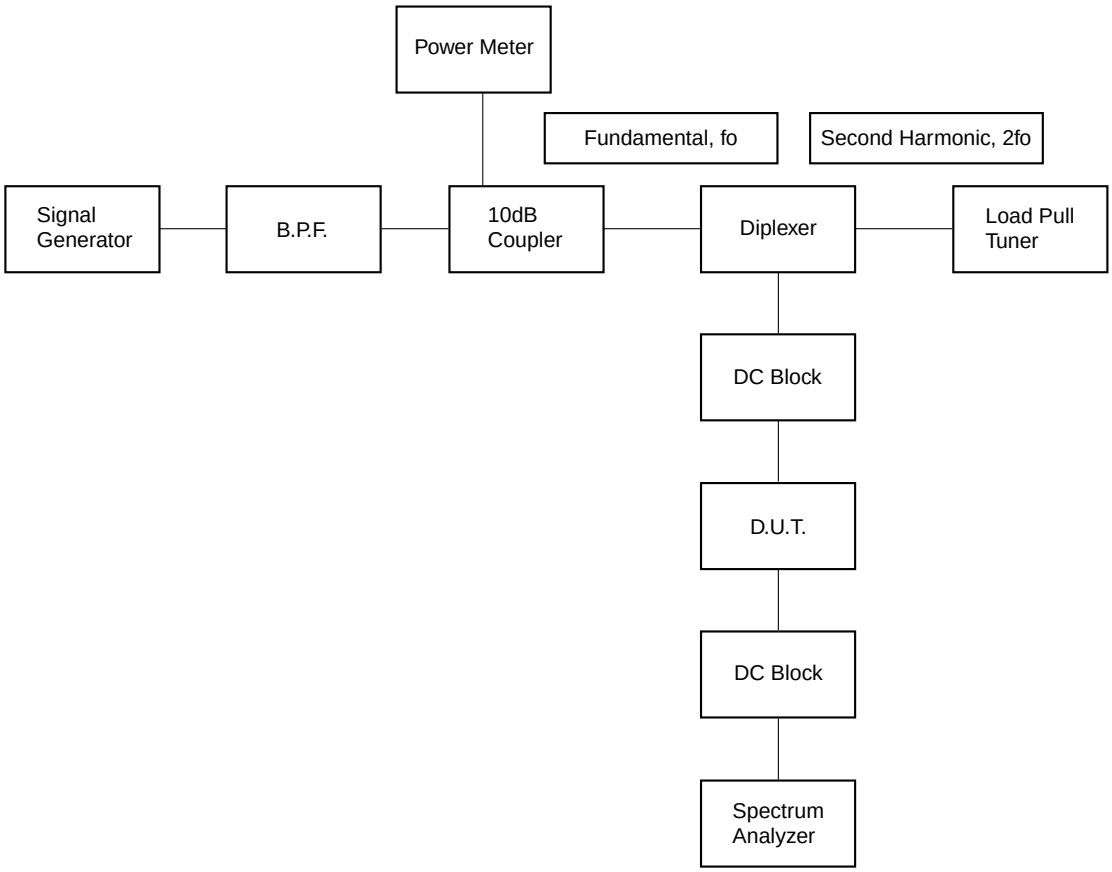


Note) Capacitors are required on all the RF ports for DC blocking (22pF – 47pF). Decoupling capacitors are required on V_{DD} and on control lines.

Application Note

Impedance Matching for Harmonic Minimization

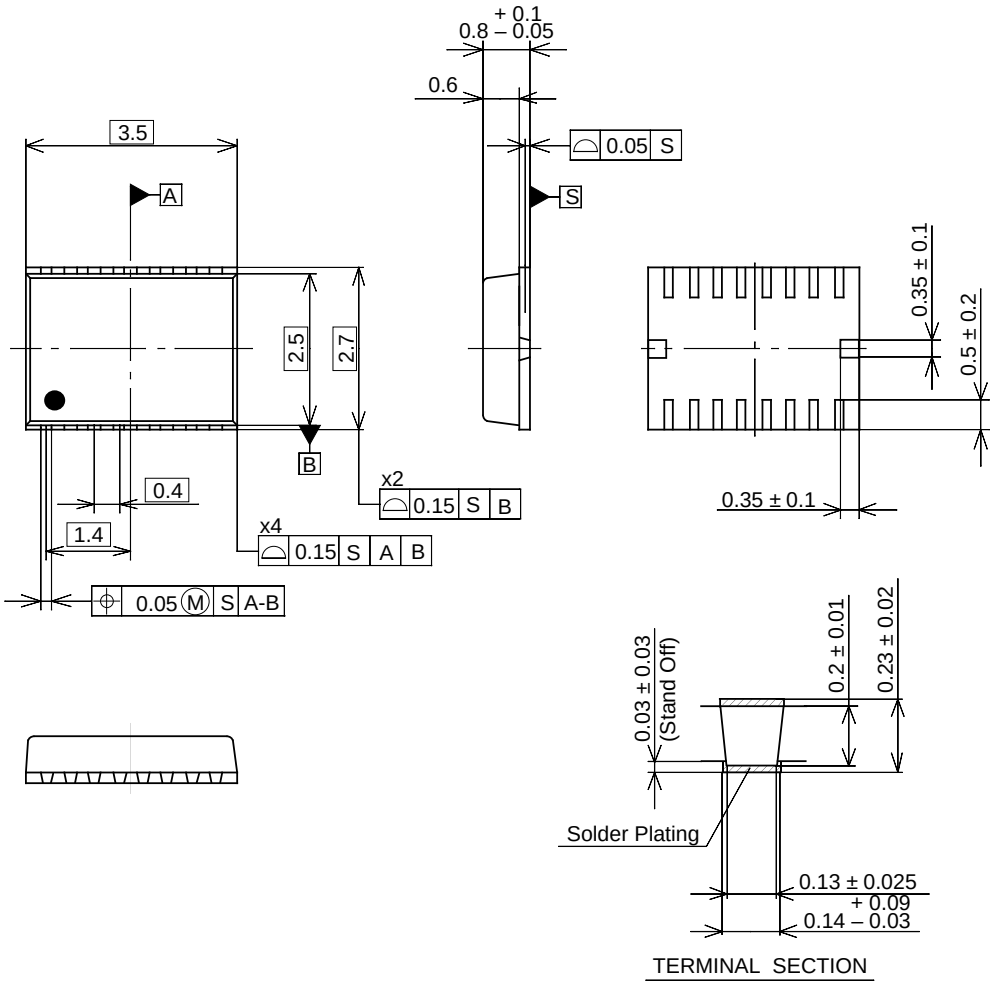
This note outlines the method used to find the source impedance to present to a transmit port at the second harmonic frequency (2fo) to reduce the second harmonic level at the antenna.
This should be carried out for a set of devices that represent the process variants. This way a compromise can be found that suits all the variants.
The necessary equipment is shown immediately below.



The device should be mounted on a PCB with 50Ω tracks running from all the RF pins to SMA connectors on the PCB edge (DUT). All the ports should be externally DC blocked and the unused ports should be terminated in 50Ω. All the measurements should be performed at the incident powers for which the harmonic levels are specified in this document.
The 2nd harmonic level at the antenna port is measured using the spectrum analyzer and the vertical and horizontal position of the load pull stub adjusted such that this level is minimized.
The device should then be removed from the board and an SMA connector mounted such that the source impedance seen by the transmit port at 2fo can be measured using a VNA.
Measurements should be de-embedded to the end of the SMA center pin.
A network should then be designed to match the impedance of the low pass filter (LPF), which usually comes in front of the device, to the 2fo source impedance that gives sufficiently reduced 2fo levels for all the devices measured.
The network should be designed to maintain a good match and insertion loss at the fundamental frequency.

Package Outline Unit: mm

16PIN VSON (PLASTIC)



NOTE: 1) The dimensions of the terminal section apply to the ranges of 0.1mm and 0.25mm from the end of a terminal.

SONY CODE	VSON-16P-01
EIAJ CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.02 g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm