

# CXK58512TM/M -55LL\*/70LL/10LL

## 65536-word × 8-bit High Speed CMOS Static RAM

\*Under development

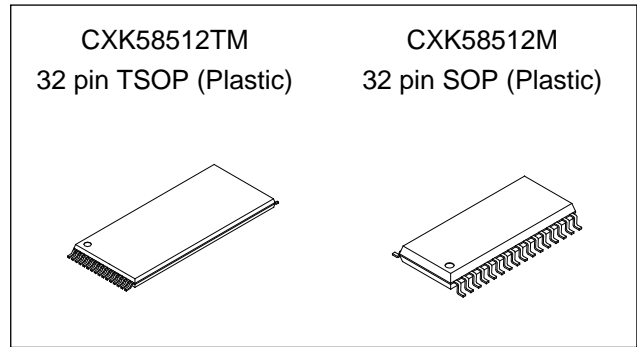
**Description**

The CXK58512TM/M is a high speed CMOS static RAM organized as 65536-words by 8 bits.

A polysilicon TFT cell technology realized extremely low stand-by current and higher data retention stability.

Special feature are low power consumption, high speed.

The CXK58512TM/M is a suitable RAM for portable equipment with battery back up.



**Features**

- Fast access time (Access time)
  - 55LL 55ns (Max.)
  - 70LL 70ns (Max.)
  - 10LL 100ns (Max.)
- Low standby current 10µA (Max.)
- Low data retention current 6µA (Max.)
- Single +5V supply: +5V ± 10%
- Low voltage data retention: 2.0V (Min.)
- Broad package line-up
  - CXK58512TM 8mm × 20mm 32 pin TSOP package
  - CXK58512M 525mil 32 pin SOP Package

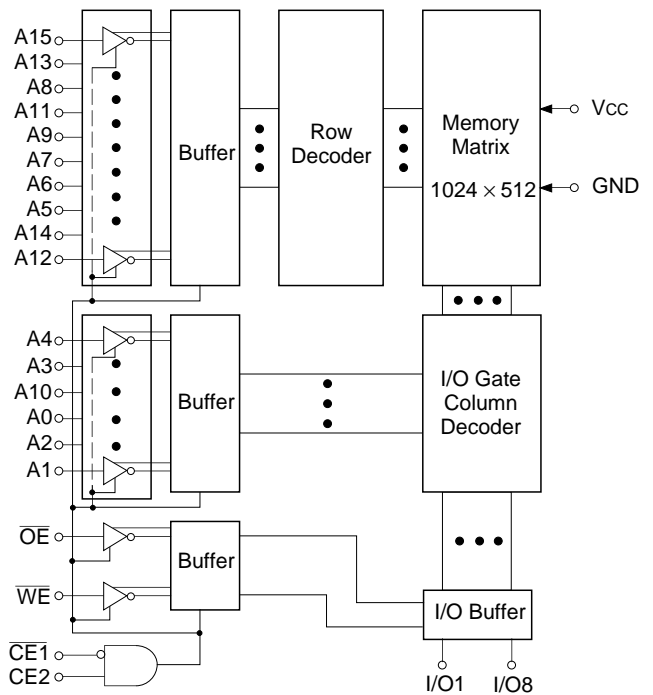
**Function**

65536-word × 8 bit static RAM

**Structure**

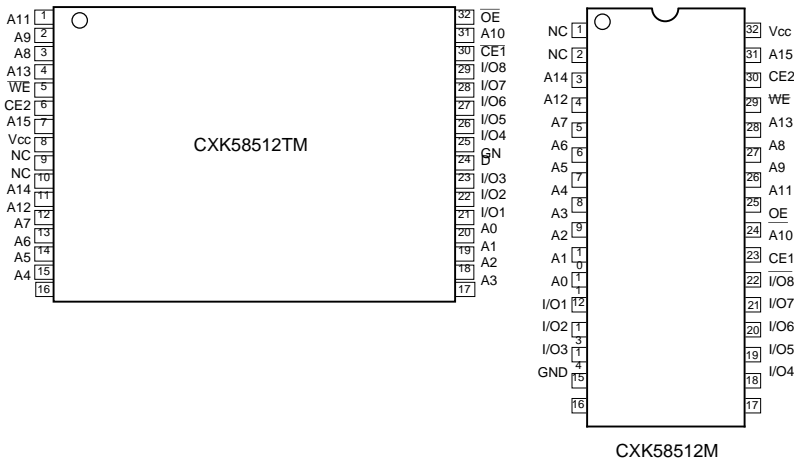
Silicon gate CMOS IC

**Block Diagram**



Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A15	Address input
I/O1 to I/O8	Data input output
$\overline{\text{CE1}}, \text{CE2}$	Chip enable 1, 2 input
$\overline{\text{WE}}$	Write enable input
$\overline{\text{OE}}$	Output enable input
Vcc	Power supply
GND	Ground
NC	No connection

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	Vcc	-0.5 to +7.0	V
Input voltage	V <sub>IN</sub>	-0.5* to Vcc + 0.5	V
Input and output voltage	V <sub>I/O</sub>	-0.5* to Vcc + 0.5	V
Allowable power dissipation	P <sub>D</sub>	0.7	W
Operating temperature	T <sub>opr</sub>	0 to +70	°C
Storage temperature	T <sub>stg</sub>	-55 to +150	°C
Soldering temperature • time	T <sub>solder</sub>	235 • 10	°C • s

\* V<sub>IN</sub>, V<sub>I/O</sub> = -3.0V Min. for pulse width less than 50ns.

Truth Table

$\overline{\text{CE1}}$	CE2	$\overline{\text{OE}}$	$\overline{\text{WE}}$	Mode	I/O pin	Vcc Current
H	x	x	x	Not selected	High Z	ISB1, ISB2
x	L	x	x	Not selected	High Z	ISB1, ISB2
L	H	H	H	Output disable	High Z	Icc1, Icc2, Icc3
L	H	L	H	Read	Data out	Icc1, Icc2, Icc3
L	H	x	L	Write	Data in	Icc1, Icc2, Icc3

x: "H" or "L"

DC Recommended Operating Conditions

(Ta = 0 to +70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Input high voltage	V <sub>IH</sub>	2.2	—	Vcc + 0.3	V
Input low voltage	V <sub>IL</sub>	-0.3*	—	0.8	V

\* V<sub>IL</sub> = -3.0V Min. for pulse width less than 50ns.

## Electrical Characteristics

## • DC Characteristics

(V<sub>CC</sub> = 5V ± 10%, GND = 0V, Ta = 0 to +70°C)

Item	Symbol	Test conditions	Min.	Typ.*	Max.	Unit	
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> = GND to V <sub>CC</sub>	-1	—	+1	μA	
Output leakage current	I <sub>LO</sub>	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ V <sub>I/O</sub> = GND to V <sub>CC</sub>	-1	—	+1	μA	
Operating power supply current	I <sub>CC1</sub>	$\overline{CE1} = V_{IL}$ , CE2 = V <sub>IH</sub> V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OUT</sub> = 0mA	—	7	15	mA	
Average operating current	I <sub>CC2</sub>	Min. cycle duty = 100% I <sub>OUT</sub> = 0mA	-55LL	—	45	90	mA
			-70LL	—	40	70	
			-10LL	—	35	60	
Average operating current	I <sub>CC3</sub>	Cycle time 1μs duty = 100% I <sub>OUT</sub> = 0mA $\overline{CE1} \leq 0.2V$ CE2 ≥ V <sub>CC</sub> - 0.2V V <sub>IL</sub> ≤ 0.2V V <sub>IH</sub> ≥ V <sub>CC</sub> - 0.2V	—	10	20	mA	
Standby current	I <sub>SB1</sub>	CE2 = 0.2V or $\overline{CE1} \geq V_{CC} - 0.2V$ or $\overline{OE} \geq V_{CC} - 0.2V$	0 to +70°C	—	—	10	μA
			0 to +40°C	—	—	2	
			+25°C	—	0.4	1	
	I <sub>SB2</sub>	$\overline{CE1} = V_{IH}$ or CE2 = V <sub>IL</sub>	—	0.6	3	mA	
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1.0mA	2.4	—	—	V	
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.1mA	—	—	0.4	V	

\* V<sub>CC</sub> = 5V, Ta = 25°C

**I/O capacitance**

(Ta = 25°C, f = 1MHz)

Item	Symbol	Test conditons	Min.	Typ.	Max.	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0V	—	—	7	pF
I/O capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> = 0V	—	—	8	pF

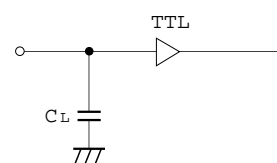
**Note)** This parameter is sampled and is not 100% tested.

**AC Characteristics**

• **AC test conditions** (V<sub>CC</sub> = 5V ± 10%, Ta = 0 to +70°C)

Item	Conditions	
Input pulse high level	V <sub>IH</sub> = 2.2V	
Input pulse low level	V <sub>IL</sub> = 0.8V	
Input rise time	tr = 5ns	
Input fall time	tf = 5ns	
Input and output reference level	1.5V	
Output load conditions	-55LL	C <sub>L</sub> * = 30pF, 1TTL
	-70LL/10LL	C <sub>L</sub> * = 100pF, 1TTL

• Test circuit



\* C<sub>L</sub> includes scope and jig capacitances.

## • Read cycle (WE = "H")

(V<sub>CC</sub> = 5V ± 10%, GND = 0V, T<sub>a</sub> = 0 to +70°C)

Item	Symbol	-55LL		-70LL		-10LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t <sub>RC</sub>	55	—	70	—	100	—	ns
Address access time	t <sub>AA</sub>	—	55	—	70	—	100	ns
Chip enable access time ( $\overline{\text{CE}}1$ )	t <sub>CO1</sub>	—	55	—	70	—	100	ns
Chip enable access time (CE2)	t <sub>CO2</sub>	—	55	—	70	—	100	ns
Output enable to output valid	t <sub>OE</sub>	—	30	—	40	—	50	ns
Output hold from address change	t <sub>OH</sub>	15	—	15	—	15	—	ns
Chip enable to output in low Z ( $\overline{\text{CE}}1$ , CE2)	t <sub>LZ1</sub> , t <sub>LZ2</sub>	10	—	10	—	10	—	ns
Output enable to output in low Z ( $\overline{\text{OE}}$ )	t <sub>OLZ</sub>	5	—	5	—	5	—	ns
Chip disable to output in high Z ( $\overline{\text{CE}}1$ , CE2)	t <sub>HZ1</sub> <sup>*</sup> , t <sub>HZ2</sub> <sup>*</sup>	—	25	—	25	—	35	ns
Output disable to output in high Z ( $\overline{\text{OE}}$ )	t <sub>OHZ</sub> <sup>*</sup>	—	25	—	25	—	35	ns

\* t<sub>HZ1</sub>, t<sub>HZ2</sub> and t<sub>OHZ</sub> are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

## • Write cycle

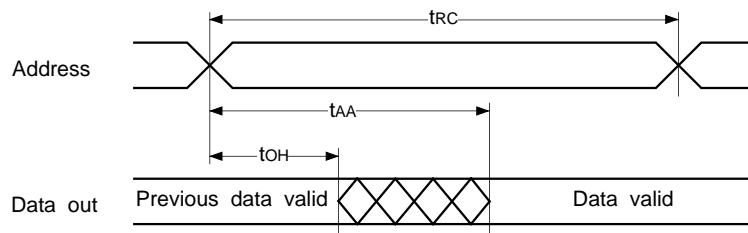
(V<sub>CC</sub> = 5V ± 10%, GND = 0V, T<sub>a</sub> = 0 to +70°C)

Item	Symbol	-55LL		-70LL		-10LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t <sub>WC</sub>	55	—	70	—	100	—	ns
Address valid to end of write	t <sub>AW</sub>	50	—	60	—	70	—	ns
Chip enable to end of write	t <sub>CW</sub>	50	—	60	—	70	—	ns
Data to write time overlap	t <sub>DW</sub>	25	—	30	—	40	—	ns
Data hold from write time	t <sub>DH</sub>	0	—	0	—	0	—	ns
Write pulse width	t <sub>WP</sub>	40	—	50	—	70	—	ns
Address setup time	t <sub>AS</sub>	0	—	0	—	0	—	ns
Write recovery time ( $\overline{\text{WE}}$ )	t <sub>WR</sub>	0	—	0	—	0	—	ns
Write recovery time ( $\overline{\text{CE}}1$ , CE2)	t <sub>WR1</sub>	0	—	0	—	0	—	ns
Output active from end of write	t <sub>OW</sub>	10	—	10	—	10	—	ns
Write to output in high Z	t <sub>WHZ</sub> <sup>*</sup>	—	25	—	25	—	30	ns

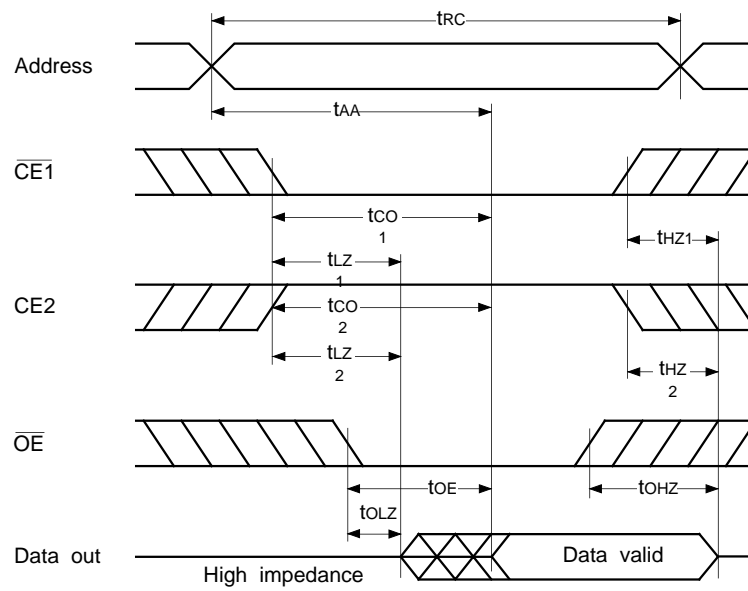
\* t<sub>WHZ</sub> is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

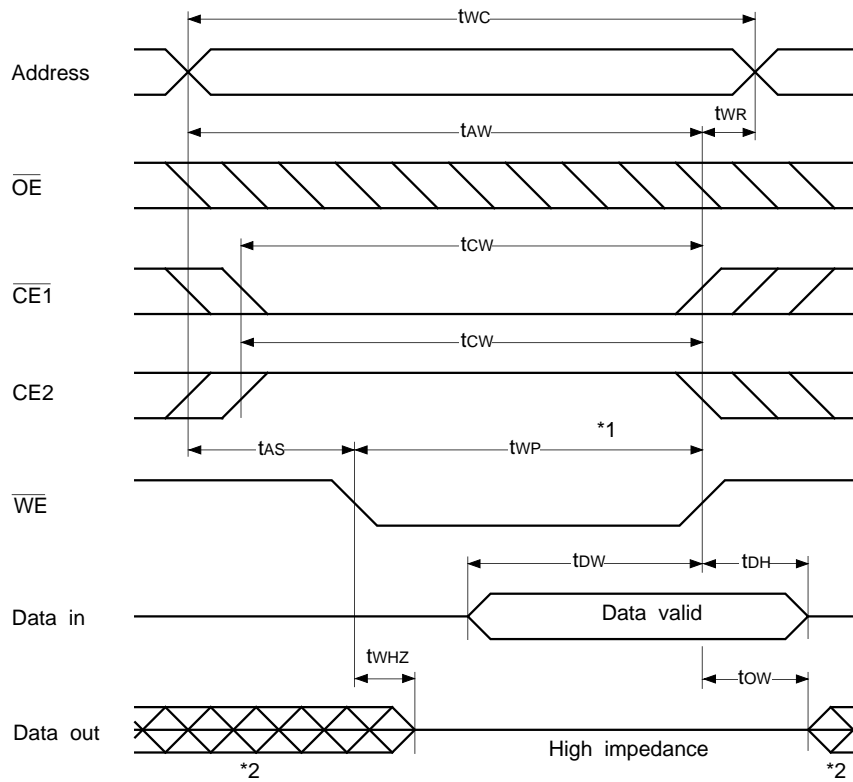
- Read cycle (1) :  $\overline{CE1} = \overline{OE} = V_{IL}$ ,  $CE2 = V_{IH}$ ,  $\overline{WE} = V_{IH}$



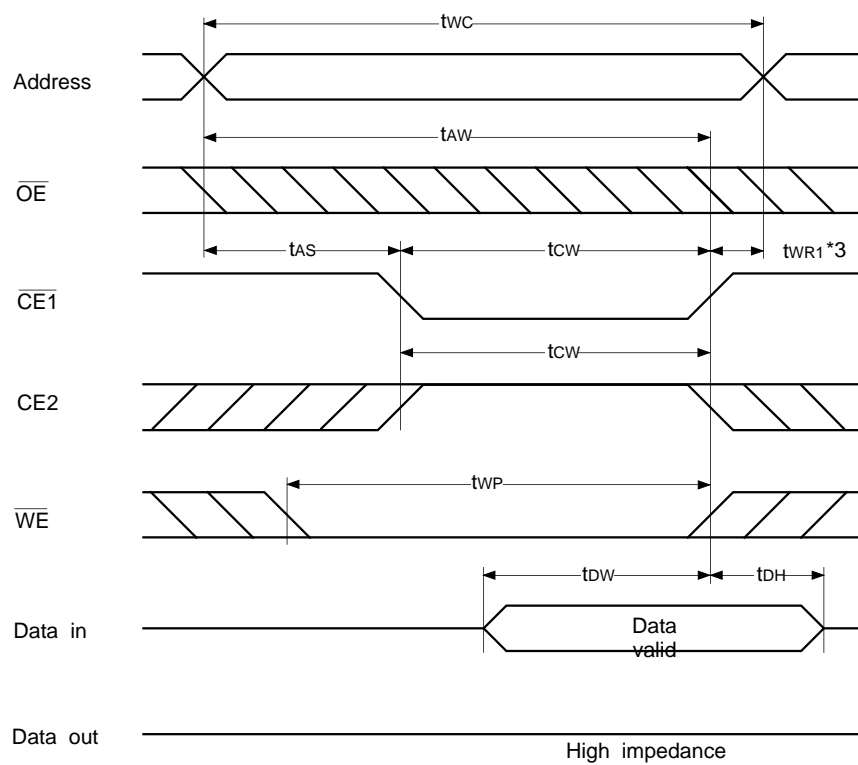
- Read cycle (2) :  $\overline{WE} = V_{IH}$



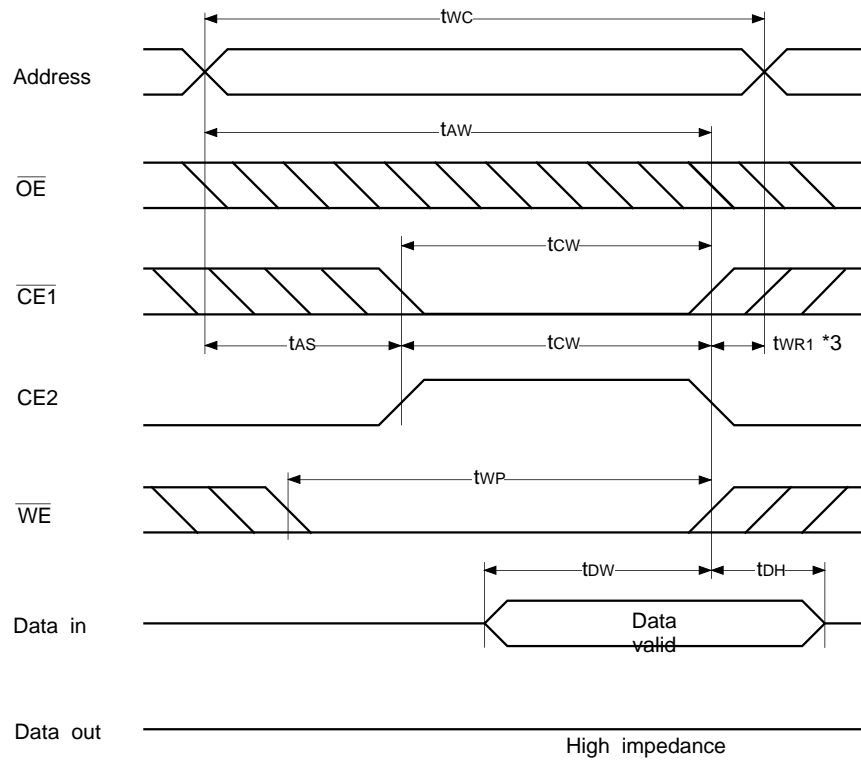
• Write cycle (1) :  $\overline{WE}$  control



• Write cycle (2) :  $\overline{CE1}$  control



• Write cycle (3) : CE2 control



\*1 Write is executed when both  $\overline{CE1}$  and  $\overline{WE}$  are at low and CE2 is at high simultaneously.

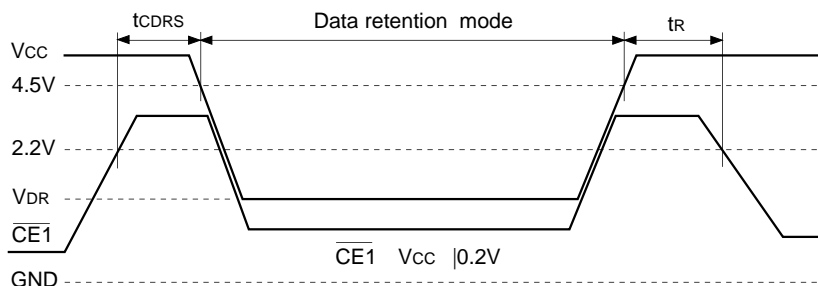
\*2 Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.

\*3  $t_{WR1}$  is tested from either the rising edge of  $\overline{CE1}$  or the falling edge of CE2, whichever comes earlier, until the end of the write cycle.

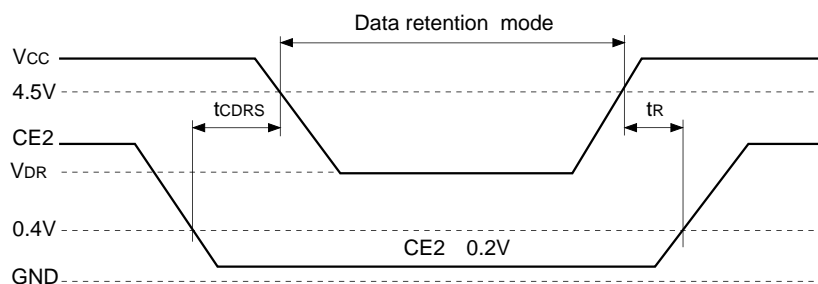


Data retention waveform

• Low supply voltage data retention waveform (1) ( $\overline{CE1}$  control)



• Low supply voltage data retention waveform (2) (CE2 control)



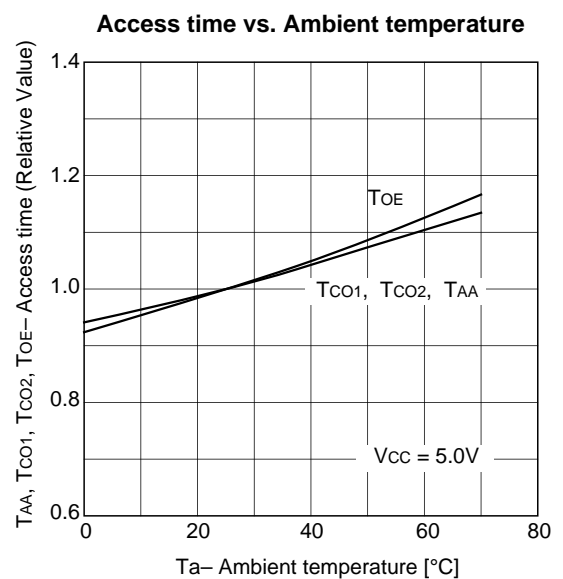
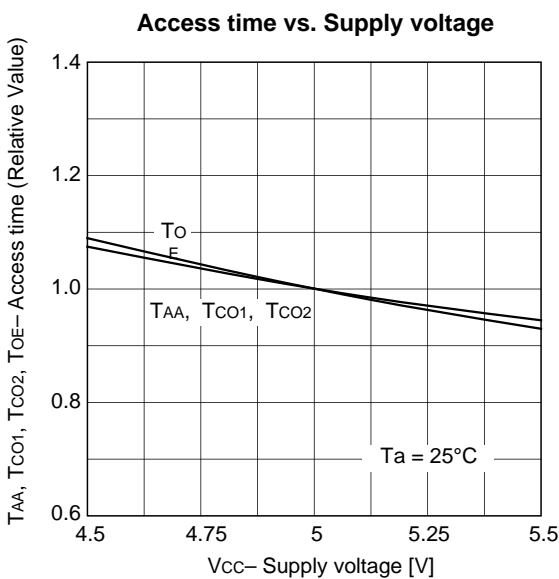
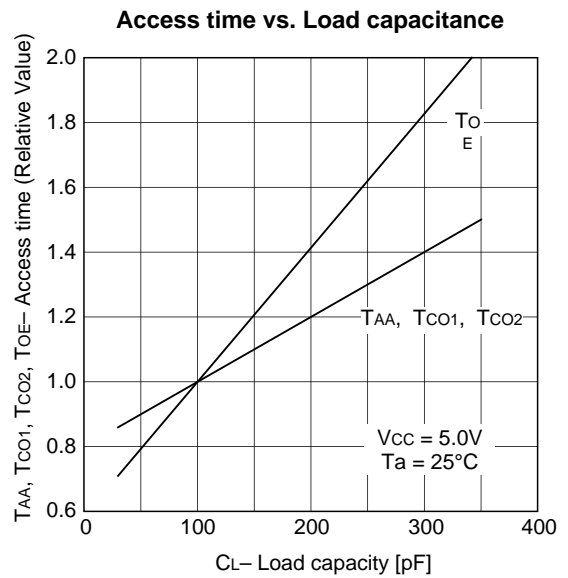
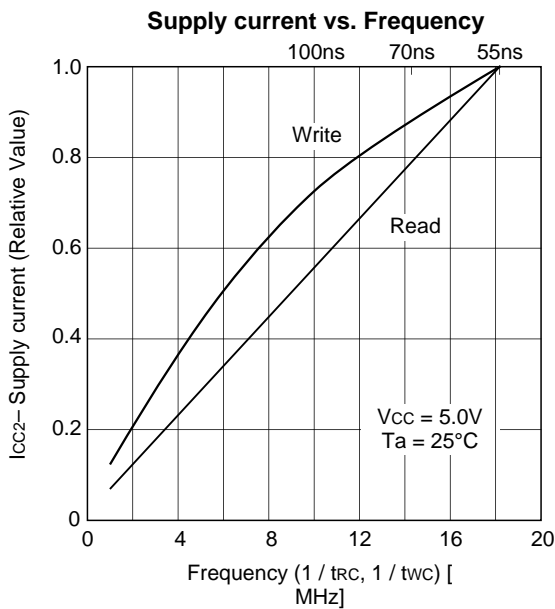
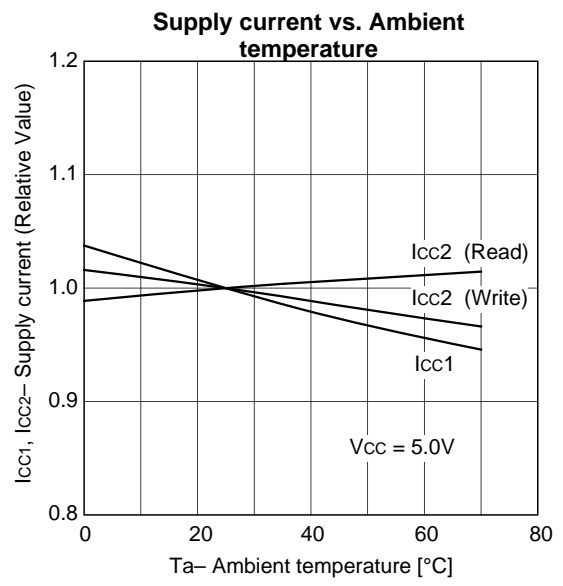
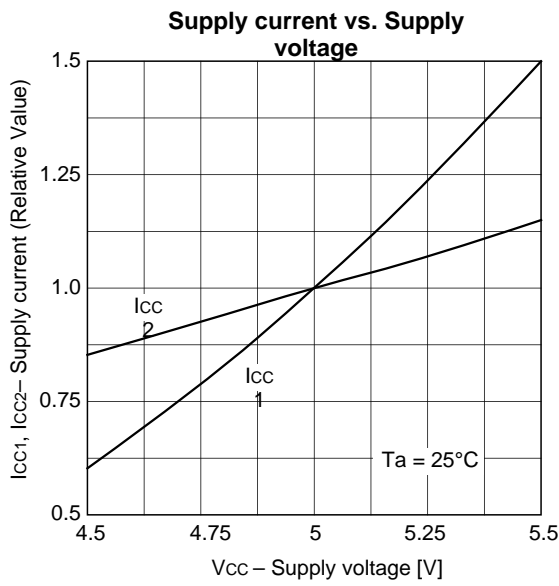
Data Retention Characteristics

(Ta = 0 to +70°C)

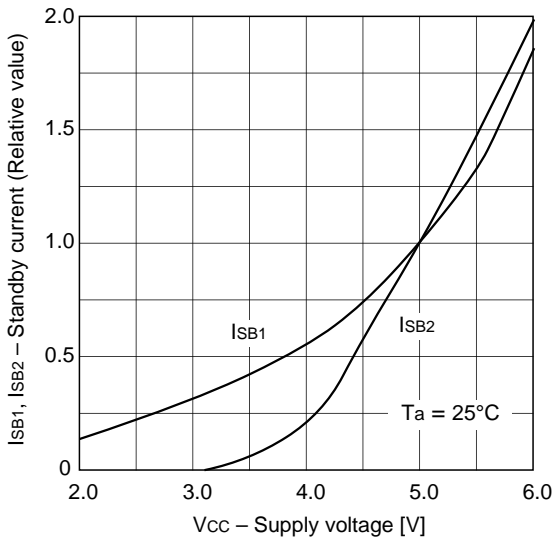
Item	Symbol	Test conditions	Min.	Typ.	Max.	Unit	
Data retention voltage	V <sub>DR</sub>	*	2.0	—	5.5	V	
Data retention current	I <sub>CCDR1</sub>	V <sub>CC</sub> = 3.0V*	0 to +70°C	—	—	6	μA
			0 to +40°C	—	—	1.2	
			+25°C	—	0.2	0.6	
	I <sub>CCDR2</sub>	V <sub>CC</sub> = 2.0 to 5.5V*	—	0.4	10	μA	
Data retention setup time	t <sub>CDRS</sub>	Chip disable to data retention mode	0	—	—	ns	
Recovery time	t <sub>R</sub>		5	—	—	ms	

\*  $\overline{CE1} \geq V_{CC} - 0.2V$ ,  $CE2 \geq V_{CC} - 0.2V$  ( $\overline{CE1}$  control) or  $CE2 \leq 0.2V$  (CE2 control)

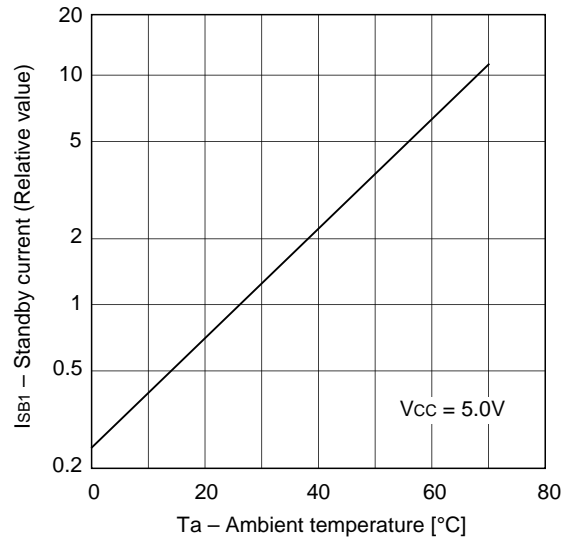
Example of Representative Characteristics



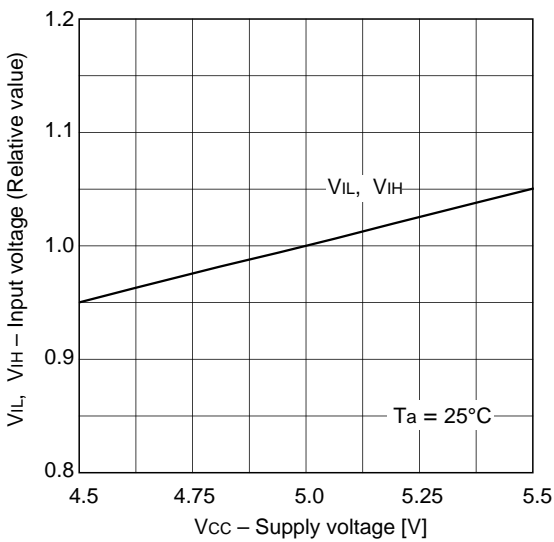
Standby current vs. Supply voltage



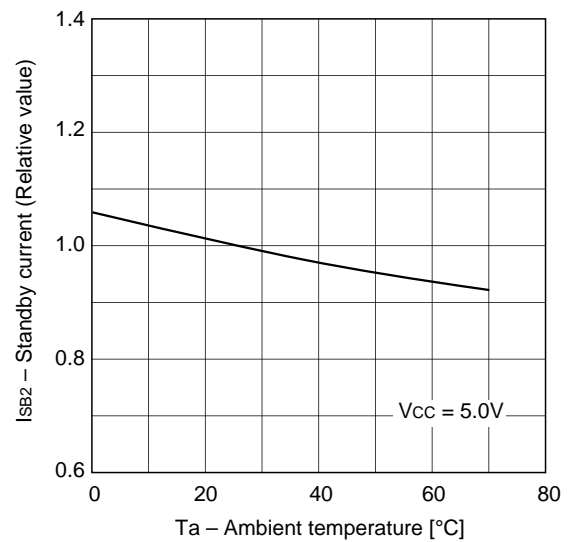
Standby current vs. Ambient temperature



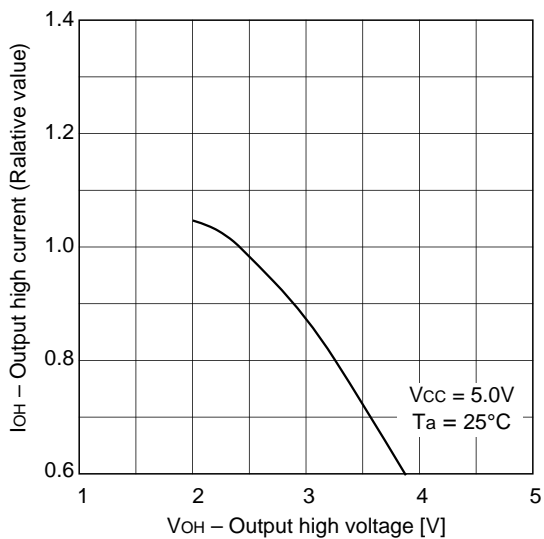
Input voltage level vs. Supply voltage



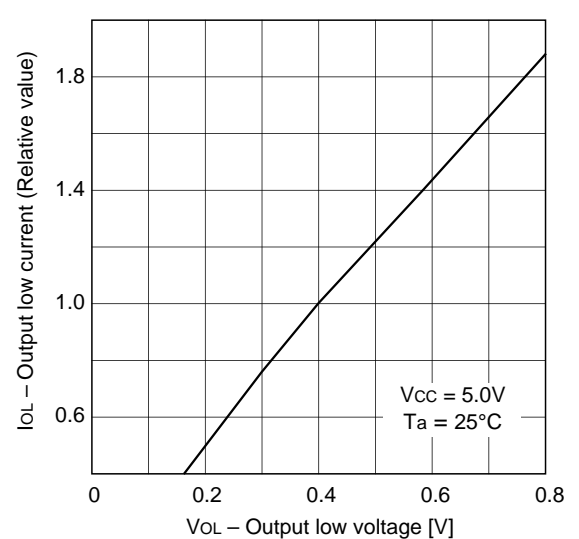
Standby current vs. Ambient temperature



Output high current vs. Output high voltage



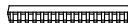
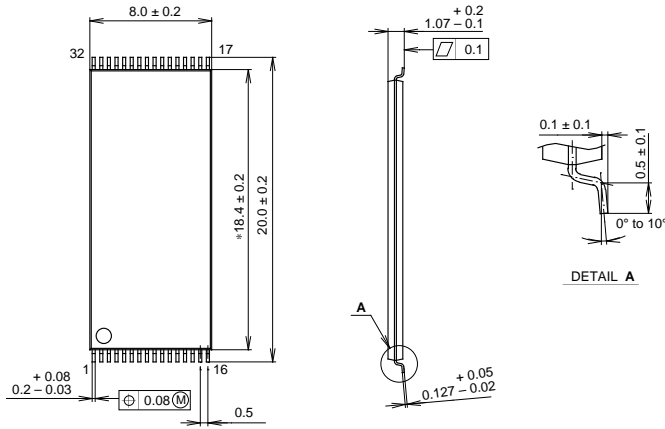
Output low current vs. Output low voltage



Package Outline Unit: mm

CXK58512TM

32PIN TSOP (I) (PLASTIC)



NOTE: Dimension "\*" does not include mold protrusion.

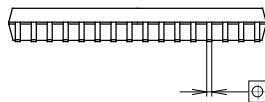
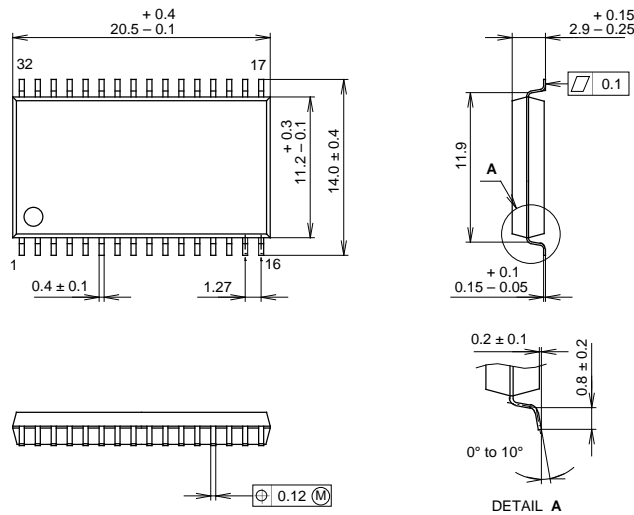
PACKAGE STRUCTURE

SONY CODE	TSOP (I) -32P-L01
EIAJ CODE	TSOP (I) 032-P-0820-A
JEDEC CODE	

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	

CXK58512M

32PIN SOP (PLASTIC) 525mil



PACKAGE STRUCTURE

SONY CODE	SOP-32P-L02
EIAJ CODE	*SOP032-P-0525-A
JEDEC CODE	

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	