

**CXK5T81000ATN/AYN -10LLX/12LLX**

**131072-word × 8-bit High Speed CMOS Static RAM Preliminary**

**Description**

The CXK5T81000ATN/AYN is a high speed CMOS static RAM organized as 131072-words by 8-bits.

Special feature are low power consumption and high speed.

The CXK5T81000ATN/AYN is a suitable RAM for portable equipment with battery back up.

**Features**

- Extended operating temperature range: -25 to +85°C
- Wide supply voltage range operation: 2.7 to 3.6V
- Fast access time: (Access time)
 

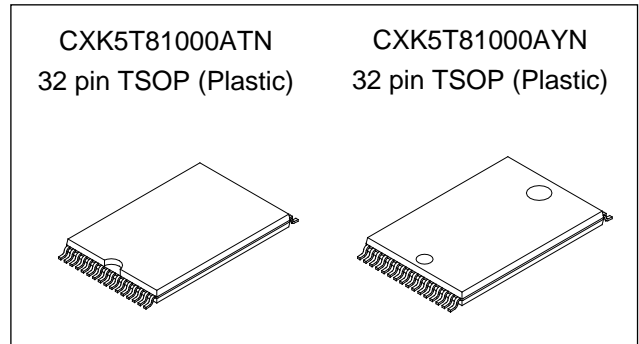
3.0V operation	-10LLX	100ns	(Max.)
	-12LLX	120ns	(Max.)
3.3V operation	-10LLX	85ns	(Max.)
	-12LLX	100ns	(Max.)
- Low standby current: 28µA (Max.)
- Low data retention current: 24µA (Max.)
- Low power data retention: 2.0V (Min.)
- Package 8mm × 13.4mm 32 pin TSOP package

**Function**

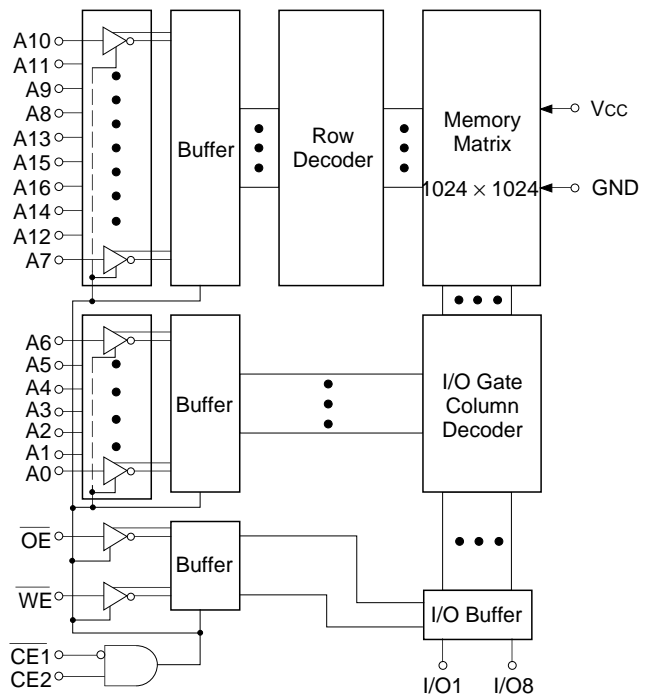
131072-word × 8-bit static RAM

**Structure**

Silicon gate CMOS IC

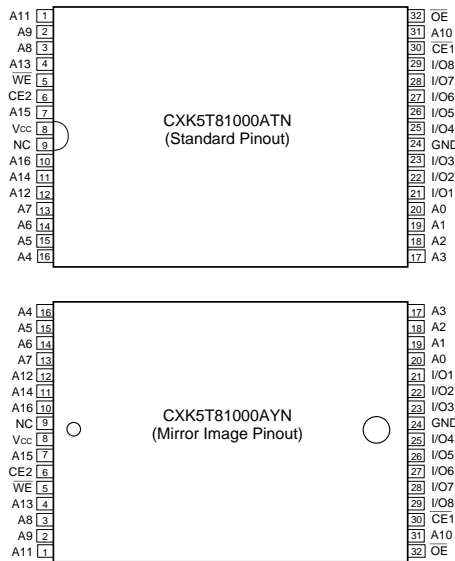


**Block Diagram**



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Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A16	Address input
I/O1 to I/O8	Data input output
$\overline{CE1}$ , $\overline{CE2}$	Chip enable 1, 2 input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
V <sub>CC</sub>	Power supply
GND	Ground
NC	No connection

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V <sub>CC</sub>	-0.5 to +4.6	V
Input voltage	V <sub>IN</sub>	-0.5*1 to V <sub>CC</sub> + 0.5	V
Input and output voltage	V <sub>I/O</sub>	-0.5*1 to V <sub>CC</sub> + 0.5	V
Allowable power dissipation	P <sub>D</sub>	0.7	W
Operating temperature	T <sub>opr</sub>	-25 to +85	°C
Storage temperature	T <sub>stg</sub>	-55 to +150	°C
Soldering temperature · time	T <sub>solder</sub>	235 · 10	°C · s

\*1 V<sub>IN</sub>, V<sub>I/O</sub> = -3.0V Min. for pulse width less than 50ns.

Truth Table

$\overline{CE1}$	$\overline{CE2}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O pin	V <sub>CC</sub> Current
H	×	×	×	Not selected	High Z	I <sub>SB1</sub> , I <sub>SB2</sub>
×	L	×	×	Not selected	High Z	I <sub>SB1</sub> , I <sub>SB2</sub>
L	H	H	H	Output disable	High Z	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC3</sub>
L	H	L	H	Read	Data out	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC3</sub>
L	H	×	L	Write	Data in	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC3</sub>

× : "H" or "L"

DC Recommended Operating Conditions

(Ta = -25 to +85°C, GND = 0V)

Item	Symbol	V <sub>CC</sub> = 2.7 to 3.6V			V <sub>CC</sub> = 3.3V ± 0.3V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply voltage	V <sub>CC</sub>	2.7	3.3	3.6	3.0	3.3	3.6	V
Input high voltage	V <sub>IH</sub>	2.4	—	V <sub>CC</sub> + 0.3	2.2	—	V <sub>CC</sub> + 0.3	
Input low voltage	V <sub>IL</sub>	-0.3*2	—	0.4	-0.3*2	—	0.6	

\*2 V<sub>IL</sub> = -3.0V Min. for pulse width less than 50ns.

**Electrical Characteristics**

**• DC Characteristics**

(V<sub>CC</sub> = 2.7 to 3.6V, GND = 0V, T<sub>a</sub> = -25 to +85°C)

Item	Symbol	Test conditions	Min.	Typ.*1	Max.	Unit	
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> = GND to V <sub>CC</sub>	-1	—	+1	μA	
Output leakage current	I <sub>LO</sub>	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ V <sub>I/O</sub> = GND to V <sub>CC</sub>	-1	—	+1	μA	
Operating power supply current	I <sub>CC1</sub>	$\overline{CE1} = V_{IL}$ , CE2 = V <sub>IH</sub> V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OUT</sub> = 0mA	—	1	3	mA	
Average operating current	I <sub>CC2</sub>	Min. cycle duty = 100% I <sub>OUT</sub> = 0mA	10LLX	—	25*2	35*3	mA
			12LLX	—	25	35	
	I <sub>CC3</sub>	Cycle time 1μs duty = 100% I <sub>OUT</sub> = 0mA CE1 ≤ 0.2V CE2 ≥ V <sub>CC</sub> - 0.2V V <sub>IL</sub> ≤ 0.2V V <sub>IH</sub> ≥ V <sub>CC</sub> - 0.2V	—	5	10	mA	
Standby current	I <sub>SB1</sub>	CE2 ≤ 0.2V or { CE1 ≥ V <sub>CC</sub> - 0.2V CE2 ≥ V <sub>CC</sub> - 0.2V	-25 to +85°C	—	—	28	μA
			-25 to +70°C	—	—	14	
			+25°C	—	0.48	—	
	I <sub>SB2</sub>	$\overline{CE1} = V_{IH}$ or CE2 = V <sub>IL</sub>	—	0.12	1.4	mA	
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = -2.0mA	2.4	—	—	V	
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.0mA	—	—	0.4	V	

\*1 V<sub>CC</sub> = 3.3V, T<sub>a</sub> = 25°C

\*2 I<sub>CC2</sub> = 30mA for 3.3V operation (V<sub>CC</sub> = 3.3V ± 0.3V)

\*3 I<sub>CC2</sub> = 40mA for 3.3V operation (V<sub>CC</sub> = 3.3V ± 0.3V)

**I/O capacitance**

(T<sub>a</sub> = 25°C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0V	—	—	8	pF
I/O capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> = 0V	—	—	10	pF

**Note)** This parameter is sampled and is not 100% tested.

AC Characteristics

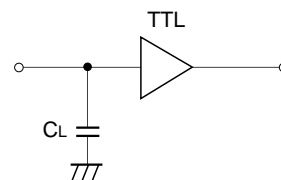
• AC test conditions

(Ta = -25 to +85°C)

Item	Conditions		
	V <sub>CC</sub> = 2.7 to 3.6V	V <sub>CC</sub> = 3.3V ± 0.3V	
Input pulse high level	V <sub>IH</sub> = 2.4V	V <sub>IH</sub> = 2.2V	
Input pulse low level	V <sub>IL</sub> = 0.4V	V <sub>IL</sub> = 0.6V	
Input rise time	t <sub>r</sub> = 5ns	t <sub>r</sub> = 5ns	
Input fall time	t <sub>f</sub> = 5ns	t <sub>f</sub> = 5ns	
Input and output reference level	1.4V	1.4V	
Output load conditions	-10LLX	C <sub>L</sub> *1 = 100pF, 1TTL	C <sub>L</sub> *1 = 30pF, 1TTL
	-12LLX	C <sub>L</sub> *1 = 100pF, 1TTL	C <sub>L</sub> *1 = 100pF, 1TTL

\*1 C<sub>L</sub> includes scope and jig capacitances.

• Test circuit



• Read cycle ( $\overline{WE} = "H"$ )

Item	Symbol	V <sub>CC</sub> = 2.7 to 3.6V				V <sub>CC</sub> = 3.3V ± 0.3V				Unit
		-10LLX		-12LLX		-10LLX		-12LLX		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t <sub>RC</sub>	100	—	120	—	85	—	100	—	ns
Address access time	t <sub>AA</sub>	—	100	—	120	—	85	—	100	ns
Chip enable access time ( $\overline{CE1}$ )	t <sub>CO1</sub>	—	100	—	120	—	85	—	100	ns
Chip enable access time (CE2)	t <sub>CO2</sub>	—	100	—	120	—	85	—	100	ns
Output enable to output valid	t <sub>OE</sub>	—	50	—	60	—	40	—	50	ns
Output hold from address change	t <sub>OH</sub>	10	—	10	—	10	—	10	—	ns
Chip enable to output in low Z ( $\overline{CE1}$ , CE2)	t <sub>LZ1</sub> t <sub>LZ2</sub>	10	—	10	—	10	—	10	—	ns
Output enable to output in low Z ( $\overline{OE}$ )	t <sub>OLZ</sub>	5	—	5	—	5	—	5	—	ns
Chip disable to output in high Z ( $\overline{CE1}$ , CE2)	t <sub>HZ1</sub> *1 t <sub>HZ2</sub> *1	—	40	—	40	—	35	—	40	ns
Output disable to output in high Z ( $\overline{OE}$ )	t <sub>OHZ</sub> *1	—	35	—	35	—	30	—	35	ns

\*1 t<sub>HZ1</sub>, t<sub>HZ2</sub> and t<sub>OHZ</sub> are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

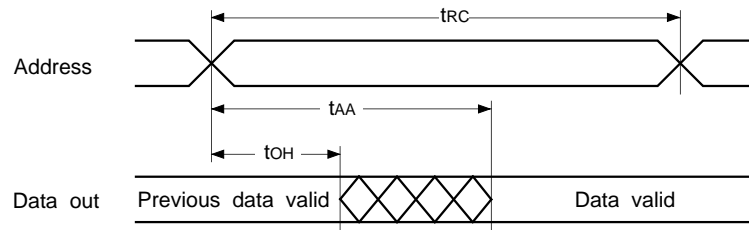
• Write cycle

Item	Symbol	V <sub>CC</sub> = 2.7 to 3.6V				V <sub>CC</sub> = 3.3V ± 0.3V				Unit
		-10LLX		-12LLX		-10LLX		-12LLX		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t <sub>WC</sub>	100	—	120	—	85	—	100	—	ns
Address valid to end of write	t <sub>AW</sub>	80	—	100	—	70	—	80	—	ns
Chip enable to end of write	t <sub>CW</sub>	80	—	100	—	70	—	80	—	ns
Data to write time overlap	t <sub>DW</sub>	40	—	50	—	35	—	40	—	ns
Data hold from write time	t <sub>DH</sub>	0	—	0	—	0	—	0	—	ns
Write pulse width	t <sub>WP</sub>	70	—	70	—	60	—	70	—	ns
Address setup time	t <sub>AS</sub>	0	—	0	—	0	—	0	—	ns
Write recovery time ( $\overline{WE}$ )	t <sub>WR</sub>	0	—	0	—	0	—	0	—	ns
Write recovery time ( $\overline{CE1}$ , CE2)	t <sub>WR1</sub>	0	—	0	—	0	—	0	—	ns
Output active from end of write	t <sub>OW</sub>	5	—	5	—	5	—	5	—	ns
Write to output in high Z	t <sub>WHZ</sub> *2	—	40	—	40	—	35	—	40	ns

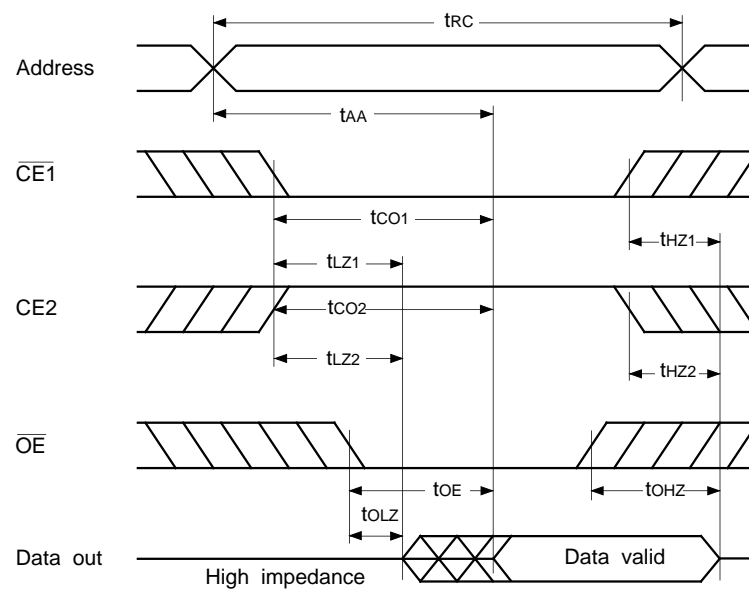
\*2 t<sub>WHZ</sub> is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

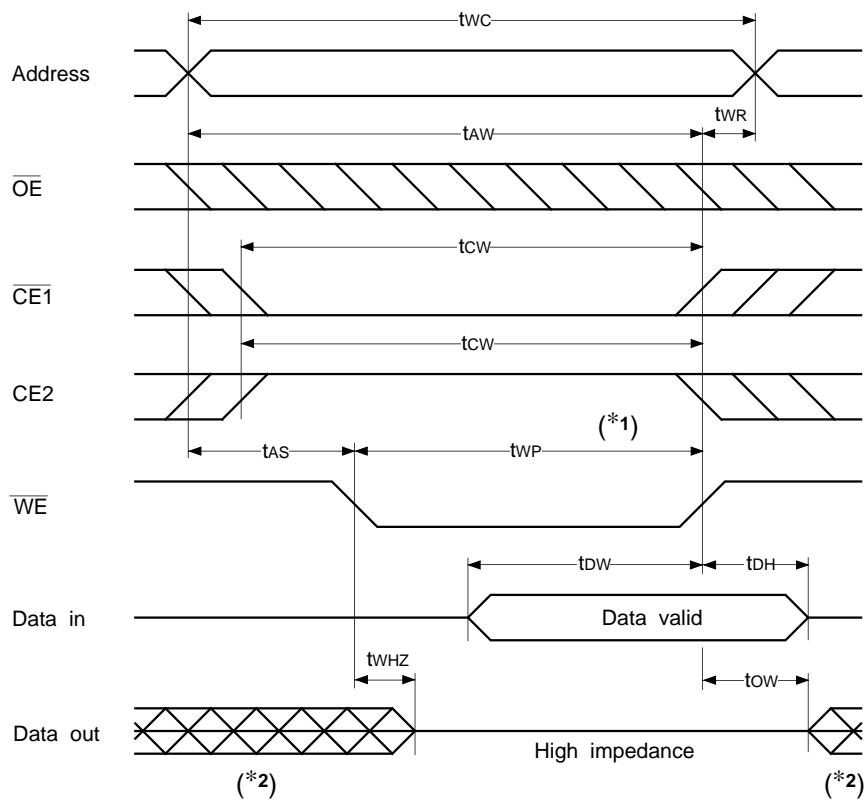
- Read cycle (1) :  $\overline{CE1} = \overline{OE} = V_{IL}$ ,  $CE2 = V_{IH}$ ,  $\overline{WE} = V_{IH}$



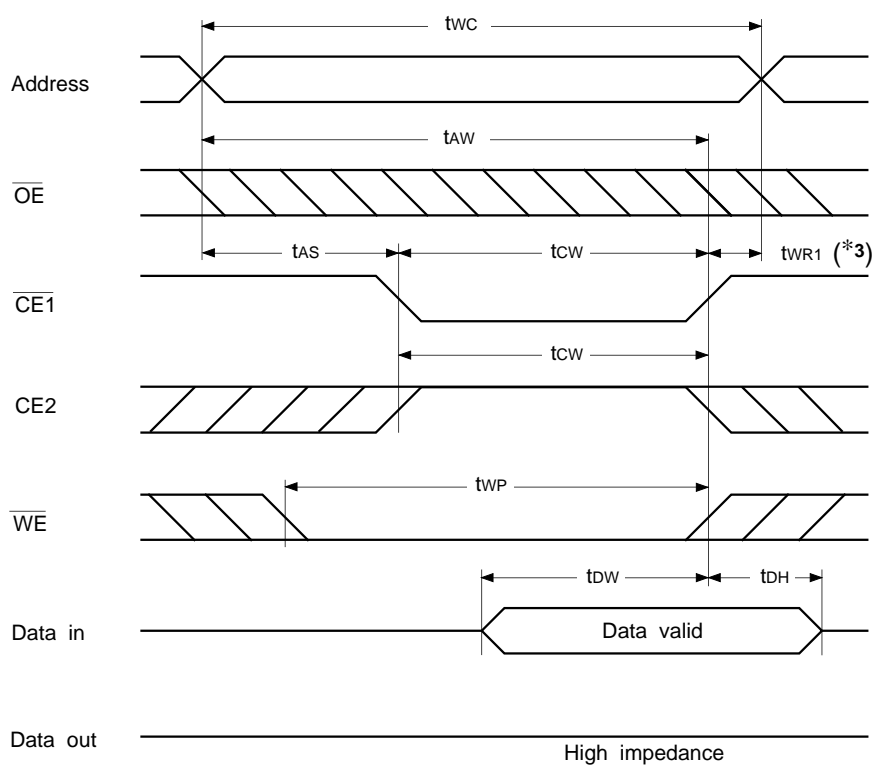
- Read cycle (2) :  $\overline{WE} = V_{IH}$



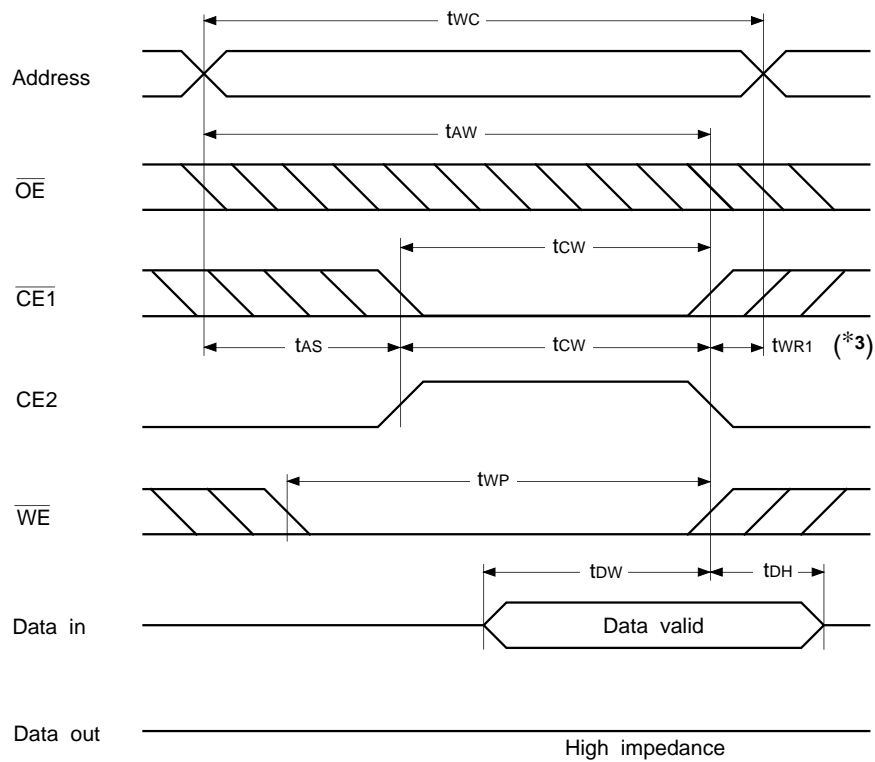
• Write cycle (1) :  $\overline{WE}$  control



• Write cycle (2) :  $\overline{CE1}$  control



• Write cycle (3) : CE2 control



\*1 Write is executed when both  $\overline{CE1}$  and  $\overline{WE}$  are at low and CE2 is at high simultaneously.

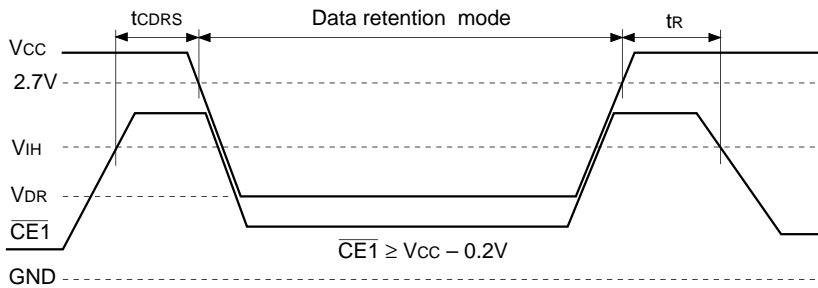
\*2 Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.

\*3  $t_{WR1}$  is tested from either the rising edge of  $\overline{CE1}$  or the falling edge of CE2, whichever comes earlier, until the end of the write cycle.

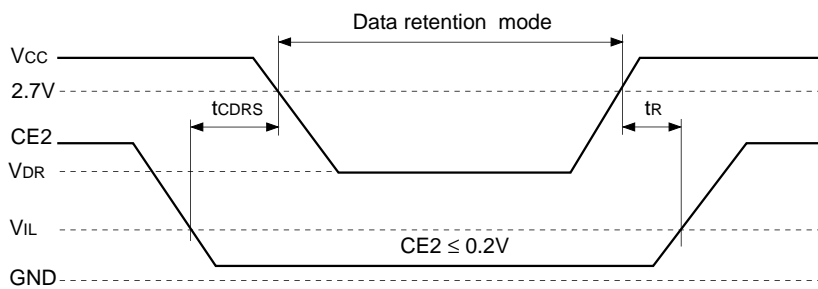


Data retention waveform

• Low supply voltage data retention waveform (1) ( $\overline{CE1}$  control)



• Low supply voltage data retention waveform (2) (CE2 control)



Data Retention Characteristics

(Ta = -25 to +85°C)

Item	Symbol	Test conditions	Min.	Typ.	Max.	Unit	
Data retention voltage	V <sub>DR</sub>	*1	2.0	—	3.6	V	
Data retention current	I <sub>CCDR1</sub>	V <sub>CC</sub> = 3.0V*1	-25 to +85°C	—	—	24	μA
			-25 to +70°C	—	—	12	
			+25°C	—	0.4	—	
	I <sub>CCDR2</sub>	V <sub>CC</sub> = 2.0 to 3.6V*1	—	0.48*2	28	μA	
Data retention setup time	t <sub>CDRS</sub>	Chip disable to data retention mode	0	—	—	ns	
Recovery time	t <sub>R</sub>		5	—	—	ns	

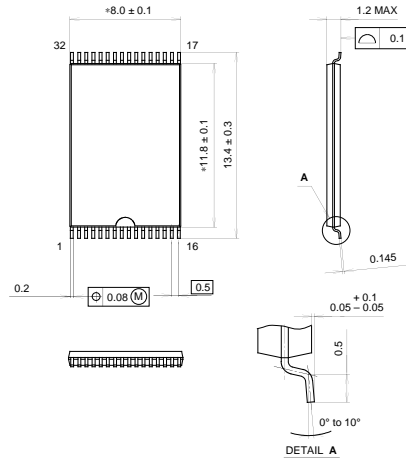
\*1  $\overline{CE1} \geq V_{CC} - 0.2V$ ,  $CE2 \geq V_{CC} - 0.2V$  ( $\overline{CE1}$  control) or  $CE2 \leq 0.2V$  (CE2 control)

\*2 V<sub>CC</sub> = 3.3V, Ta = 25°C

Package Outline Unit: mm

CXK5T81000ATN

32PIN TSOP (PLASTIC)



NOTE: Dimension "\*" does not include mold protrusion.

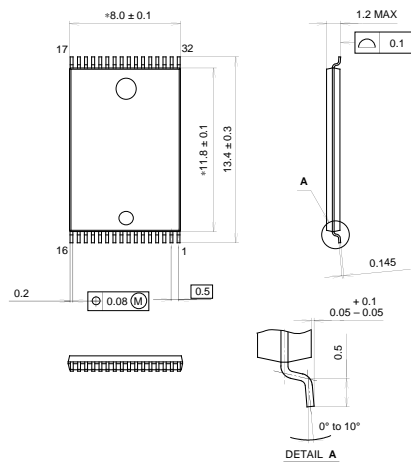
PACKAGE STRUCTURE

SONY CODE	TSOP-32P-L02
EIAJ CODE	TSOP032-P-0813.4-C
JEDEC CODE	---

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.2g

CXK5T81000AYN

32PIN TSOP (PLASTIC)



NOTE: Dimension "\*" does not include mold protrusion.

PACKAGE STRUCTURE

SONY CODE	TSOP-32P-L02R
EIAJ CODE	TSOP032-P-0813.4-D
JEDEC CODE	---

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.2g