

# CXK5V16100TM -85LLX/10LLX

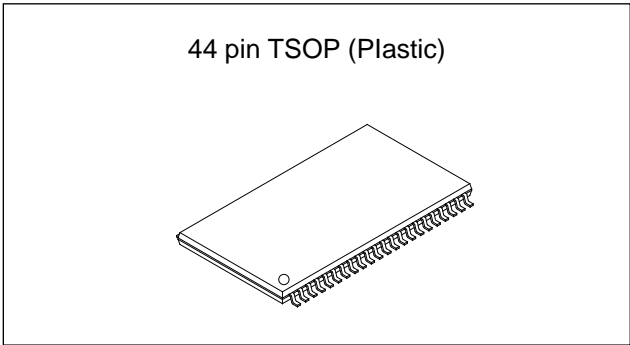
## 65536-word × 16-bit High Speed CMOS Static RAM

**Description**

CXK5V16100TM is a general purpose high speed CMOS static RAM organized as 65536-words by 16-bits. Operating on a single 3.3V supply, this asynchronous IC is suitable for high speed and low power consumption applications where battery back up for nonvolatility is required.

**Features**

- Extended operating temperature range: -25 to +85°C
- Fast access time: (Access time)
  - 85LLX 85ns (max.)
  - 10LLX 100ns (max.)
- Low power consumption operation:
  - Standby / DC operation
  - 1.7μW (typ.) / 3.3mW (typ.)
- Single 3.3V supply: 3.3V±0.3V
- Fully static memory: No clock or timing strobe required
- Equal access and cycle time
- Common data input and output: three state output
- Directly LVTTTL compatible: All inputs and outputs
- Low voltage data retention: 2.0V (min.)
- 400mil 44pin TSOP (type II) package



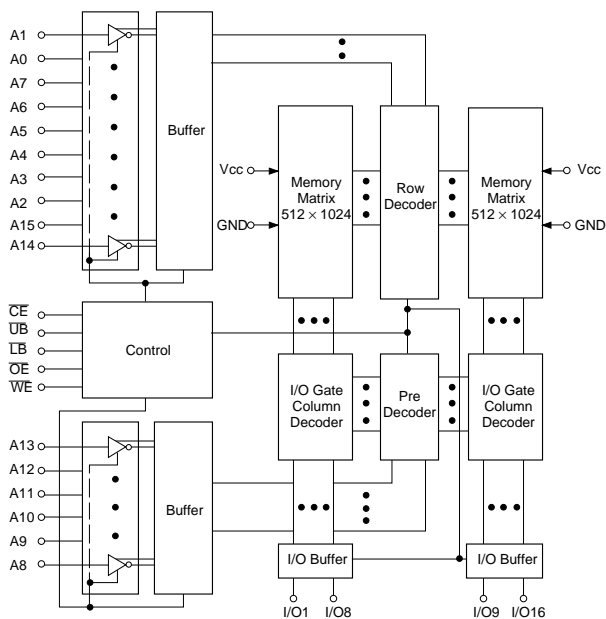
**Function**

65536-word × 16-bit static RAM

**Structure**

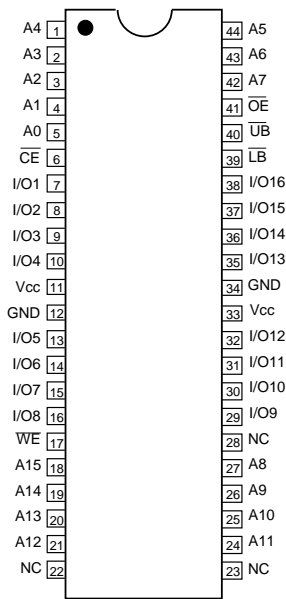
Silicon gate CMOS IC

**Block Diagram**



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Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A15	Address input
I/O1 to I/O16	Data input/output
$\overline{CE}$	Chip enable input
$\overline{LB}$	Byte enable input (I/O1 to I/O8)
$\overline{UB}$	Byte enable input (I/O9 to I/O16)
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	+3.3V power supply
GND	Ground
NC	No connection

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	Vcc	-0.5 to +4.6	V
Input voltage	V <sub>IN</sub>	-0.5* to Vcc + 0.5	V
Input and output voltage	V <sub>I/O</sub>	-0.5* to Vcc + 0.5	V
Allowable power dissipation	P <sub>D</sub>	0.7	W
Operating temperature	T <sub>opr</sub>	-25 to +85	°C
Storage temperature	T <sub>stg</sub>	-55 to +150	°C
Soldering temperature • time	T <sub>solder</sub>	235 • 10	°C • s

\* V<sub>IN</sub>, V<sub>I/O</sub> = -3.0V Min. for pulse width less than 50ns.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O1 to I/O8	I/O9 to I/O16	Vcc Current
H	×	×	×	×	Not selected	Not selected	I <sub>SB1</sub> , I <sub>SB2</sub>
L	L	H	L	L	Read	Read	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC3</sub>
			L	H	Read	High-Z	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC3</sub>
			H	L	High-Z	Read	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC3</sub>
L	×	L	L	L	Write	Write	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC3</sub>
			L	H	Write	Not Write/Hi-Z	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC3</sub>
			H	L	Not Write/Hi-Z	Write	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC3</sub>
L	H	H	×	×	High-Z	High-Z	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC3</sub>
L	×	×	H	H	High-Z	High-Z	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC3</sub>

×: "H" or "L"

**DC Recommended Operating Conditions** ( $T_a = -25$  to  $+85^\circ\text{C}$ ,  $\text{GND} = 0\text{V}$ )

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	$V_{CC}$	3.0	3.3	3.6	V
Input high voltage	$V_{IH}$	2.0	—	$V_{CC} + 0.3$	V
Input low voltage	$V_{IL}$	-0.3*	—	0.8	V

\*  $V_{IL} = -3.0\text{V}$  Min. for pulse width less than 50ns.

**Electrical Characteristics****DC and operating characteristics**( $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$ ,  $\text{GND} = 0\text{V}$ ,  $T_a = -25$  to  $+85^\circ\text{C}$ )

Item	Symbol	Test condition	Min.	Typ.*	Max.	Unit	
Input leakage current	$I_{LI}$	$V_{IN} = \text{GND to } V_{CC}$	-1	—	1	$\mu\text{A}$	
Output leakage current	$I_{LO}$	$\overline{CE} = V_{IH}$ or $\overline{UB} = V_{IH}$ or $\overline{LB} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ $V_{IO} = \text{GND to } V_{CC}$	-1	—	1	$\mu\text{A}$	
Operating power supply current	$I_{CC1}$	$\overline{CE} = V_{IL}$ $V_{IN} = V_{IH}$ or $V_{IL}$ $I_{OUT} = 0\text{mA}$	—	1	3	mA	
Average operating current	$I_{CC2}$	Min. cycle Duty = 100% $I_{OUT} = 0\text{mA}$	85LLX	—	40	55	mA
			10LLX	—	35	50	
	$I_{CC3}$	Cycle time 1 $\mu\text{s}$ Duty = 100% $I_{OUT} = 0\text{mA}$ $\overline{CE} \leq 0.2\text{V}$ $V_{IL} \leq 0.2\text{V}$ $V_{IH} \geq V_{CC} - 0.2\text{V}$	—	10	20	mA	
Standby current	$I_{SB1}$	$\overline{CE} \geq V_{CC} - 0.2\text{V}$	-25 to +85 $^\circ\text{C}$	—	—	40	$\mu\text{A}$
			-25 to +70 $^\circ\text{C}$	—	—	20	
			-25 to +40 $^\circ\text{C}$	—	—	4	
			+25 $^\circ\text{C}$	—	0.5	2	
	$I_{SB2}$	$\overline{CE} = V_{IH}$	—	0.03	0.6	mA	
Output high voltage	$V_{OH}$	$I_{OH} = -2.0\text{mA}$	2.4	—	—	V	
Output low voltage	$V_{OL}$	$I_{OL} = 2.0\text{mA}$	—	—	0.4	V	

\*  $V_{CC} = 3.3\text{V}$ ,  $T_a = 25^\circ\text{C}$

**I/O capacitance**

(Ta = 25°C, f = 1MHz)

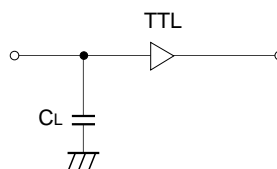
Item	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0V	—	—	8	pF
I/O capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> = 0V	—	—	10	pF

**Note)** This parameter is sampled and is not 100% tested.

**AC Characteristics**

• **AC test conditions** (V<sub>CC</sub> = 3.3V ± 0.3V, Ta = -25 to +85°C)

Item	Conditions	
Input pulse high level	V <sub>IH</sub> = 2.2V	
Input pulse low level	V <sub>IL</sub> = 0.6V	
Input rise time	tr = 5ns	
Input fall time	tf = 5ns	
Input and output reference level	1.4V	
Output load conditions	85ns	C <sub>L</sub> * = 30pF, 1TTL
	100ns	C <sub>L</sub> * = 100pF, 1TTL



\* C<sub>L</sub> includes scope and jig capacitances.

• Read cycle ( $\overline{WE} = "H"$ )

Item	Symbol	-85LLX		-10LLX		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t <sub>RC</sub>	85	—	100	—	ns
Address access time	t <sub>AA</sub>	—	85	—	100	ns
Chip enable access time ( $\overline{CE}$ )	t <sub>CO</sub>	—	85	—	100	ns
Byte enable access time ( $\overline{UB}, \overline{LB}$ )	t <sub>BO</sub>	—	40	—	50	ns
Output enable to output valid	t <sub>OE</sub>	—	40	—	50	ns
Output hold from address change	t <sub>OH</sub>	10	—	10	—	ns
Chip enable to output in low Z ( $\overline{CE}$ )	t <sub>LZ</sub>	10	—	10	—	ns
Output enable to output in low Z ( $\overline{OE}$ )	t <sub>OLZ</sub>	5	—	5	—	ns
Byte enable to output in low Z ( $\overline{UB}, \overline{LB}$ )	t <sub>BLZ</sub>	5	—	5	—	ns
Chip disable to output in high Z ( $\overline{CE}$ )	t <sub>HZ</sub> *	—	35	—	40	ns
Chip disable to output in high Z ( $\overline{OE}$ )	t <sub>OHZ</sub> *	—	30	—	35	ns
Byte disable to output in high Z ( $\overline{UB}, \overline{LB}$ )	t <sub>BHZ</sub> *	—	30	—	35	ns

\* t<sub>HZ</sub>, t<sub>OHZ</sub> and t<sub>BHZ</sub> are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

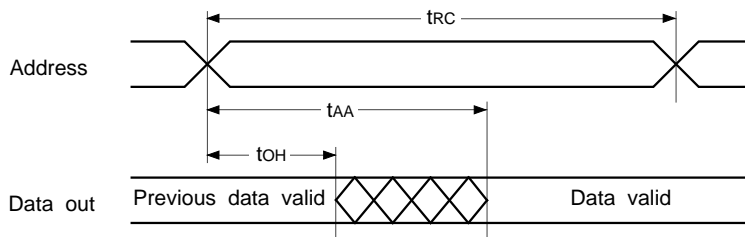
• Write cycle

Item	Symbol	-85LLX		-10LLX		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t <sub>WC</sub>	85	—	100	—	ns
Address valid to end of write	t <sub>AW</sub>	70	—	80	—	ns
Chip enable to end of write	t <sub>CW</sub>	70	—	80	—	ns
Byte enable to end of write	t <sub>BW</sub>	70	—	80	—	ns
Data to write time overlap	t <sub>DW</sub>	35	—	40	—	ns
Data hold from write time	t <sub>DH</sub>	0	—	0	—	ns
Write pulse width	t <sub>WP</sub>	60	—	70	—	ns
Address setup time	t <sub>AS</sub>	0	—	0	—	ns
Write recovery time ( $\overline{WE}$ )	t <sub>WR</sub>	5	—	5	—	ns
Write recovery time ( $\overline{CE}, \overline{UB}, \overline{LB}$ )	t <sub>WR1</sub>	5	—	5	—	ns
Output active from end of write	t <sub>OW</sub>	5	—	5	—	ns
Write to output in high Z	t <sub>WHZ</sub> *	—	35	—	40	ns

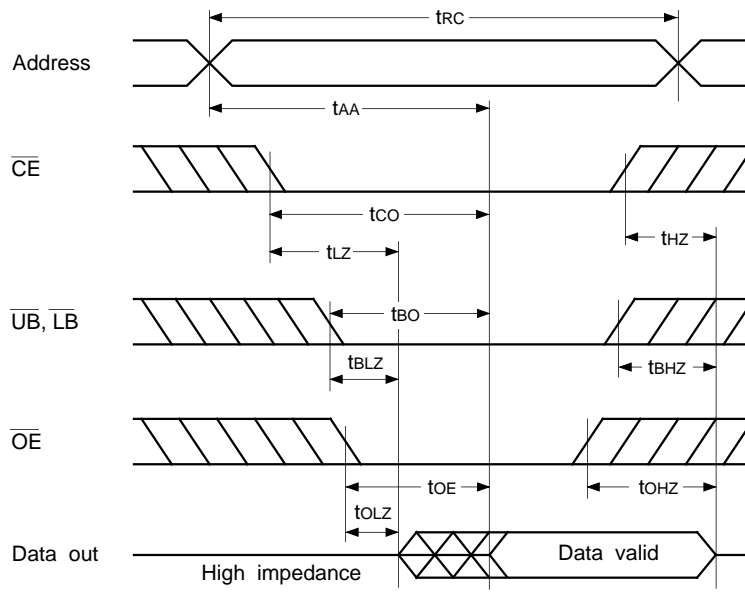
\* t<sub>WHZ</sub> is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage levels.

Timing Waveform

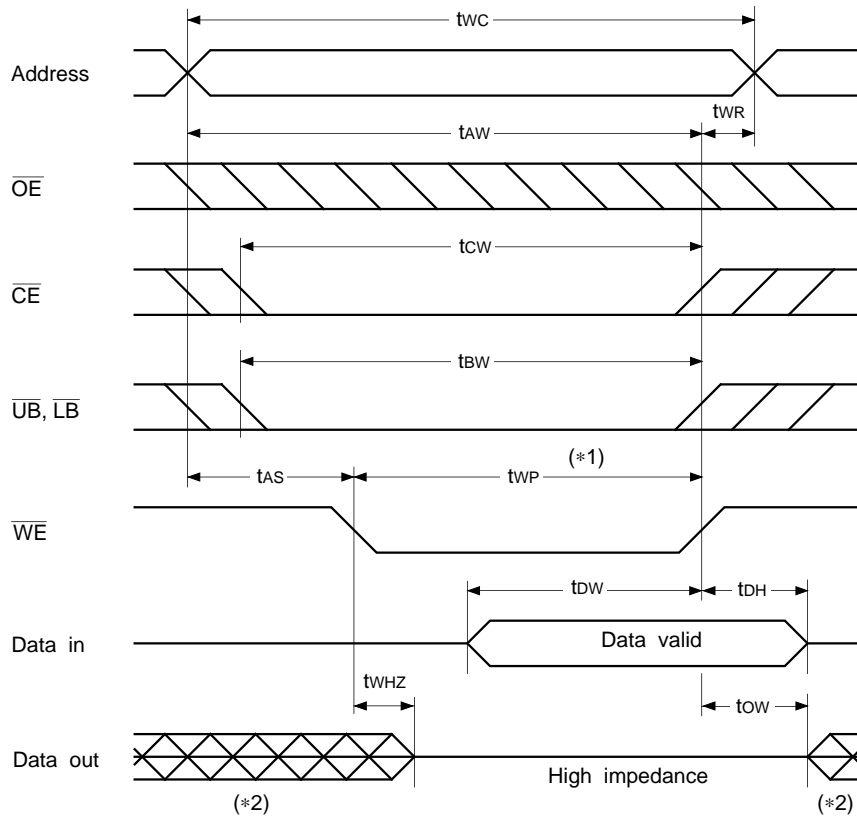
- Read cycle (1) :  $\overline{CE} = \overline{OE} = V_{IL}$ ,  $\overline{WE} = V_{IH}$ ,  $\overline{UB}$  and, or  $\overline{LB} = V_{IL}$



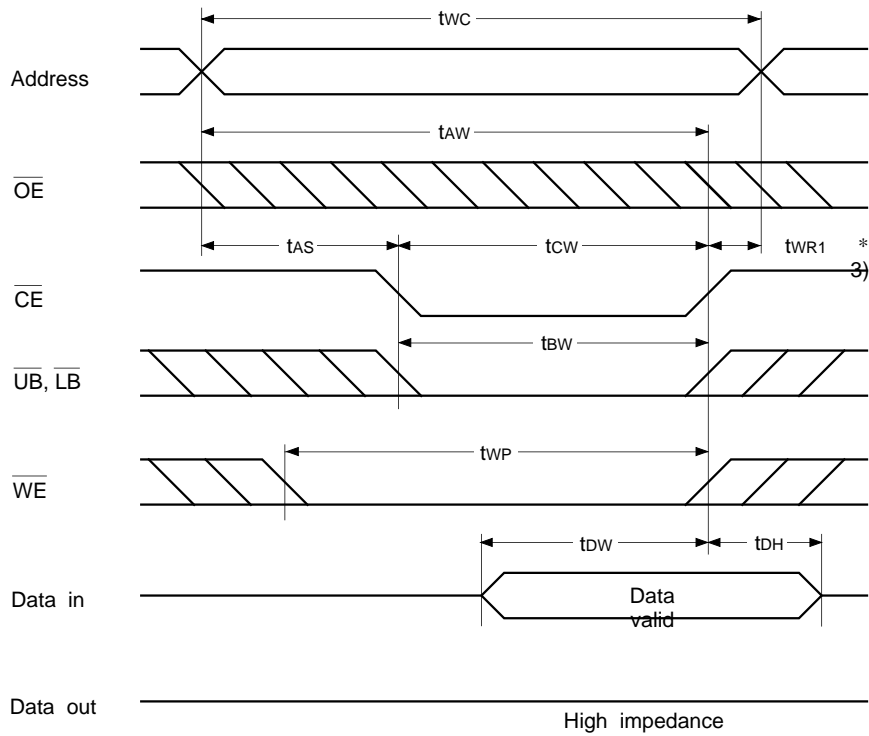
- Read cycle (2) :  $\overline{WE} = V_{IH}$



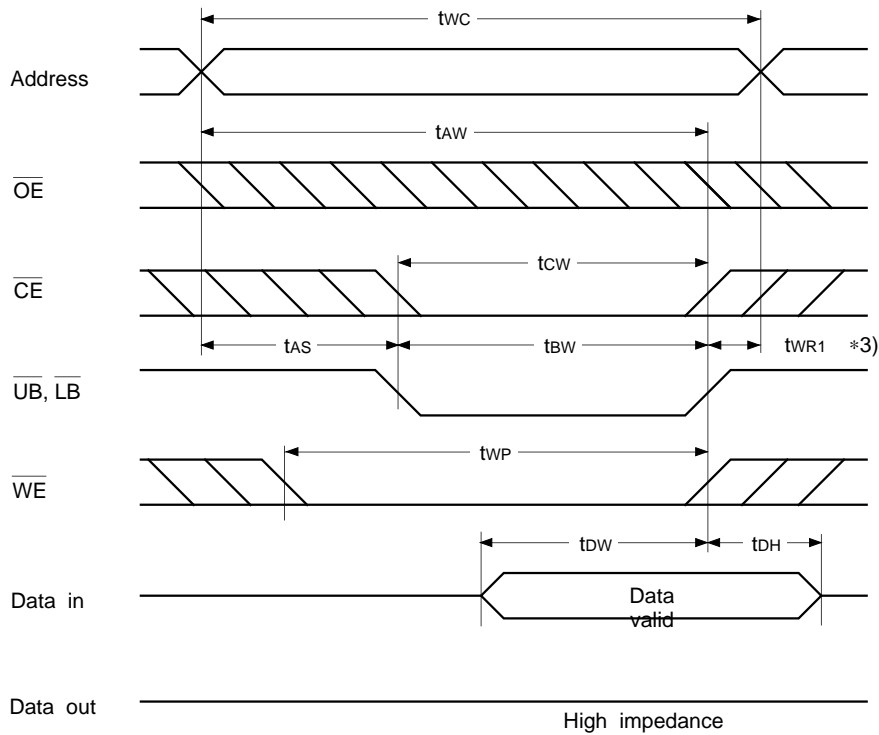
• Write cycle (1) :  $\overline{WE}$  control



• Write cycle (2) :  $\overline{CE}$  control



• Write cycle (3) :  $\overline{UB}$ ,  $\overline{LB}$  control



\*1 Write is executed when all of the  $\overline{CE}$ ,  $\overline{WE}$  and ( $\overline{UB}$  and, or  $\overline{LB}$ ) are at low simultaneously.

\*2 Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.

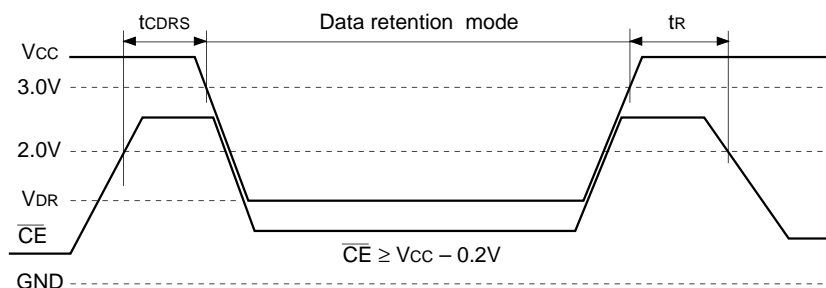
\*3  $t_{WR1}$  (for I/O1 to 8) is tested from either the rising edge of  $\overline{CE}$  or  $\overline{LB}$ , whichever comes earlier, until the end of the write cycle.

$t_{WR1}$  (for I/O9 to 16) is tested from either the rising edge of  $\overline{CE}$  or  $\overline{UB}$ , whichever comes earlier, until the end of the write cycle.



**Data Retention Waveform**

- Low supply voltage data retention waveform



**Data Retention Characteristics**

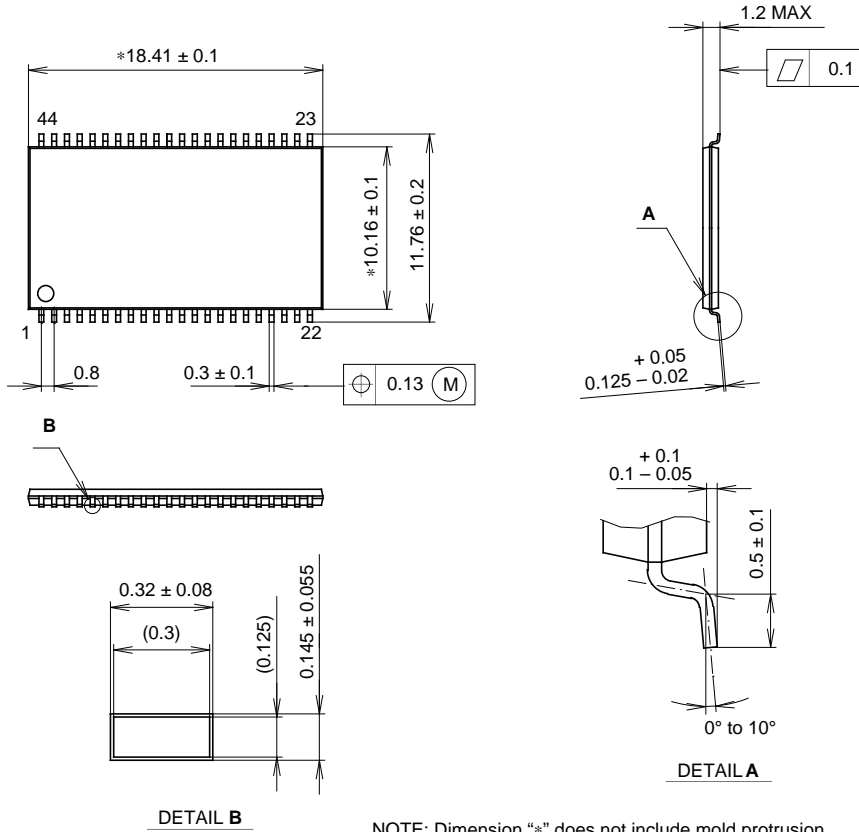
( $T_a = -25$  to  $+85^\circ\text{C}$ )

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit	
Data retention voltage	$V_{DR}$	$\overline{CE} \geq V_{CC} - 0.2V$	2.0	—	3.6	V	
Data retention current	$I_{CCDR1}$	$V_{CC} = 3.0V$	$-25$ to $+85^\circ\text{C}$	—	—	24	$\mu\text{A}$
			$-25$ to $+70^\circ\text{C}$	—	—	12	
			$-25$ to $+40^\circ\text{C}$	—	—	2.4	
			$+25^\circ\text{C}$	—	0.4	1.2	
	$I_{CCDR2}$	$V_{CC} = 2.0$ to $3.6V$	—	0.5*	40	$\mu\text{A}$	
Data retention setup time	$t_{CDRS}$	Chip disable to data retention mode	0	—	—	ns	
Recovery time	$t_R$		5	—	—	ms	

\*  $V_{CC} = 3.3V$ ,  $T_a = 25^\circ\text{C}$

Package Outline Unit: mm

44PIN TSOP (II) (PLASTIC) 400mil



NOTE: Dimension "\*" does not include mold protrusion.

PACKAGE STRUCTURE

SONY CODE	TSOP (II) -44P-L01
EIAJ CODE	TSOP (II) 044-P-0400-A
JEDEC CODE	_____

MOLDING COMPOUND	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.5g