

CMOS 8-bit Single Chip Microcomputer**Piggyback/
evaluator type****Description**

The CXP81800 is a CMOS 8-bit single chip micro-computer of piggyback/evaluator combined type, which is developed for evaluating the function of the CXP81840A/81848A.

Features

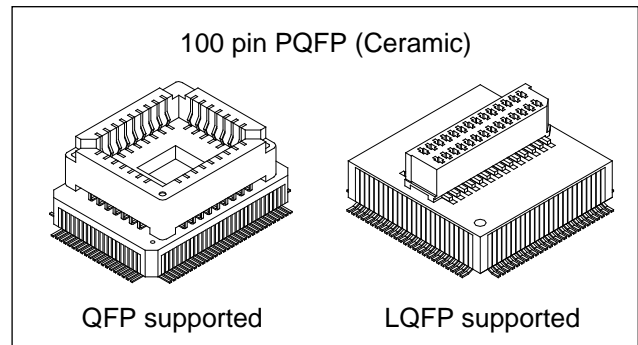
- A wide instruction set (213 instructions) which cover various types of data
 - 16-bit operation/multiplication and division/
boolean bit operation instructions
- Minimum instruction cycle
 - 333ns at 12MHz operation (3.0 to 5.5V)
 - 250ns at 16MHz operation (4.5 to 5.5V)
 - 122μs at 32kHz operation
- Applicable EPROM
 - LCC type 27C256, LCC type 27C512
(Maximum 48Kbytes are available)
- Incorporated RAM capacity
 - 1344bytes
- Peripheral functions
 - A/D converter
 - 8-bit, 12-channel, successive approximation method
(Conversion time of 20μs/16MHz)
 - Serial interface
 - Incorporated 8-bit, 8-stage FIFO
(auto transfer for 1 to 8bytes), 1-channel
 - 8-bit clock synchronous 1-channel
 - Timer
 - 8-bit timer
 - 8-bit timer/counter
 - 19-bit time base timer
 - 32kHz timer/counter
 - High precision timing pattern generator
 - PPG 19-pin, 32-stage programmable
 - RTG 5-pin, 2-channel
 - PWM/DA gate output
 - PWM output 12-bit, 2-channel
(repetitive frequency 62.5kHz/16MHz)
 - DA gate pulse output 12-bit, 4-channel
 - FRC capture unit
 - PWM output
 - Remote control receiving circuit
- Interruption
 - 21 factors, 15 vectors, multi-interruption possible
- Standby mode
 - SLEEP/STOP
- Package
 - 100-pin ceramic PQFP

Note) Mask option depends on the type of the CXP81800. Refer to the Products List for details.

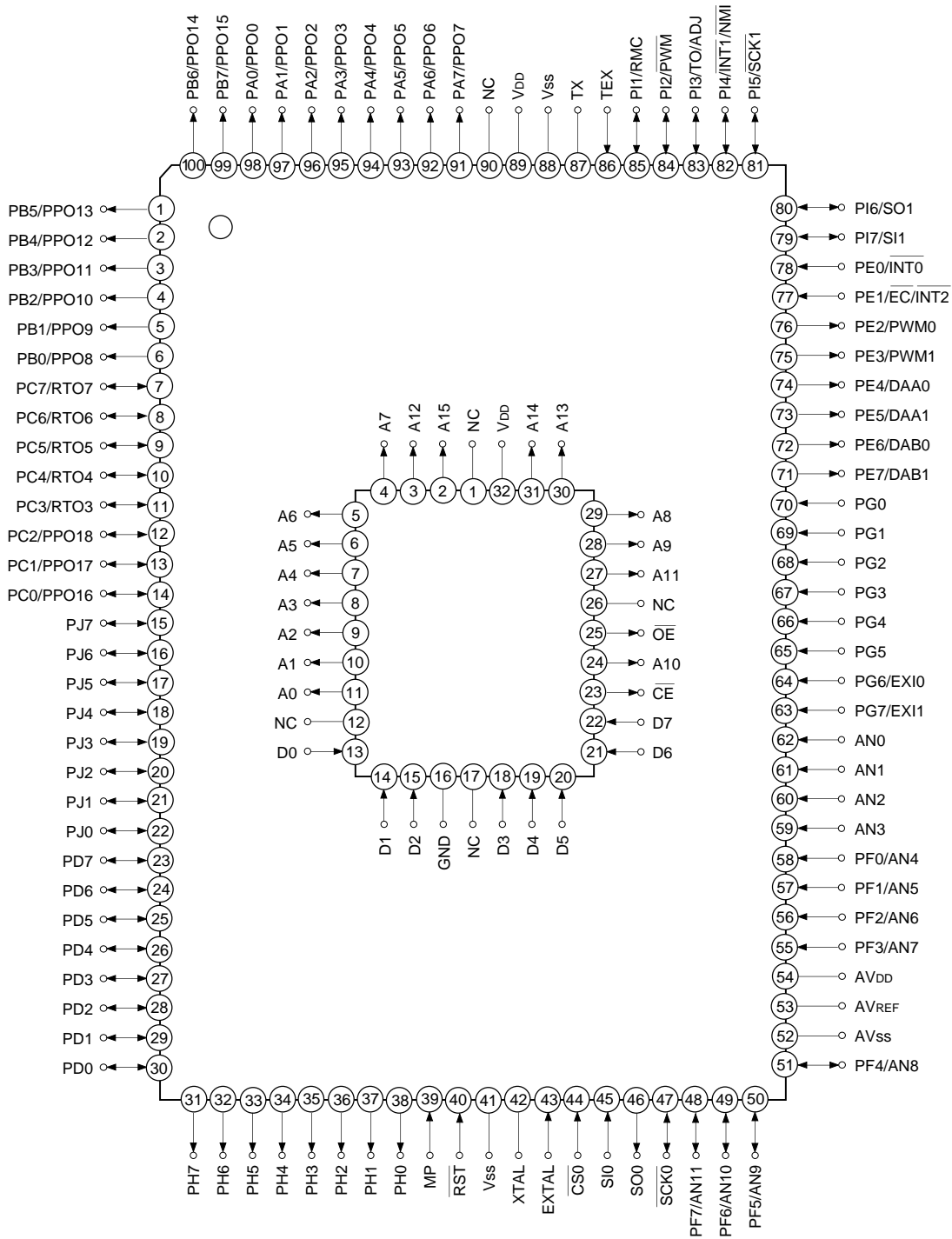
Structure

Silicon gate CMOS IC

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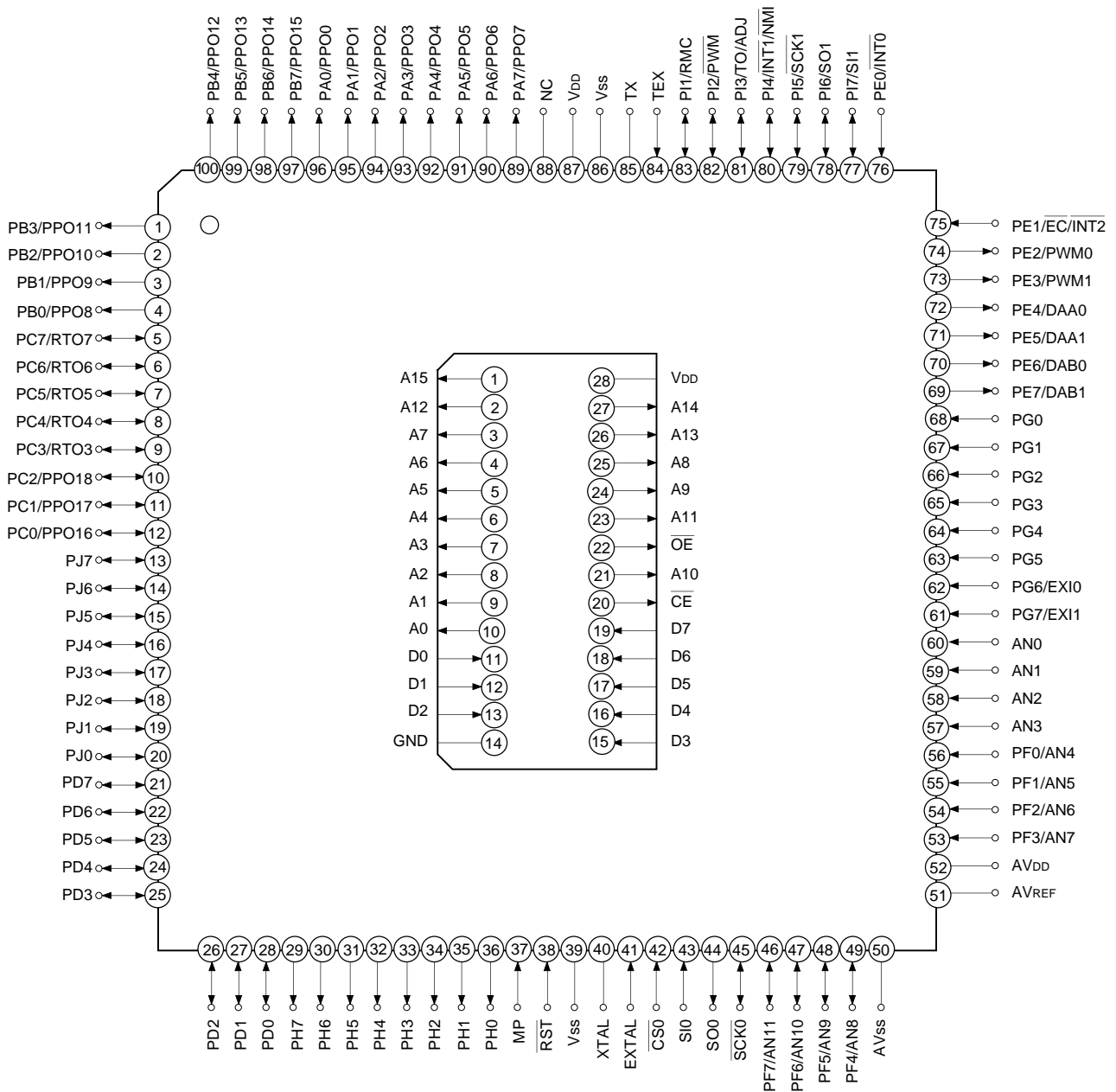


Pin Configuration in Piggyback Mode (QFP package)



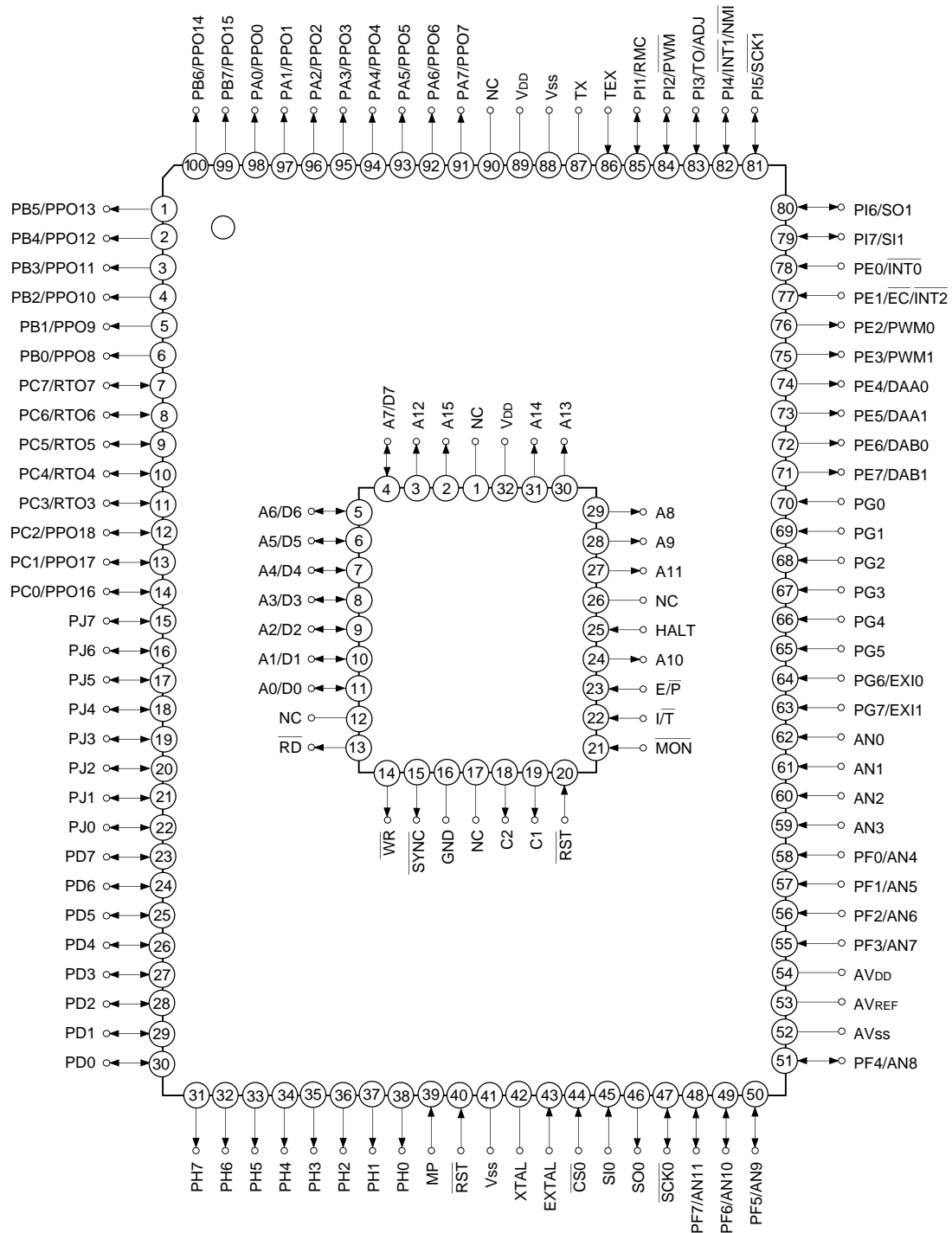
Note) 1. NC (Pin 90) is always connected to VDD.
 2. VSS (Pins 41 and 88) are both connected to GND.
 3. MP (Pin 39) is always connected to GND.

Pin Configuration in Piggyback Mode (LQFP package)



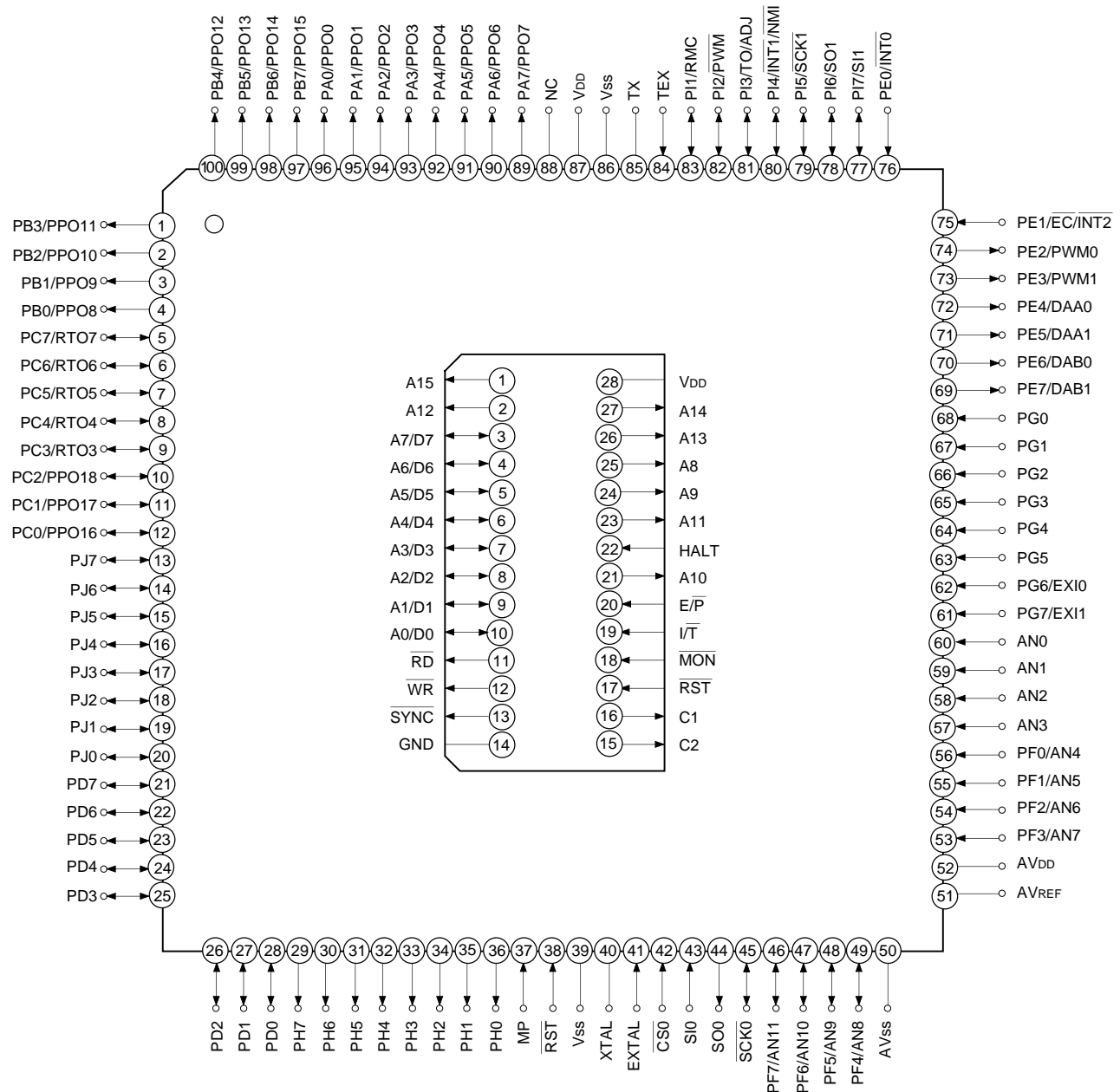
- Note)**
1. NC (Pin 88) is always connected to V_{DD}.
 2. V_{SS} (Pins 39 and 86) are both connected to GND.
 3. MP (Pin 37) is always connected to GND.

Pin Configuration in Evaluator Mode (QFP package)



- Note)**
1. NC (Pin 90) is always connected to VDD.
 2. Vss (Pins 41 and 88) are both connected to GND.
 3. MP (Pin 39) is always connected to GND.

Pin Configuration in Evaluator Mode (LQFP package)



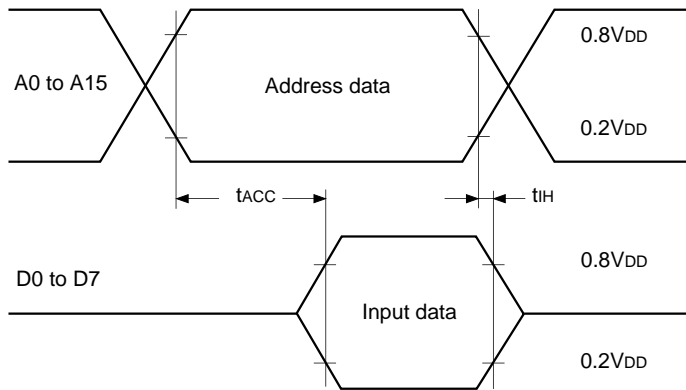
- Note)** 1. NC (Pin 88) is always connected to V_{DD}.
 2. V_{SS} (Pins 39 and 86) are both connected to GND.
 3. MP (Pin 37) is always connected to GND.

EPROM Read Timing ($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 3.0$ to 5.5V , $V_{SS} = 0\text{V}$)

Item	Symbol	Pin	Min.	Max.	Unit
Address → data input delay time	t_{ACC}	A0 to A15 D0 to D7		100*1	ns
				75*2	
Address → data hold time	t_{IH}	A0 to A15 D0 to D7	0		ns

*1 At 12MHz operation ($V_{DD} = 4.5$ to 5.5V)

*2 At 12MHz operation ($V_{DD} = 3.0$ to 5.5V), At 16MHz operation ($V_{DD} = 4.5$ to 5.5V)

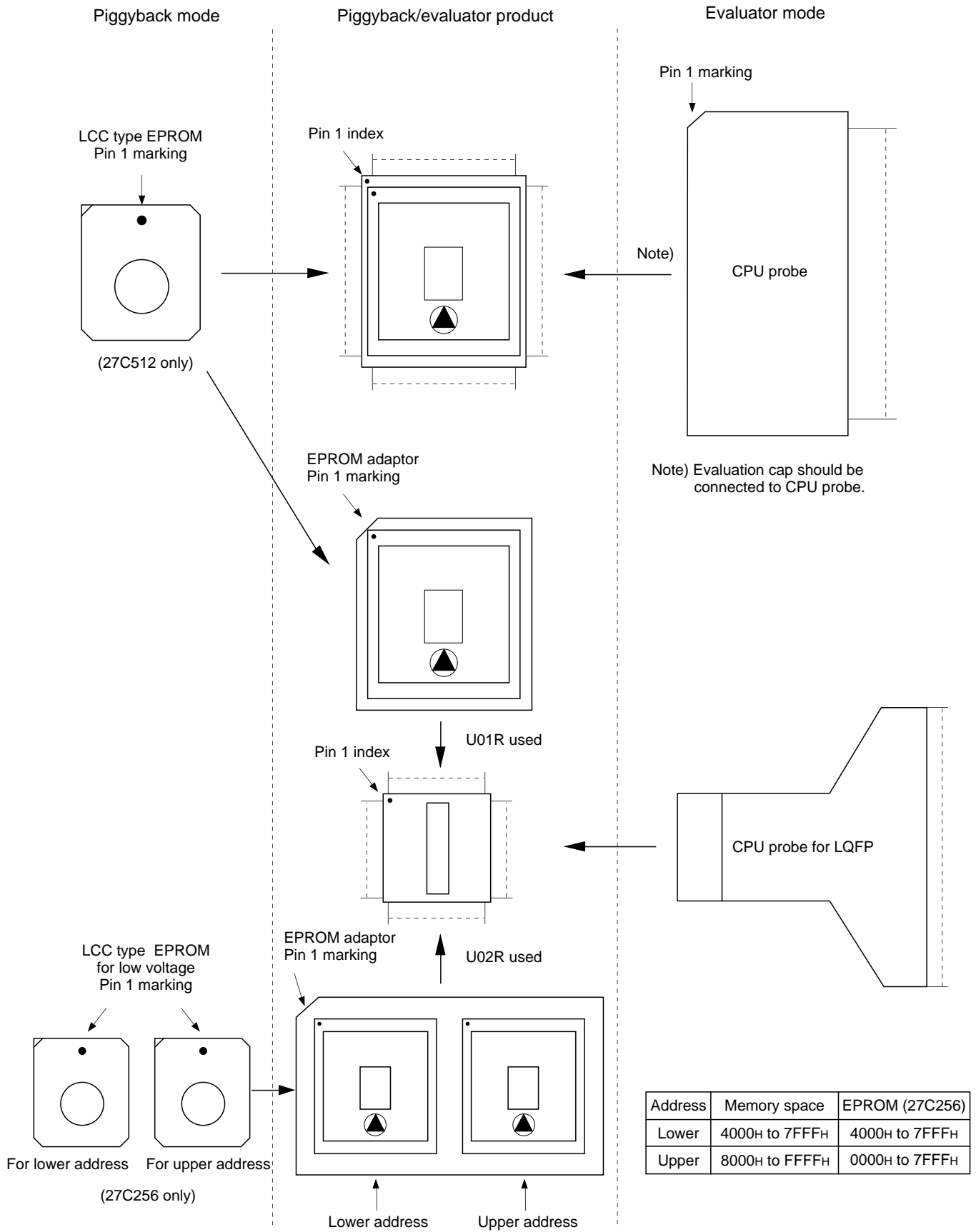


Products List

Optional item	Products			
	Mask product		Piggyback/evaluator product	
	CXP81840A	CXP81848A	CXP81800-U01Q CXP81800-U01R	CXP81800-U02R
Package	100-pin plastic QFP/LQFP		100-pin ceramic PQFP	
ROM capacitance	40Kbytes	48Kbytes	EPROM 48Kbytes	
			27C512 × 1	27C256 × 2
Pull-up resistance for reset pin	Existent/Non-existent		Existent	
Input circuit format*1	CMOS schmitt/TTL schmitt		TTL schmitt	CMOS schmitt

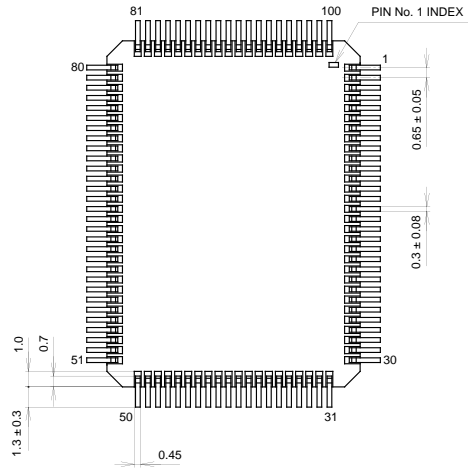
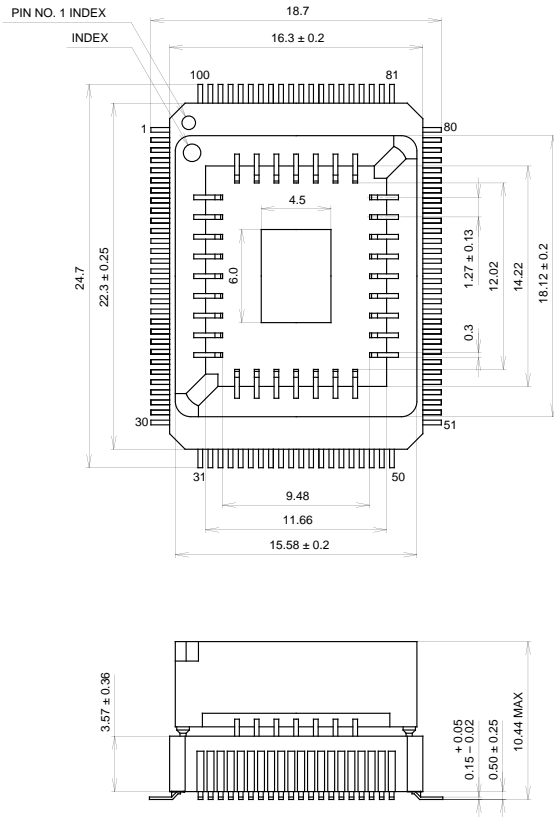
*1 On PG4 pin and PG5 pin, the input circuit format can be selected to every pin.

Piggyback mode/evaluator mode can be switched as shown below



Package Outline Unit: mm

100PIN PQFP (CERAMIC)

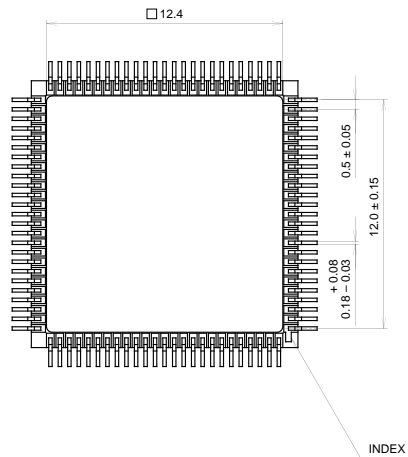
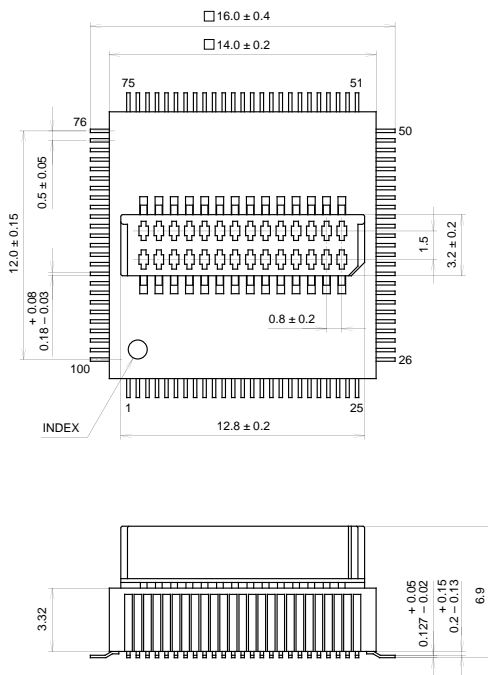


PACKAGE STRUCTURE

SONY CODE	PQFP-100C-L01
EIAJ CODE	AQFP100-C-0000-A
JEDEC CODE	

PACKAGE MATERIAL	CERAMIC
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	5.7g

100PIN PQFP (CERAMIC)



PACKAGE STRUCTURE

SONY CODE	PQFP-100C-L02
EIAJ CODE	AQFP100-C-1414-A
JEDEC CODE	

PACKAGE MATERIAL	CERAMIC
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	2.2g