

CMOS 8-bit Single Chip Microcomputer

Piggyback/
evaluator type**Description**

The CXP84200 is a CMOS 8-bit single chip micro-computer of piggyback/evaluator combined type, which is developed for evaluating the function of the CXP84220/84224.

Features

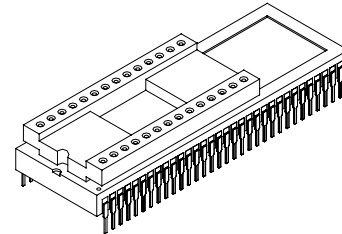
- Wide-range instruction system (213 instructions) to cover various types of data
 - 16-bit operation/multiplication and division/Boolean bit operation instructions
- Minimum instruction cycle 400ns at 10MHz operation
- Applicable EPROM LCC type 27C128, LCC type 27C256
(Maximum 24K bytes are available.)
- Incorporated RAM capacity 624 bytes
- Peripheral functions
 - A/D converter 8-bit, 8-channel, successive approximation method
(Conversion time of 32 μ s/10MHz)
 - Serial interface Incorporated 8-bit, 8-stage FIFO
(Auto transfer for 1 to 8 bytes), 1 channel
8-bit clock sync type, 1 channel
 - Timer 8-bit timer
8-bit timer/counter
19-bit time base timer
16-bit capture timer/counter
 - Remote control reception circuit 8-bit pulse measurement counter with on-chip 6-stage FIFO
 - PWM output 14 bits, 1 channel
- Interruption 14 factors, 14 vectors, multi-interruption possible
- Standby mode Sleep/stop
- Package 64-pin ceramic SDIP

Note) Mask option depends on the type of the CXP84200. Refer to the Products List for details.

Structure

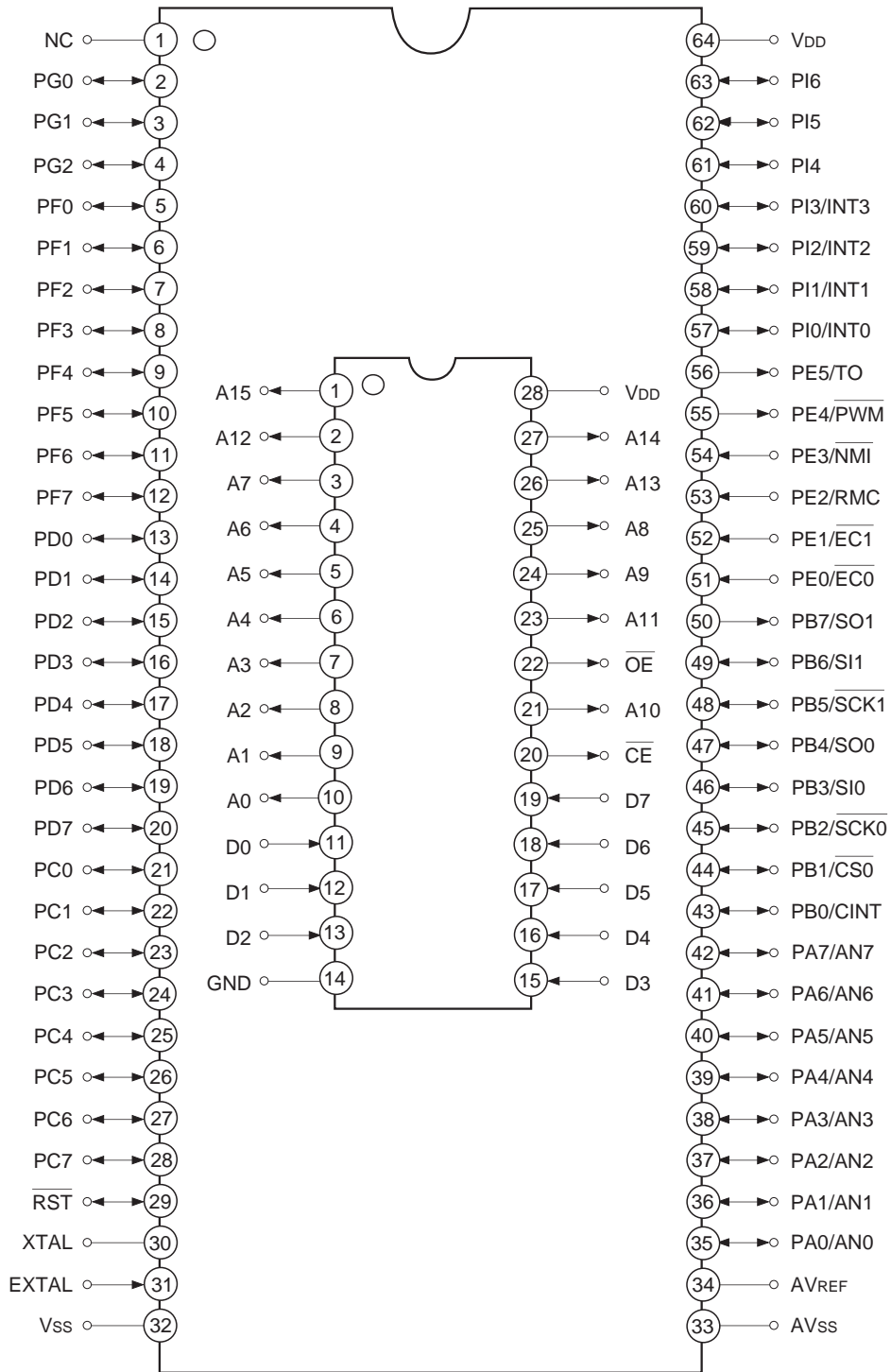
Silicon gate CMOS IC

64 pin PSDIP (Ceramic)



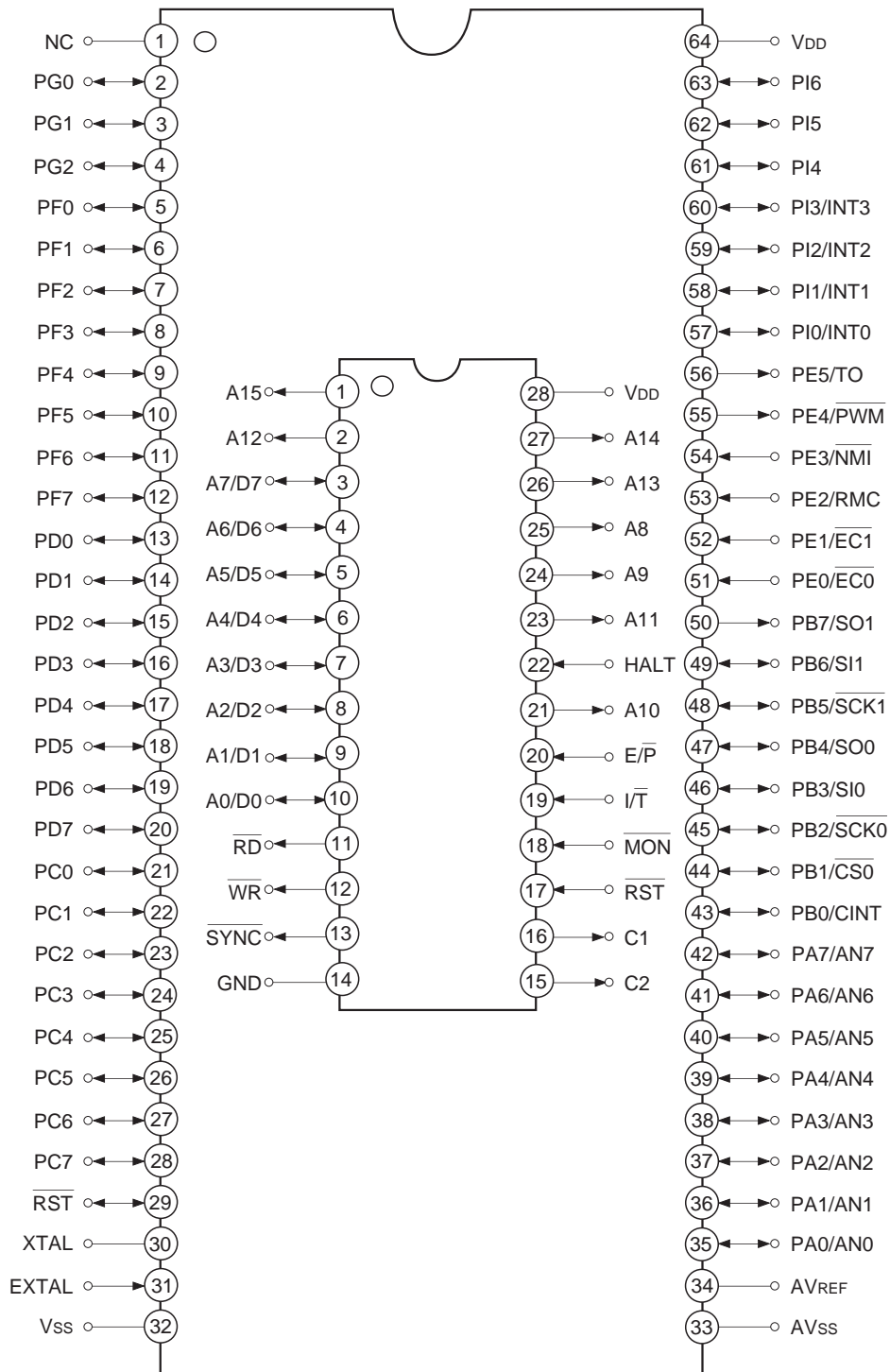
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Pin Assignment in Piggyback Mode



Note) NC (Pin 1) is always connected to V_{DD}.

Pin Assignment in Evaluator Mode

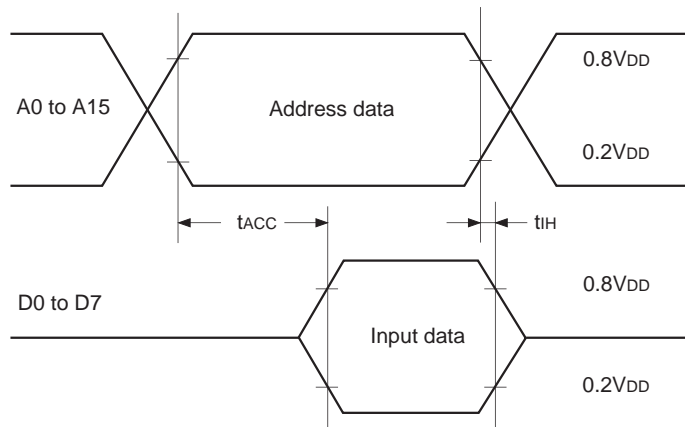


Note) NC (Pin 1) is always connected to VDD.

EPROM Read Timing

($T_a = -20$ to $+75^\circ\text{C}$, $V_{cc} = 4.5$ to 5.5V , $V_{ss} = 0\text{V}$ reference)

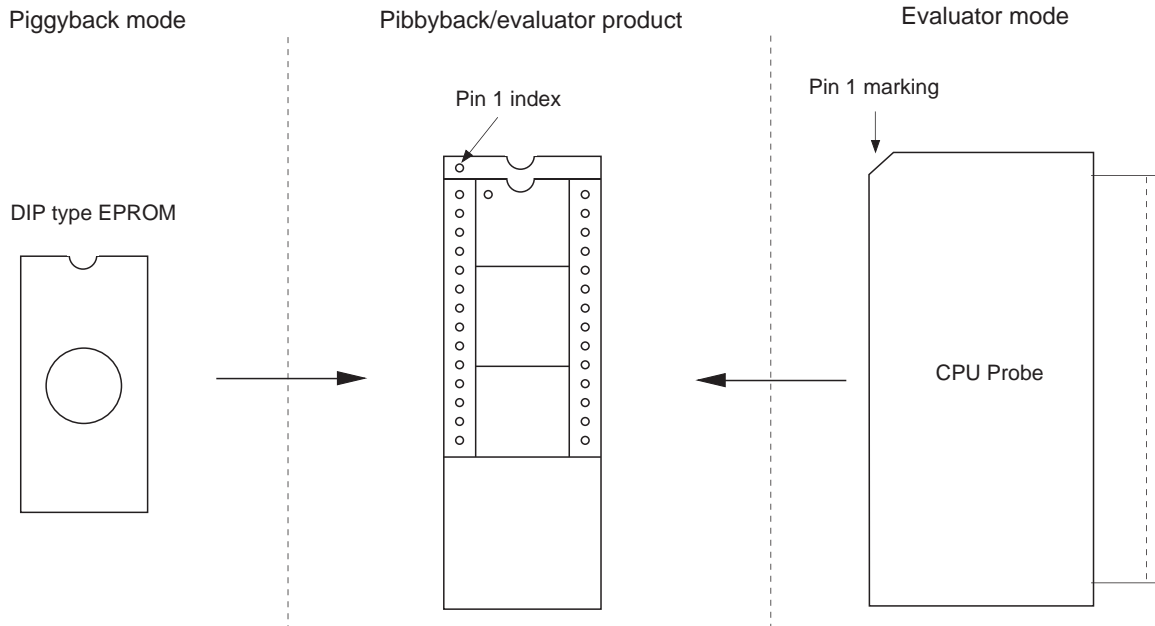
Item	Symbol	Pins	Min.	Max.	Unit
Address → Data Input delay time	t_{ACC}	A0 to A15 D0 to D7		120	ns
Address → Data Hold time	t_{IH}	A0 to A15 D0 to D7	0		ns



Products List

Option item	Products		
	Mask		Piggyback/evaluator
	CXP84220	CXP84224	CXP84200-U01S
Package	64-pin plastic SDIP		64-pin ceramic PSDIP
ROM capacitance	20K bytes	24K bytes	24K bytes
Pull-up resistance for reset pin	Existent/Non-existent		Existent
Power-on reset circuit	Existent/Non-existent		Existent

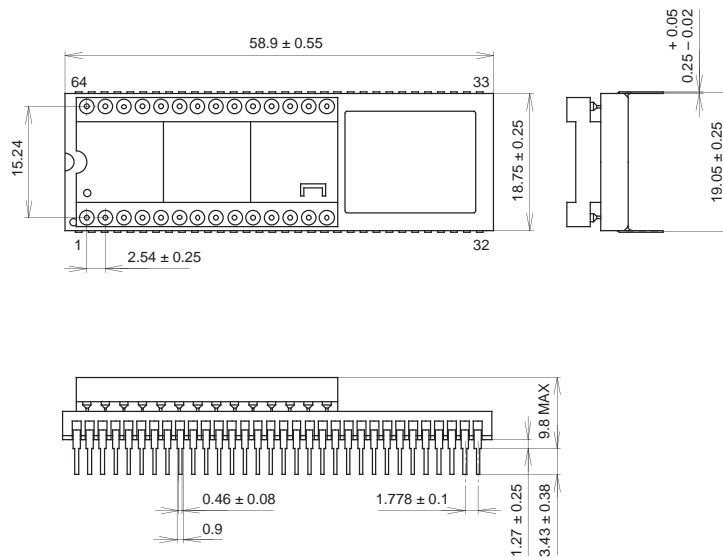
Piggyback mode/evaluator mode can be switched as shown below.



Package Outline

Unit: mm

64PIN PSDIP (CERAMIC) 750mil



PACKAGE STRUCTURE

SONY CODE	PSDIP-64C-01	PACKAGE MATERIAL	CERAMIC
EIAJ CODE	ADIP064-C-0750-A	LEAD TREATMENT	GOLD PLATING
JEDEC CODE	_____	LEAD MATERIAL	42 ALLOY
		PACKAGE WEIGHT	16.0g