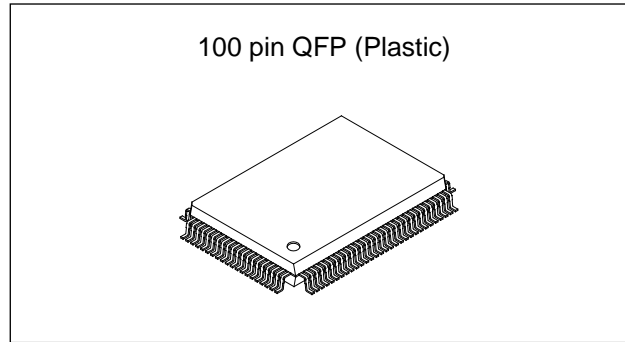


**CMOS 8-bit Single Chip Microcomputer**

**Description**

The CXP88852/88860 is a CMOS 8-bit micro-computer which consists of A/D converter, serial interface, timer/counter, time base timer, high precision timing pattern generation circuits, PWM output, VISS/ VASS circuit, 32kHz timer/counter, remote control receiving circuit, VSYNC separator and the measurement circuit which measure signals of capstan FG amplifier and drum FG/PG amplifier and other servo systems, as well as basic configurations like 8-bit CPU, ROM, RAM and I/O port. They are integrated into a single chip.

Also, CXP88852/88860 provides sleep/stop function which enables to lower power consumption.



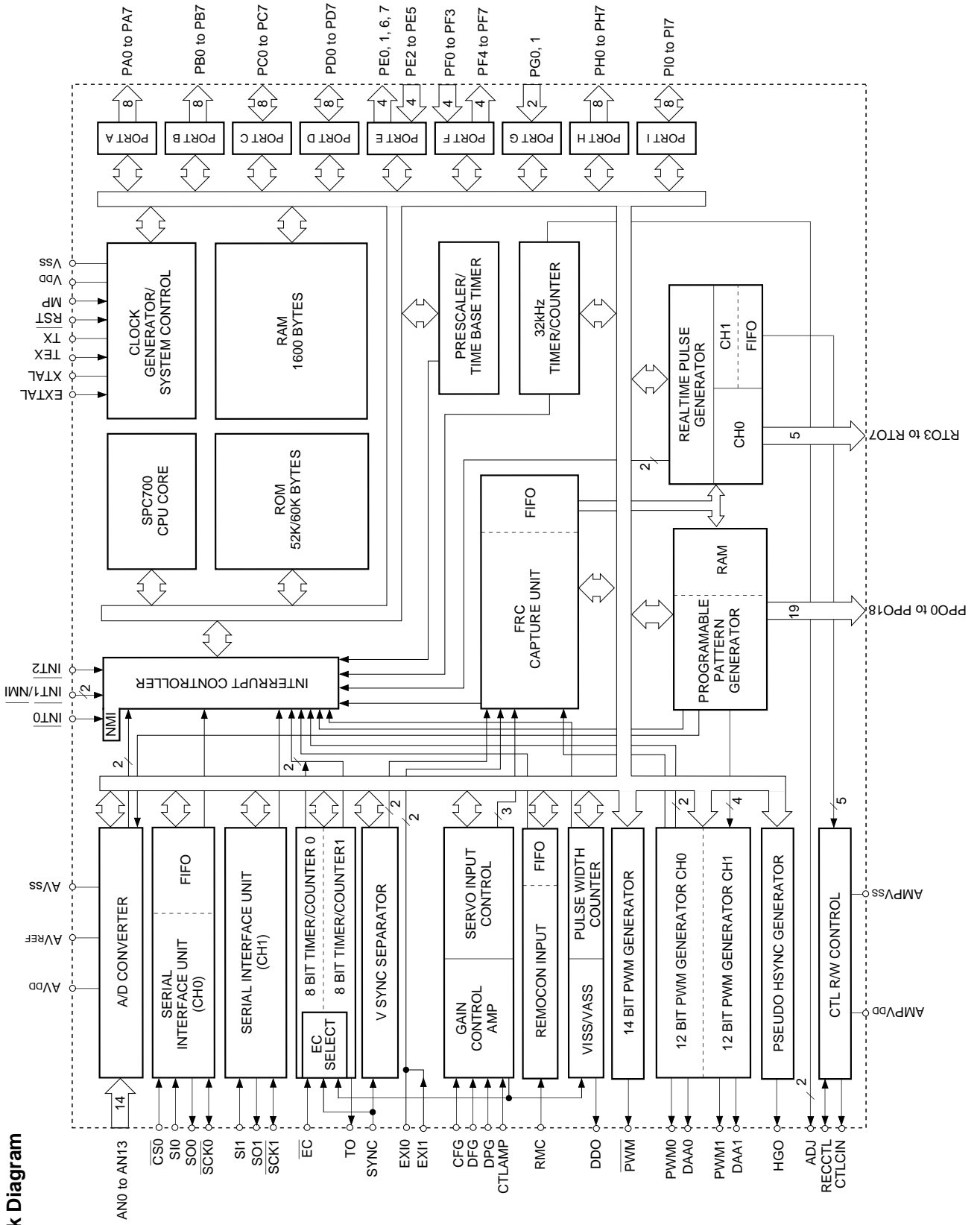
**Structure**

Silicon gate CMOS IC

**Features**

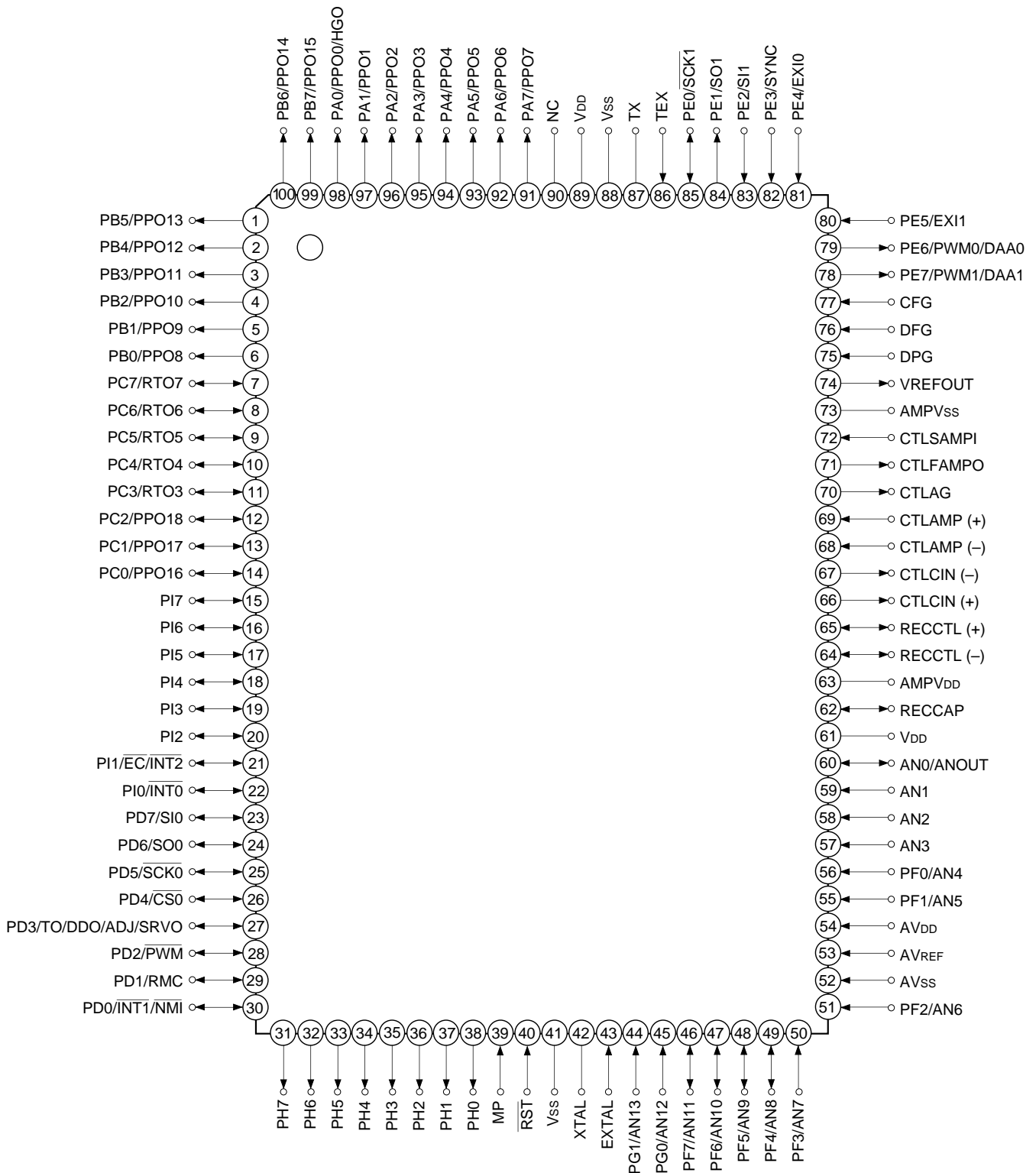
- A wide instruction set (213 instructions) which cover various types of data
  - 16-bit arithmetic/multiplication and division/boolean bit operation instructions
- Minimum instruction cycle
  - 250ns at 16MHz operation
  - 122µs at 32kHz operation
- Incorporated ROM capacity
  - 52K bytes (CXP88852)
  - 60K bytes (CXP88860)
- Incorporated RAM capacity
  - 1600 bytes (including PPG RAM)
- Peripheral function
  - A/D converter
    - 8 bits, 14 channels, successive approximation system (Conversion time of 20µs/16MHz)
  - Serial interface
    - Incorporated 8-bit, 8-stage FIFO for data (Auto transfer for 1 to 8 bytes), 1 channel
    - 8-bit clock sync type, 1 channel
  - Timer
    - 8-bit timer/counter, 2 channels
    - 19-bit time base timer
    - 32kHz timer/counter
  - High precision timing pattern generation
    - PPG 19 pins 32-stage programmable circuit
    - RTG 5 pins, 1 channel
    - 5-bit, 8-stage FIFO (RECCTL control), 1 channel
  - PWM/DA gate output
    - 12 bits, 2 channels (Repetitive frequency 62.5kHz/16MHz)
    - DA gate pulse output, 13 bits, 2 channels
  - Analog signal input circuit
    - Capstan FG amplifier circuit
    - Drum FG amplifier circuit
    - Drum PG amplifier circuit
    - PBCTL amplifier circuit
    - Recording current control circuit
    - Capstan FG, Drum FG/PG, CTL input
  - CTL write/rewrite circuit
    - Incorporated 26-bit and 8-stage FIFO
  - Servo input control
    - 14-bit, 1 channel
  - VSYNC separator
    - Pulse duty auto detection circuit
  - FRC capture unit
    - 32kHz oscillation circuit, ultra-low speed instruction mode
  - PWM output
    - 8-bit pulse measurement counter, 6-stage FIFO
  - VISS/VASS circuit
    - PPG 1 pin, output 8 pins
  - 32kHz timer/event counter
    -
  - Remote control reception circuit
    -
  - Tri-state output
    -
  - Pseudo HSYNC output function
    -
  - High speed head switching circuit
    -
- Interruption
  - 20 factors, 15 vectors, multi-interruption possible
- Standby mode
  - SLEEP/STOP
- Package
  - 100-pin plastic QFP
- Piggyback/evaluation chip
  - CXP88800 100-pin ceramic QFP

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Block Diagram

Pin Assignment (Top View)



- Note)**
1. NC (Pin 90) is always connected to VDD.
  2. VDD (Pins 61 and 89) are both connected to VDD
  3. VSS (Pins 41 and 88) are both connected to GND.
  4. MP (Pin 39) must be connected to GND.

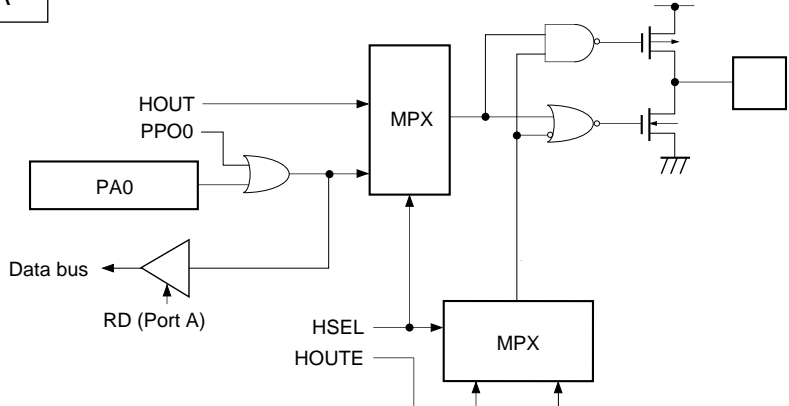
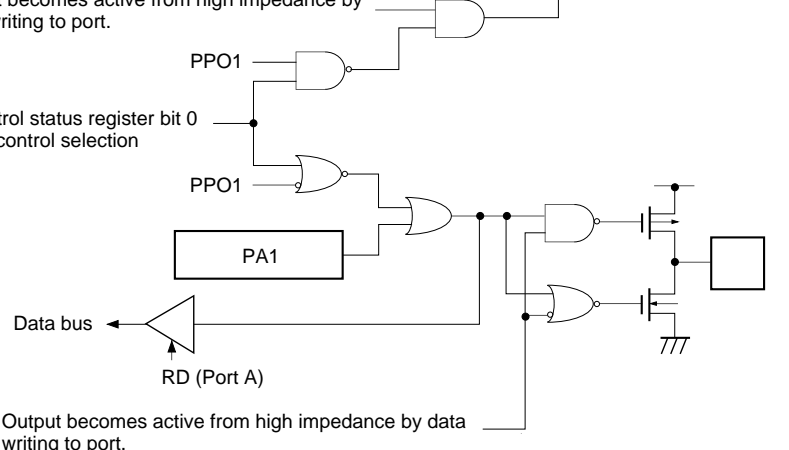
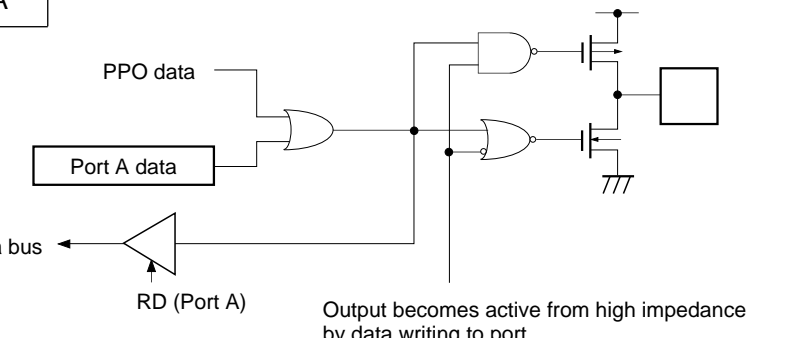
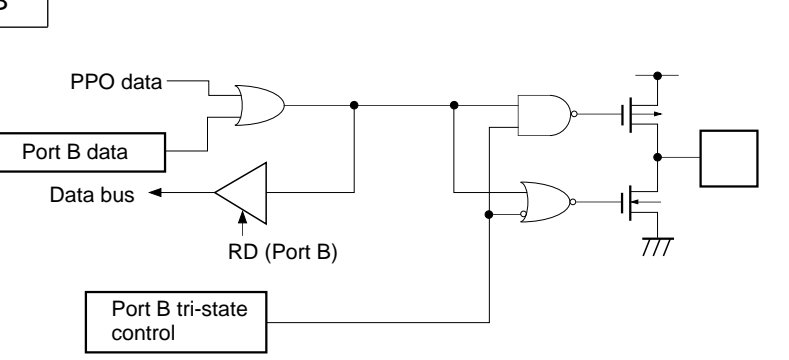
Pin Description

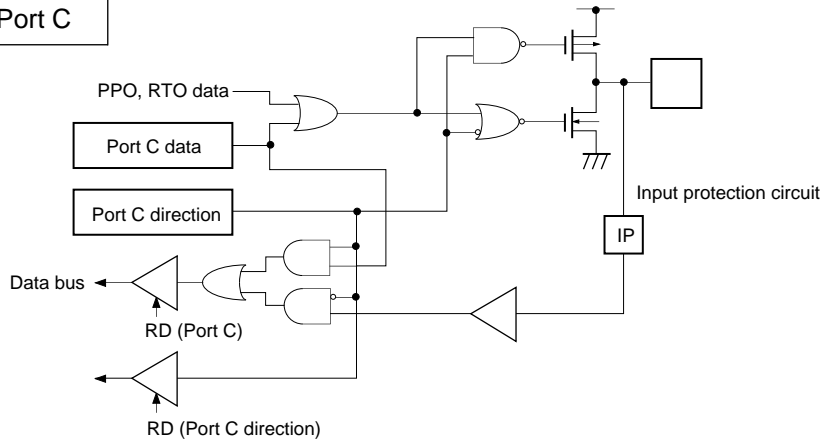
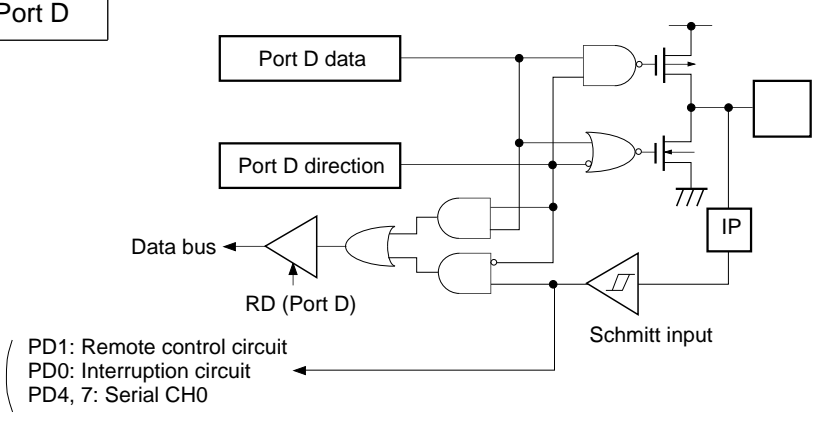
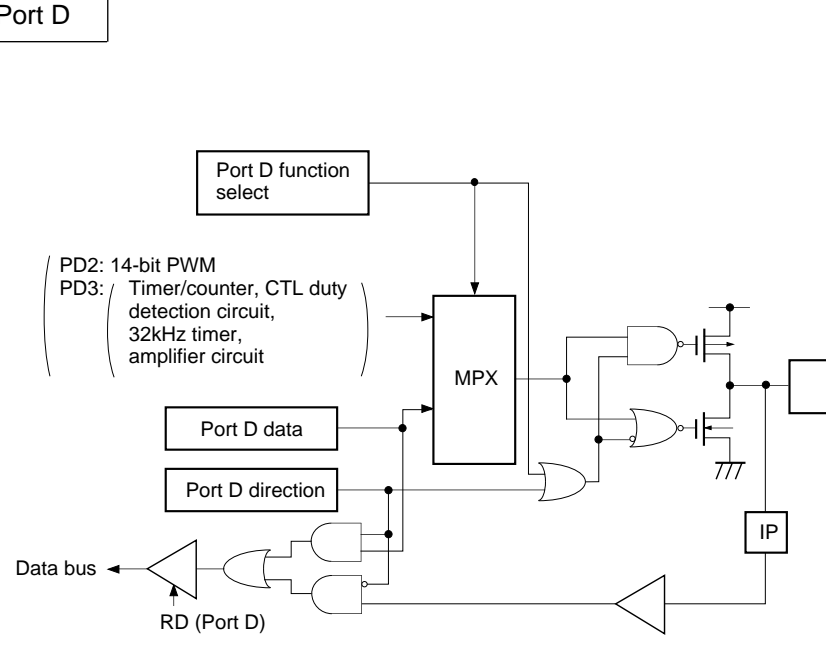
| Symbol                 | I/O                             | Description  |   |
|------------------------|---------------------------------|--|---|
| PA0/PPO0/HGO           | Output/Real-time output/Output  | (Port A)<br>8-bit output port. Data is gated with PPO contents by OR-gate and they are output.<br>(8 pins)   | Pseudo HSYNC output pin.  |
| PA1/PPO1 to PA7/PPO7   | Output/Real-time output         |  |   |
| PB0/PPO8 to PB7/PPO15  | Output/Real-time output         |  | Programmable pattern generator (PPG) output. Functions as high precision real-time pulse output port.<br>(19 pins)<br>PA0 can be tri-state controlled with PPG. |
| PC0/PPO16 to PC2/PPO18 | I/O/Real-time output            | (Port C)<br>8-bit I/O port. I/O can be set in a unit of single bits. Data is gated with PPO or RT contents by OR-gate and they are output.<br>(8 pins) |   |
| PC3/RTO3 to PC7/RTO7   | I/O/Real-time output            |  | Real-time pulse generator (RTG) output. Functions as high precision real-time pulse output port.<br>(5 pins)  |
| PD0/INT1/NMI           | I/O/Input/Input                 | (Port D)<br>8-bit I/O port. I/O can be set in a unit of single bits.<br>(8 pins)   | Input pin to request external interruption and non-maskable interruption.   |
| PD1/RMC                | I/O/Input                       |  | Remote control receiving circuit input pin.   |
| PD2/PWM                | I/O/Output                      |  | 14-bit PWM output pin.  |
| PD3/TO DDO/ADJ SRVO    | I/O/Output/Output/Output/Output |  | Timer/counter, CTL duty detector, 32kHz oscillation adjustment and servo amplifier output pin.  |
| PD4/CS0                | I/O/Input                       |  | Serial chip select (CH0) input pin.   |
| PD5/SCK0               | I/O/I/O                         |  | Serial clock (CH0) I/O pin.   |
| PD6/SO0                | I/O/Output                      |  | Serial data (CH0) output pin.   |
| PD7/SI0                | I/O/Input                       |  | Serial data (CH0) input pin.  |
| PE0/SCK1               | Output/I/O                      |  | Serial clock (CH1) I/O pin  |
| PE1/SO1                | Output/Output                   | Serial data (CH1) output pin   |   |
| PE2/SI1                | Input/Input                     | Serial data (CH1) input pin  |   |
| PE3/SYNC               | Input/Input                     | (Port E)<br>8-bit port. Bits 2, 3, 4 and 5 are for inputs; bits 0, 1, 6 and 7 are for outputs.<br>(8 pins)   | Composite sync signal input pin.  |
| PE4/EXI0               | Input/Input                     |  | External input pin for FRC capture unit.<br>(2 pins)  |
| PE5/EXI1               | Input/Input                     |  |   |
| PE6/PWM0/DAA0          | Output/Output                   |  | PWM output pin.<br>(2 pins)   |
| PE7/PWM1/DAA1          | Output/Output                   |  | DA gate pulse output pin.<br>(2 pins)   |

| Description                     | I/O             | Description  |   |   |
|---------------------------------|-----------------|--|---|---|
| AN0/ANOUT                       | Input/Output    |  | Analog circuit internal waveform output pin.                          |   |
| AN1 to AN3                      | Input           |  |   |   |
| PF0/AN4 to PF3/AN7              | Input/Input     | (Port F)<br>Lower 4 bits are for inputs; upper 4 bits are for outputs. Lower 4 bits are standby release input pins. (8 pins)                         | Analog input pin for A/D converter. (14 pins)                         |   |
| PF4/AN8 to PF7/AN11             | Output/Input    |  |   |   |
| PG0/AN12 PG1/AN13               | Input/Input     |  |   | (Port G)<br>2-bit input port. (2 pins)                                |
| PH0 to PH7                      | Output          | (Port H)<br>8-bit output port; N-ch open drain output of medium drive voltage (12V) and large current (12mA). (8 pins)                               |   |   |
| PI0/ $\overline{\text{INT0}}$   | I/O/Input       | (Port I)<br>8-bit I/O port. I/O can be set in a unit of single bits. Function as standby release input can be set in a unit of single bits. (8 pins) | Input pin to request external interruption. Active when falling edge. |   |
| $\overline{\text{PI1/EC/INT2}}$ | I/O/Input/Input |  | External event input pin for timer/counter.                           | Input pin to request external interruption. Active when falling edge. |
| PI2 to PI7                      | I/O             |  |   |   |
| CFG                             | Input           | Capstan FG input pin.  |   |   |
| DFG                             | Input           | Drum FG input pin.   |   |   |
| DPG                             | Input           | Drum PG input pin.   |   |   |
| RECCTL (+)<br>RECCTL (-)        | I/O             | RECCTL signal output pin. (2 pins)   | PBCTL signal input pin. (2 pins)                                      |   |
| CTLCIN (+)<br>CTLCIN (-)        | Output          | Connected to RECCTL (+) and RECCTL (-) with the internal switch for playback. (2 pins)   |   |   |
| CTLAMP (+)<br>CTLAMP (-)        | Input           | Input PBCTL signal with capacitor coupled. (2 pins)  |   |   |
| CTLFAMPO                        | Output          | PBCTL signal 1st amplifier output.   |   |   |
| CTLSAMPI                        | Input           | PBCTL signal 2nd amplifier input.  |   |   |
| RECCAP                          | I/O             | Capacitor connecting pin for the slope setting of the CTL writing trapezoidal wave.  |   |   |
| VREFOUT                         | Output          | Capacitor connecting pin for the VREF level smoothing of DPG, DFG and CFG.   |   |   |
| CTLAG                           | Output          | Capacitor connecting pin for the CTL and AGND smoothing.   |   |   |
| AMPV <sub>SS</sub>              |                 | Analog signal input circuit GND pin.   |   |   |
| AMPV <sub>DD</sub>              |                 | Analog signal input circuit power supply pin.  |   |   |

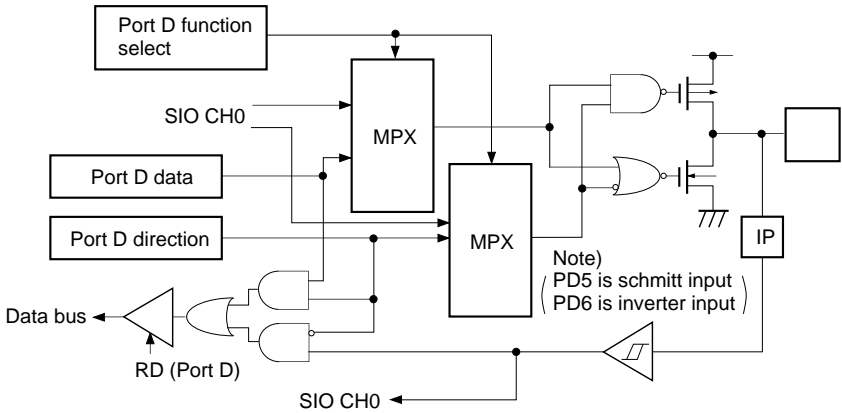
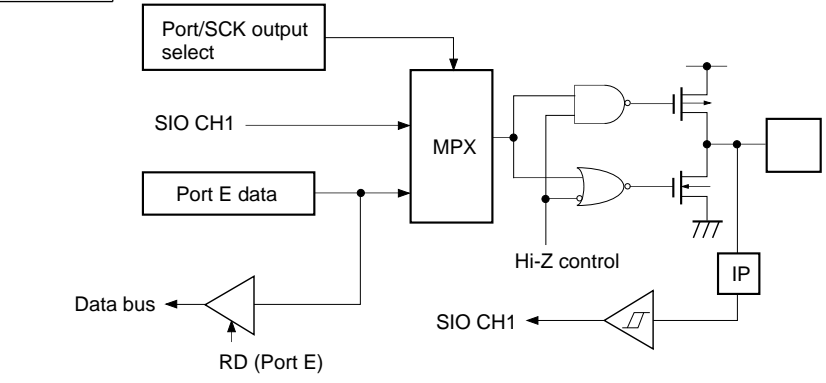
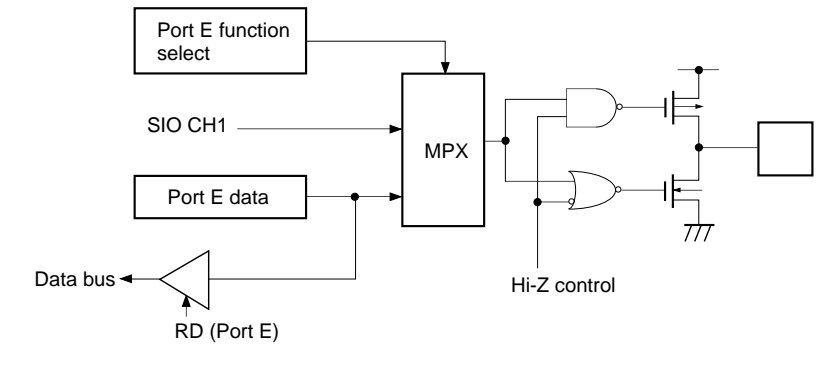
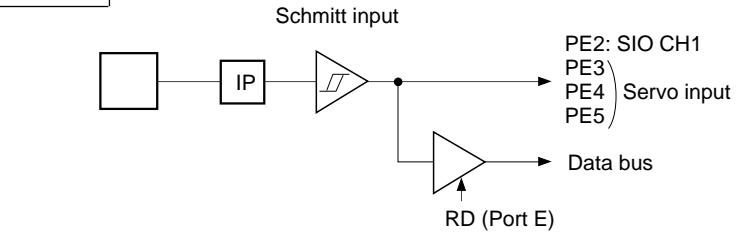
| Symbol                  | I/O    | Description   |
|-------------------------|--------|---|
| EXTAL                   | Input  | Connecting pin of crystal oscillator for system clock. When supplying the external clock, input it to EXTAL pin and input the opposite phase clock to XTAL pin.                   |
| XTAL                    | Output |   |
| TEX                     | Input  | Connecting pin of crystal oscillator for 32kHz timer clock. When used as event counter, input to TEX pin and leave TX pin open. (In this time, feedback resistor is not removed.) |
| TX                      | Output |   |
| $\overline{\text{RST}}$ | Input  | System reset pin; Low level active.   |
| NC                      |        | NC pin. Connect this pin to $V_{DD}$ for normal operation.  |
| MP                      | Input  | Test mode input pin. Always connect to GND.   |
| $AV_{DD}$               |        | Positive power supply pin for A/D converter.  |
| $AV_{REF}$              | Input  | Reference voltage input pin for A/D converter.  |
| $AV_{SS}$               |        | GND pin for A/D converter.  |
| $V_{DD}$                |        | Positive power supply pin.  |
| $V_{SS}$                |        | GND pin. Connect both $V_{SS}$ pins to GND.   |

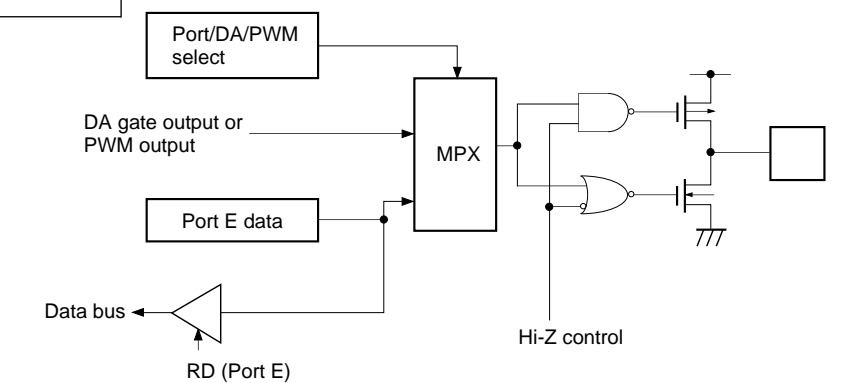
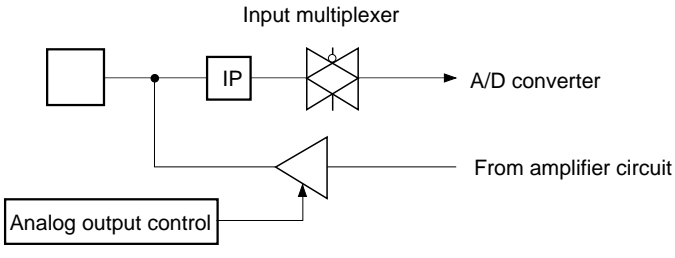
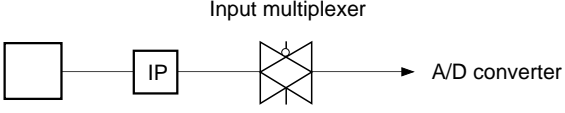
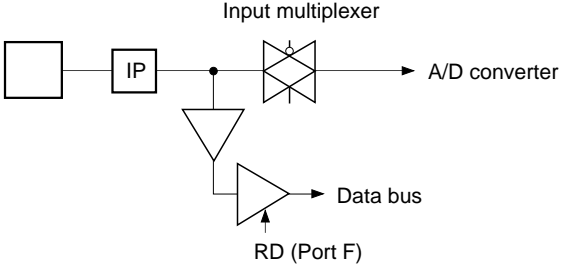
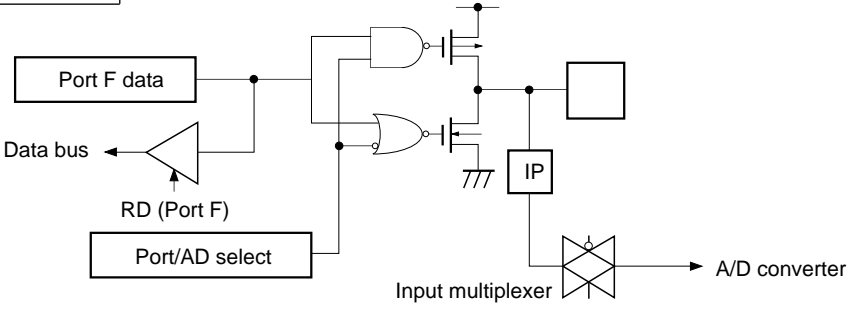
Input/Output Circuit Formats for Pins

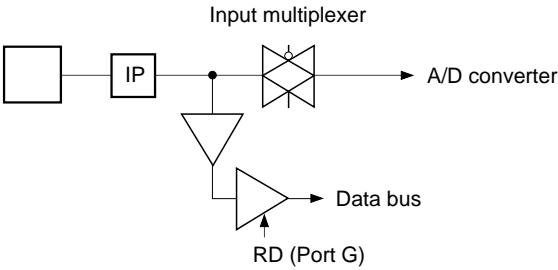
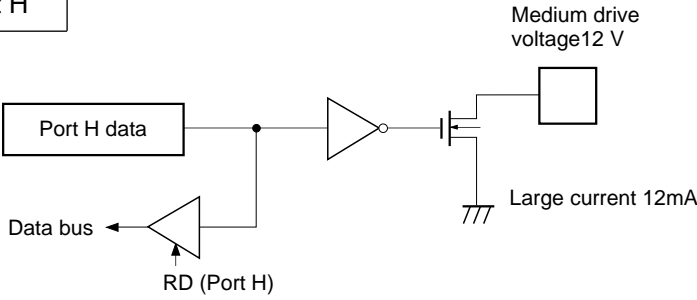
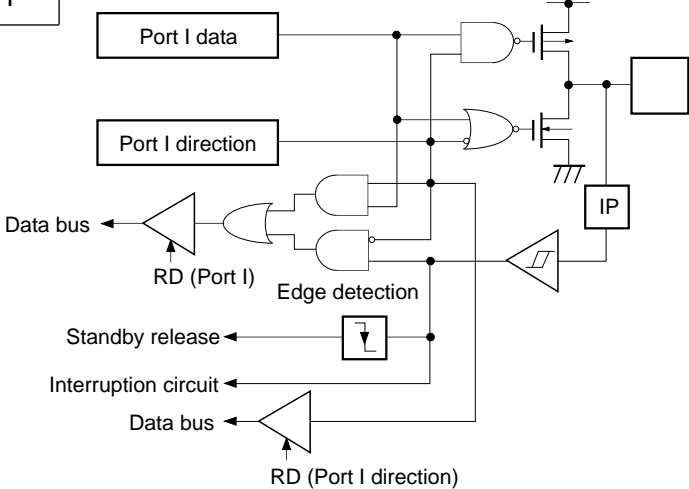
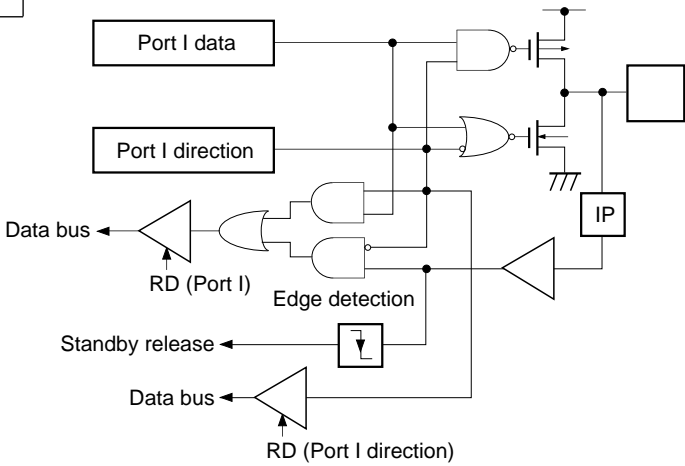
| Pin   | Circuit format   | When reset  |
|---|--|-------------|
| <p>PA0/PPO0/<br/>HGO<br/>1 pin</p>              | <p>Port A</p>  <p>Output becomes active from high impedance by data writing to port.</p>  <p>Output becomes active from high impedance by data writing to port.</p> | <p>Hi-Z</p> |
| <p>PA2/PPO2<br/>to<br/>PA7/PPO7<br/>6 pins</p>  | <p>Port A</p>  <p>Output becomes active from high impedance by data writing to port.</p>   | <p>Hi-Z</p> |
| <p>PB0/PPO8<br/>to<br/>PB7/PPO15<br/>8 pins</p> | <p>Port B</p>  <p>Output becomes active from high impedance by data writing to port.</p>   | <p>Hi-Z</p> |

| Pin  | Circuit format   | When reset  |
|--|--|-------------|
| <p>PC0/PPO16<br/>to<br/>PC2/PPO18</p> <p>PC3/RTO3<br/>to<br/>PC7/RTO7</p> <p>8 pins</p>  | <p>Port C</p>    | <p>Hi-Z</p> |
| <p>PD0/<math>\overline{\text{INT1}}</math>/<br/>NMI<br/>PD1/<math>\overline{\text{RMC}}</math><br/>PD4/<math>\overline{\text{CS0}}</math><br/>PD7/<math>\overline{\text{SI0}}</math></p> <p>4 pins</p> | <p>Port D</p>  <p>( PD1: Remote control circuit<br/>PD0: Interruption circuit<br/>PD4, 7: Serial CH0</p>                                  | <p>Hi-Z</p> |
| <p>PD2/<math>\overline{\text{PWM}}</math><br/>PD3/<math>\overline{\text{TO}}</math>/<br/>DDO/<math>\overline{\text{ADJ}}</math>/<br/>SRVO</p> <p>2 pins</p>  | <p>Port D</p>  <p>( PD2: 14-bit PWM<br/>PD3: ( Timer/counter, CTL duty<br/>detection circuit,<br/>32kHz timer,<br/>amplifier circuit</p> | <p>Hi-Z</p> |



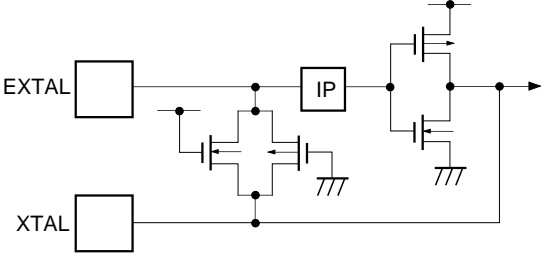
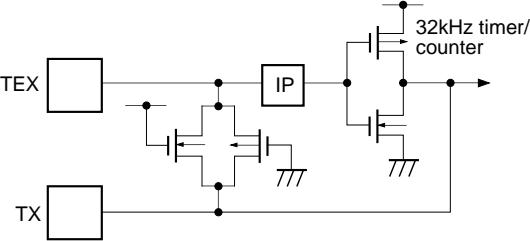
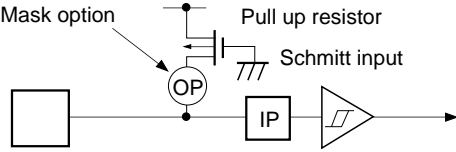
| Pin   | Circuit format   | When reset  |
|---|--|-------------|
| <p>PD5/<math>\overline{\text{SCK0}}</math><br/>PD6/<math>\overline{\text{SO0}}</math></p> <p>2 pins</p>   | <p>Port D</p>  <p>Note)<br/>PD5 is schmitt input<br/>PD6 is inverter input</p>   | <p>Hi-Z</p> |
| <p>PE0/<math>\overline{\text{SCK1}}</math></p> <p>1 pin</p>   | <p>Port E</p>   | <p>Hi-Z</p> |
| <p>PE1/<math>\overline{\text{SO1}}</math></p> <p>1 pin</p>  | <p>Port E</p>    | <p>Hi-Z</p> |
| <p>PE2/<math>\overline{\text{SI1}}</math><br/>PE3/<math>\overline{\text{SYNC}}</math><br/>PE4/<math>\overline{\text{EXI0}}</math><br/>PE5/<math>\overline{\text{EXI1}}</math></p> <p>4 pins</p> | <p>Port E</p>  <p>Note) For PE3/<math>\overline{\text{SYNC}}</math>, CMOS schmitt input or TTL schmitt input can be selected with the mask option.</p> | <p>Hi-Z</p> |

| Pin  | Circuit format   | When reset        |
|--|--|-------------------|
| <p>PE6/PWM0/<br/>DAA0<br/>PE7/PWM1/<br/>DAA1</p> <p>2 pins</p> | <p>Port E</p>    | <p>High level</p> |
| <p>AN0/ANOUT</p> <p>1 pin</p>                                  | <p>Port E</p>   | <p>Hi-Z</p>       |
| <p>AN1<br/>to<br/>AN3</p> <p>3 pin</p>                         |                | <p>Hi-Z</p>       |
| <p>PFO/AN4<br/>to<br/>PF3/AN7</p> <p>4 pins</p>                | <p>Port F</p>  | <p>Hi-Z</p>       |
| <p>PF4/AN8<br/>to<br/>PF7/AN11</p> <p>4 pins</p>               | <p>Port F</p>  | <p>Hi-Z</p>       |

| Pin  | Circuit format  | When reset  |
|--|---|-------------|
| <p>PG0/AN12<br/>to<br/>PG1/AN13</p> <p>2 pins</p>  | <p>Port G</p>  <p>Input multiplexer</p> <p>A/D converter</p> <p>Data bus</p> <p>RD (Port G)</p>   | <p>Hi-Z</p> |
| <p>PH0<br/>to<br/>PH7</p> <p>8 pins</p>  | <p>Port H</p>  <p>Port H data</p> <p>Data bus</p> <p>RD (Port H)</p> <p>Medium drive voltage 12 V</p> <p>Large current 12mA</p>   | <p>Hi-Z</p> |
| <p>PI0/<math>\overline{\text{INT0}}</math><br/>to<br/>PI1/<math>\overline{\text{EC/INT2}}</math></p> <p>2 pins</p> | <p>Port I</p>  <p>Port I data</p> <p>Port I direction</p> <p>Data bus</p> <p>RD (Port I)</p> <p>Edge detection</p> <p>Standby release</p> <p>Interruption circuit</p> <p>Data bus</p> <p>RD (Port I direction)</p> <p>IP</p> | <p>Hi-Z</p> |
| <p>PI2<br/>to<br/>PI7</p> <p>6 pins</p>  | <p>Port I</p>  <p>Port I data</p> <p>Port I direction</p> <p>Data bus</p> <p>RD (Port I)</p> <p>Edge detection</p> <p>Standby release</p> <p>Data bus</p> <p>RD (Port I direction)</p> <p>IP</p>                            | <p>Hi-Z</p> |

| Pin   | Circuit format  | When reset                  |
|---|---|-----------------------------|
| <p>CTLAMP (+)<br/>CTLAMP (-)<br/>CTLFAMPO</p> <p>3 pins</p> |   | <p>1/2AMPV<sub>DD</sub></p> |
| <p>CTLSAMPI</p> <p>1 pin</p>                                |   | <p>1/2AMPV<sub>DD</sub></p> |
| <p>CFG<br/>DFG<br/>DPG</p> <p>3 pins</p>                    |   | <p>1/2AMPV<sub>DD</sub></p> |
| <p>CTLAG<br/>VREFOUT</p> <p>2 pins</p>                      | <p>VREFOUT: CFG, DFG,<br/>DPG amplifiers<br/>CTLAG: CTL amplifier</p> | <p>1/2AMPV<sub>DD</sub></p> |

| Pin                             | Circuit format | When reset       |
|---------------------------------|----------------|------------------|
| <p>RECCTL (+)</p> <p>1 pin</p>  |                | <p>Hi-Z</p>      |
| <p>RECCTL (-)</p> <p>1 pin</p>  |                | <p>Hi-Z</p>      |
| <p>CTL CIN (+)</p> <p>1 pin</p> |                | <p>Hi-Z</p>      |
| <p>CTL CIN (-)</p> <p>1 pin</p> |                | <p>Hi-Z</p>      |
| <p>RECCAP</p> <p>1 pin</p>      |                | <p>Low level</p> |

| Pin  | Circuit format   | When reset         |
|--|--|--------------------|
| <p>EXTAL<br/>XTAL</p> <p>2 pins</p>                    |  <p>* Shows the circuit composition during oscillation.</p> <p>* Feedback resistor is removed and XTAL outputs High level during stop.</p>  | <p>Oscillation</p> |
| <p>TEX<br/>TX</p> <p>2 pins</p>                        |  <p>* Shows the circuit composition during oscillation.</p> <p>* Feedback resistor is removed during 32kHz oscillation circuit stop by software. At this time, TEX pin outputs Low level and TX pin outputs High level.</p> | <p>Oscillation</p> |
| <p><math>\overline{\text{RST}}</math></p> <p>1 pin</p> |  <p>Mask option</p> <p>Pull up resistor</p> <p>Schmitt input</p>  | <p>Low level</p>   |

## Absolute Maximum Ratings

(V<sub>SS</sub> = 0V reference)

| Item                            | Symbol             | Rating                                   | Unit | Remarks   |
|---------------------------------|--------------------|--|------|---|
| Supply voltage                  | V <sub>DD</sub>    | -0.3 to +7.0                             | V    |   |
|                                 | AV <sub>DD</sub>   | AV <sub>SS</sub> to +7.0* <sup>1</sup>   | V    |   |
|                                 | AV <sub>SS</sub>   | -0.3 to +0.3                             | V    |   |
|                                 | AMPV <sub>DD</sub> | AMPV <sub>SS</sub> to +7.0* <sup>2</sup> | V    |   |
|                                 | AMPV <sub>SS</sub> | -0.3 to +0.3                             | V    |   |
| Input voltage                   | V <sub>IN</sub>    | -0.3 to +7.0* <sup>3</sup>               | V    |   |
| Output voltage                  | V <sub>OUT</sub>   | -0.3 to +7.0* <sup>3</sup>               | V    |   |
| Medium drive output voltage     | V <sub>OUTP</sub>  | -0.3 to +15.0                            | V    | Port H  |
| High level output current       | I <sub>OH</sub>    | -5                                       | mA   |   |
| High level total output current | ∑I <sub>OH</sub>   | -50                                      | mA   | Total of output pins                                    |
| Low level output current        | I <sub>OL</sub>    | 15                                       | mA   | Other than large current output ports (value per pin)   |
|                                 | I <sub>OLC</sub>   | 20                                       | mA   | Large current output port* <sup>4</sup> (value per pin) |
| Low level total output current  | ∑I <sub>OL</sub>   | 130                                      | mA   | Total of output pins                                    |
| Operating temperature           | T <sub>opr</sub>   | -20 to +75                               | °C   |   |
| Storage temperature             | T <sub>stg</sub>   | -55 to +150                              | °C   |   |
| Allowable power dissipation     | P <sub>D</sub>     | 600                                      | mW   | QFP package type  |

\*1 AV<sub>DD</sub> and V<sub>DD</sub> must not exceed +0.3V.

\*2 AMPV<sub>DD</sub> and V<sub>DD</sub> must not exceed +0.3V.

\*3 V<sub>IN</sub> and V<sub>OUT</sub> must not exceed V<sub>DD</sub> +0.3V.

\*4 The large current output port is port H (PH).

**Note)** Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

## Recommended Operating Conditions

(V<sub>SS</sub> = 0V)

| Item                     | Symbol             | Min.                  | Max.                  | Unit | Remarks   |
|--------------------------|--------------------|-----------------------|-----------------------|------|---|
| Supply voltage           | V <sub>DD</sub>    | 4.5                   | 5.5                   | V    | Guaranteed operation range for 1/2 and 1/4 frequency dividing clock               |
|                          |                    | 3.5                   | 5.5                   |      | Guaranteed operation range for 1/16 frequency dividing clock or during SLEEP mode |
|                          |                    | 2.7                   | 5.5                   |      | Guaranteed operation range by TEX clock   |
|                          |                    | 2.5                   | 5.5                   |      | Guaranteed data hold operation range during STOP                                  |
| Analog power supply      | AV <sub>DD</sub>   | 4.5                   | 5.5                   | V    | *1  |
|                          | AMPV <sub>DD</sub> | 4.5                   | 5.5                   | V    | *2  |
| High level input voltage | V <sub>IH</sub>    | 0.7V <sub>DD</sub>    | V <sub>DD</sub>       | V    | *3  |
|                          | V <sub>IHS</sub>   | 0.8V <sub>DD</sub>    | V <sub>DD</sub>       | V    | CMOS schmitt input*4  |
|                          | V <sub>IHTS</sub>  | 2.2                   | V <sub>DD</sub>       | V    | TTL schmitt input*5   |
|                          | V <sub>IHEX</sub>  | V <sub>DD</sub> - 0.4 | V <sub>DD</sub> + 0.3 | V    | EXTAL pin*6 TEX pin*7   |
| Low level input voltage  | V <sub>IL</sub>    | 0                     | 0.3V <sub>DD</sub>    | V    | *3  |
|                          | V <sub>ILS</sub>   | 0                     | 0.2V <sub>DD</sub>    | V    | CMOS schmitt input*4  |
|                          | V <sub>ILTS</sub>  | 0                     | 0.8                   | V    | TTL schmitt input*5   |
|                          | V <sub>ILEX</sub>  | -0.3                  | 0.4                   | V    | EXTAL pin*6 TEX pin*7   |
| Operating temperature    | Topr               | -20                   | +75                   | °C   |   |

\*1 AV<sub>DD</sub> and V<sub>DD</sub> should be set to the same voltage.

\*2 AMPV<sub>DD</sub> and V<sub>DD</sub> should be set to the same voltage.

\*3 Normal input port (each pin of PC, PD2, PD3, PD6, PF0 to PF3, PG and PI2 to PI7), MP pin

\*4 Each pin of  $\overline{RST}$ , PD0/ $\overline{INT1}$ / $\overline{NM}$ , PD1/RMC, PD4/ $\overline{CS0}$ , PD5/SCK0, PD7/SI0, PE0/ $\overline{SCK1}$ , PE2/SI1, PE3/SYNC, PE4/EXI0, PE5/EXI1, PI0/ $\overline{INT0}$ , PI1/ $\overline{EC}$ / $\overline{INT2}$  (For PE3/SYNC, when CMOS schmitt input is selected with mask option.)

\*5 PE3/SYNC (when TTL schmitt input is selected with mask option.)

\*6 Specifies only during external clock input.

\*7 Specifies only during external event input.



**Electrical Characteristics**

**DC Characteristics** ( $V_{DD} = 4.5$  to  $5.5V$ )

( $T_a = -20$  to  $+75^{\circ}C$ ,  $V_{SS} = 0V$  reference)

| Item  | Symbol     | Pins   | Conditions                                       | Min.   | Typ. | Max.     | Unit    |         |
|---|------------|--|--|--|------|----------|---------|---------|
| High level output voltage                             | $V_{OH}$   | PA to PD, PE0 to PE1, PE6 to PE7,  | $V_{DD} = 4.5V, I_{OH} = -0.5mA$                 | 4.0  |      |          | V       |         |
|   |            |  | $V_{DD} = 4.5V, I_{OH} = -1.2mA$                 | 3.5  |      |          | V       |         |
| Low level output voltage                              | $V_{OL}$   | PF4 to PF7, PH ( $V_{OL}$ only) PI   | $V_{DD} = 4.5V, I_{OL} = 1.8mA$                  |  |      | 0.4      | V       |         |
|   |            |  | $V_{DD} = 4.5V, I_{OL} = 3.6mA$                  |  |      | 0.6      | V       |         |
|   |            |  | $V_{DD} = 4.5V, I_{OL} = 12.0mA$                 |  |      | 1.5      | V       |         |
| Input current   | $I_{IHE}$  | EXTAL  | $V_{DD} = 5.5V, V_{IH} = 5.5V$                   | 0.5  |      | 40       | $\mu A$ |         |
|   | $I_{ILE}$  |  | $V_{DD} = 5.5V, V_{IL} = 0.4V$                   | -0.5   |      | -40      | $\mu A$ |         |
|   | $I_{IHT}$  | TEX  | $V_{DD} = 5.5V, V_{IH} = 5.5V$                   | 0.1  |      | 10       | $\mu A$ |         |
|   | $I_{ILT}$  |  | $V_{DD} = 5.5V, V_{IL} = 0.4V$                   | -0.1   |      | -10      | $\mu A$ |         |
|   | $I_{ILR}$  |  | $\overline{RST}^{*1}$                            | $V_{IL} = 0.4V$                                  | -1.5 |          | -400    | $\mu A$ |
| I/O leakage current                                   | $I_{IZ}$   | PA to PG, PI, MP, AN0 to AN3, $\overline{RST}^{*1}$  | $V_{DD} = 5.5V, V_I = 0, 5.5V$                   |  |      | $\pm 10$ | $\mu A$ |         |
| Open drain output leakage current (N-CH Tr off state) | $I_{LOH}$  | PH   | $V_{DD} = 5.5V, V_{OH} = 12V$                    |  |      | 50       | $\mu A$ |         |
| Supply current*2                                      | $I_{DD1}$  | $V_{DD}, V_{SS}$   | 16MHz crystal oscillation ( $C_1 = C_2 = 15pF$ ) |  | 35   | 45       | mA      |         |
|   |            |  | $V_{DD} = 5.5V^{*3}$                             |  |      |          |         |         |
|   | $I_{DSD1}$ |  | SLEEP mode                                       |  | 2.0  | 8        | mA      |         |
|   |            |  | $V_{DD} = 5.5V$                                  |  |      |          |         |         |
|   | $I_{DD2}$  |  |  | 32kHz crystal oscillation ( $C_1 = C_2 = 47pF$ ) |      | 50       | 100     | $\mu A$ |
|   |            |  |  | $V_{DD} = 3.3V$                                  |      |          |         |         |
| $I_{DSD2}$  |            | SLEEP mode   |  | 9  | 35   | $\mu A$  |         |         |
|   |            | $V_{DD} = 3V \pm 0.3V$   |  |  |      |          |         |         |
| $I_{DSD3}$  |            | STOP mode (EXTAL and TEX pins oscillation stop)  |  |  | 10   | $\mu A$  |         |         |
|   |            | $V_{DD} = 5V \pm 0.5V$   |  |  |      |          |         |         |
| Input capacity  | $C_{IN}$   | PC, PD, PE0, PE2 to PE5, PF, PG, PI, RECCTL (+), RECCTL (-), CTLAMP (+), CTLAMP (-), CTLSAMPI, CFG, DFG, DPG, EXTAL, TEX | Clock 1MHz<br>0V other than the measured pins    |  | 10   | 20       | pF      |         |

\*1  $\overline{RST}$  pin specifies the input current when the pull-up resistor is selected, and specifies leakage current when no resistor is selected.

\*2 When entire output pins are open.

\*3 When setting upper 2 bits (CPU clock selection) of clock control register (CLC: 00FE<sub>H</sub>) to "00" and operating in high speed mode (1/2 frequency dividing clock).

AC Characteristics

(1) Clock timing

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V reference)

| Item  | Symbol                               | Pin             | Condition   | Min.                     | Typ.   | Max. | Unit |
|---|--------------------------------------|-----------------|---|--------------------------|--------|------|------|
| System clock frequency                      | fc                                   | XTAL<br>EXTAL   | Fig. 1, Fig. 2  | 1                        |        | 16   | MHz  |
| System clock input pulse width              | t <sub>XL</sub> ,<br>t <sub>XH</sub> | XTAL<br>EXTAL   | Fig. 1, Fig. 2<br>External clock drive                                  | 28                       |        |      | ns   |
| System clock input rise and fall times      | t <sub>CR</sub> ,<br>t <sub>CF</sub> | XTAL<br>EXTAL   | Fig. 1, Fig. 2<br>External clock drive                                  |                          |        | 200  | ns   |
| Event count clock input pulse width         | t <sub>EH</sub> ,<br>t <sub>EL</sub> | $\overline{EC}$ | Fig. 3  | t <sub>sys</sub> + 200*1 |        |      | ns   |
| Event count clock input rise and fall times | t <sub>ER</sub> ,<br>t <sub>EF</sub> | $\overline{EC}$ | Fig. 3  |                          |        | 20   | ms   |
| System clock frequency                      | fc                                   | TEX<br>TX       | V <sub>DD</sub> = 2.7 to 5.5V<br>Fig. 2 (32kHz clock applied condition) |                          | 32.768 |      | kHz  |
| Event count clock input pulse width         | t <sub>TL</sub> ,<br>t <sub>TH</sub> | TEX             | Fig. 3  | 10                       |        |      | μs   |
| Event count clock input rise and fall times | t <sub>TR</sub> ,<br>t <sub>TF</sub> | TEX             | Fig. 3  |                          |        | 20   | ms   |

\*1 t<sub>sys</sub> indicates three values according to the contents of the clock control register (CLC; 00FEH) upper 2 bits (CPU clock selection).

t<sub>sys</sub> [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Fig. 1. Clock timing

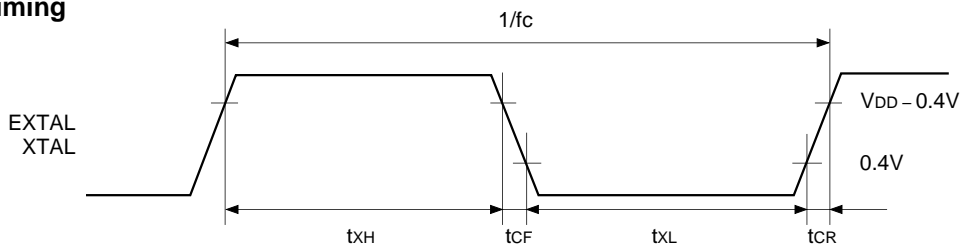


Fig. 2. Clock applied condition

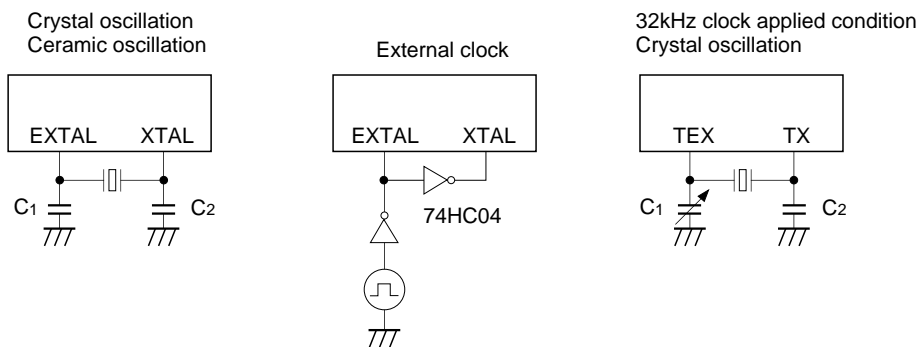
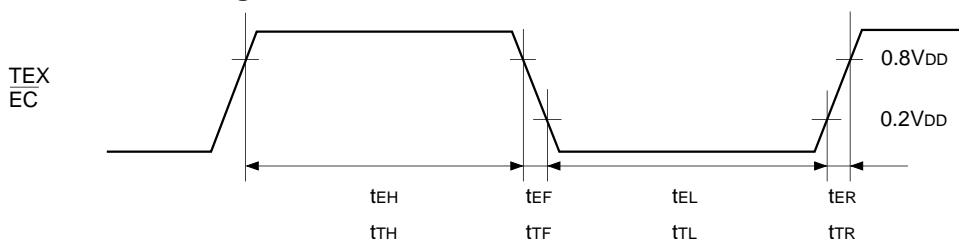


Fig. 3. Event count clock timing



## (2) Serial transfer (CH0)

(Ta = -20 to +75°C, V<sub>DD</sub> = 4.5 to 5.5V, V<sub>SS</sub> = 0V reference)

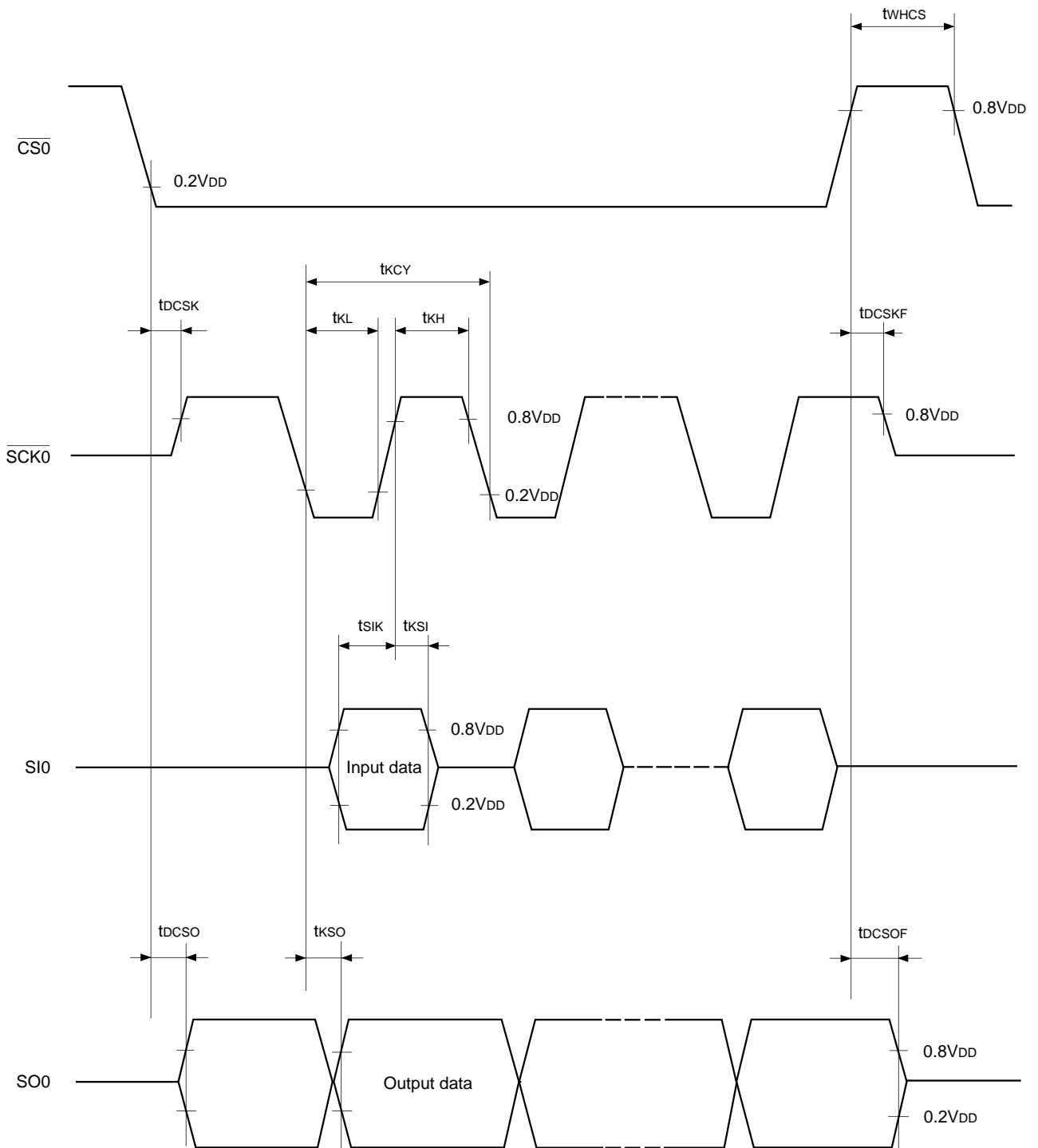
| Item   | Symbol                             | Pin                      | Condition  | Min.                    | Max.                   | Unit |
|--|------------------------------------|--------------------------|--|-------------------------|------------------------|------|
| $\overline{\text{CS0}} \downarrow \rightarrow \overline{\text{SCK0}}$<br>delay time        | t <sub>DCSK</sub>                  | $\overline{\text{SCK0}}$ | Chip select transfer mode<br>( $\overline{\text{SCK0}}$ = output mode) |                         | t <sub>sys</sub> + 200 | ns   |
| $\overline{\text{CS0}} \uparrow \rightarrow \overline{\text{SCK0}}$<br>floating delay time | t <sub>DCSKF</sub>                 | $\overline{\text{SCK0}}$ | Chip select transfer mode<br>( $\overline{\text{SCK0}}$ = output mode) |                         | t <sub>sys</sub> + 200 | ns   |
| $\overline{\text{CS0}} \downarrow \rightarrow \text{SO0}$<br>delay time                    | t <sub>DCSO</sub>                  | SO0                      | Chip select transfer mode  |                         | t <sub>sys</sub> + 200 | ns   |
| $\overline{\text{CS0}} \uparrow \rightarrow \text{SO0}$<br>floating delay time             | t <sub>DCSOF</sub>                 | SO0                      | Chip select transfer mode  |                         | t <sub>sys</sub> + 200 | ns   |
| $\overline{\text{CS0}}$<br>high level width  | t <sub>WHCS</sub>                  | $\overline{\text{CS0}}$  | Chip select transfer mode  | t <sub>sys</sub> + 200  |                        | ns   |
| $\overline{\text{SCK0}}$<br>cycle time   | t <sub>KCY</sub>                   | $\overline{\text{SCK0}}$ | Input mode   | 2t <sub>sys</sub> + 200 |                        | ns   |
|  |                                    |                          | Output mode  | 16000/fc                |                        | ns   |
| $\overline{\text{SCK0}}$<br>high and low level widths                                      | t <sub>KH</sub><br>t <sub>KL</sub> | $\overline{\text{SCK0}}$ | Input mode   | t <sub>sys</sub> + 100  |                        | ns   |
|  |                                    |                          | Output mode  | 8000/fc - 50            |                        | ns   |
| SI0 input set-up time<br>(against $\overline{\text{SCK0}} \uparrow$ )                      | t <sub>SIK</sub>                   | SI0                      | $\overline{\text{SCK0}}$ input mode                                    | 100                     |                        | ns   |
|  |                                    |                          | $\overline{\text{SCK0}}$ output mode                                   | 200                     |                        | ns   |
| SI0 input hold time<br>(against $\overline{\text{SCK0}} \uparrow$ )                        | t <sub>KSI</sub>                   | SI0                      | $\overline{\text{SCK0}}$ input mode                                    | t <sub>sys</sub> + 200  |                        | ns   |
|  |                                    |                          | $\overline{\text{SCK0}}$ output mode                                   | 100                     |                        | ns   |
| $\overline{\text{SCK0}} \downarrow \rightarrow \text{SO0}$ delay time                      | t <sub>KSO</sub>                   | SO0                      | $\overline{\text{SCK0}}$ input mode                                    |                         | t <sub>sys</sub> + 200 | ns   |
|  |                                    |                          | $\overline{\text{SCK0}}$ output mode                                   |                         | 100                    | ns   |

**Note 1)** t<sub>sys</sub> indicates three values according to the contents of the clock control register (CLC; 00FE<sub>H</sub>) upper 2 bits (CPU clock selection).

t<sub>sys</sub> [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

**Note 2)** The load of  $\overline{\text{SCK0}}$  output mode and SO0 output delay time is 50pF + 1TTL.

Fig. 4. Serial transfer timing (CH0)



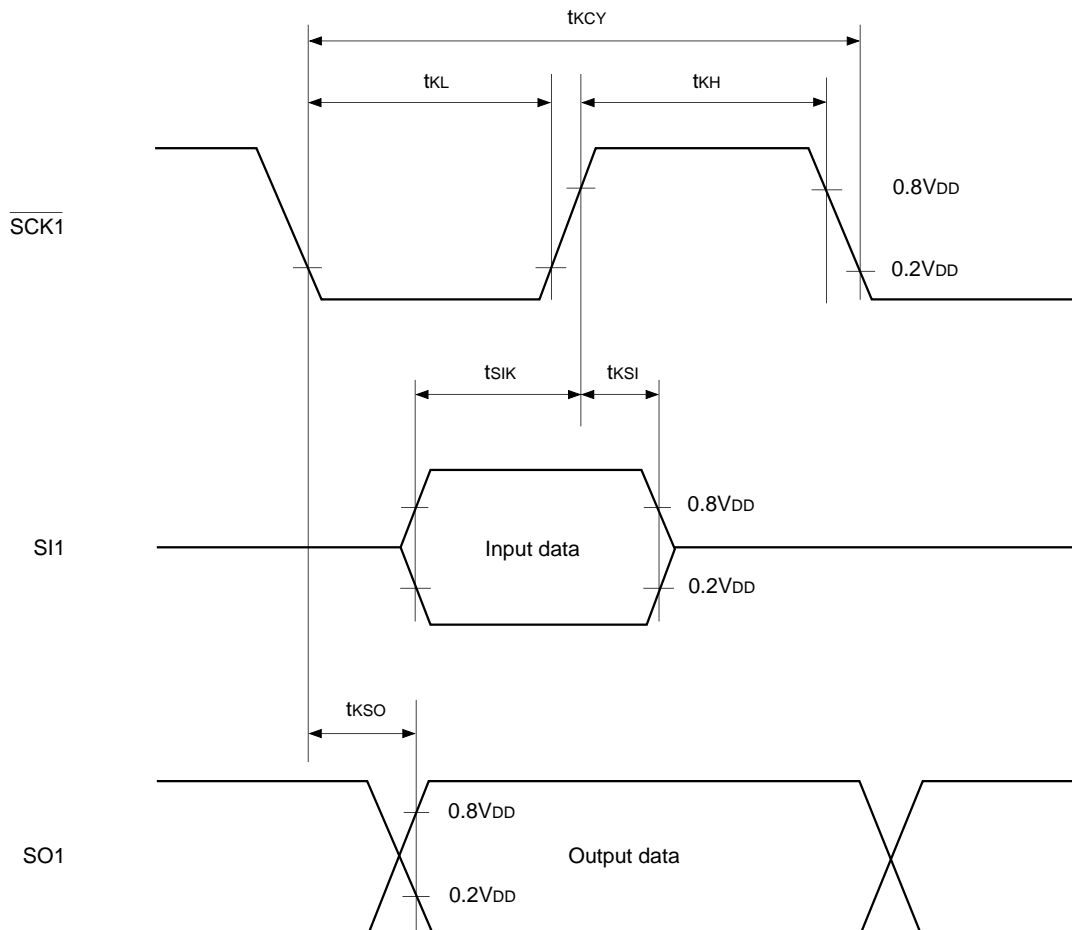
**Serial transfer (CH1)**

( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$  reference)

| Item  | Symbol                             | Pin                      | Condition                            | Min.            | Max. |
|---|------------------------------------|--------------------------|--------------------------------------|-----------------|------|
| $\overline{\text{SCK1}}$ cycle time                                   | $t_{\text{KCY}}$                   | $\overline{\text{SCK1}}$ | Input mode                           | 1000            |      |
|   |                                    |                          | Output mode                          | $16000/f_c$     |      |
| $\overline{\text{SCK1}}$ high and low level widths                    | $t_{\text{KH}}$<br>$t_{\text{KL}}$ | $\overline{\text{SCK1}}$ | Input mode                           | 400             |      |
|   |                                    |                          | Output mode                          | $8000/f_c - 50$ |      |
| SI1 input set-up time (against $\overline{\text{SCK1}} \uparrow$ )    | $t_{\text{SIK}}$                   | SI1                      | $\overline{\text{SCK1}}$ input mode  | 100             |      |
|   |                                    |                          | $\overline{\text{SCK1}}$ output mode | 200             |      |
| SI1 input hold time (against $\overline{\text{SCK1}} \uparrow$ )      | $t_{\text{KSI}}$                   | SI1                      | $\overline{\text{SCK1}}$ input mode  | 200             |      |
|   |                                    |                          | $\overline{\text{SCK1}}$ output mode | 100             |      |
| $\overline{\text{SCK1}} \downarrow \rightarrow \text{SO1}$ delay time | $t_{\text{KSO}}$                   | SO1                      | $\overline{\text{SCK1}}$ input mode  |                 | 200  |
|   |                                    |                          | $\overline{\text{SCK1}}$ output mode |                 | 100  |

**Note)** The load of  $\overline{\text{SCK1}}$  output mode and SO1 output delay time is  $50\text{pF} + 1\text{TTL}$ .

**Fig. 5. Serial transfer timing (CH1)**

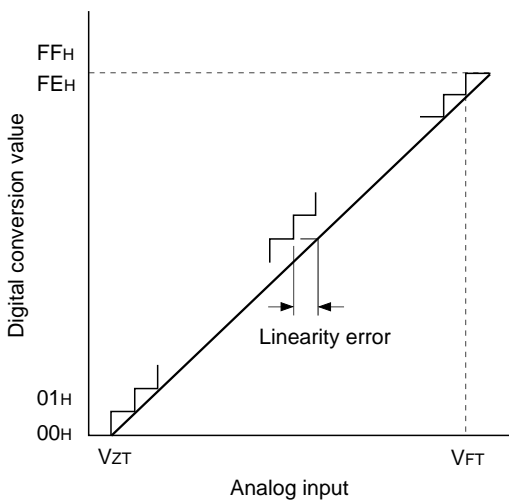


**(3) A/D converter characteristics**

( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = AV_{DD} = 4.5$  to  $5.5\text{V}$ ,  $AV_{REF} = 4.0$  to  $AV_{DD}$ ,  $V_{SS} = AV_{SS} = 0\text{V}$  reference)

| Item                    | Symbol     | Pin            | Condition   | Min.               | Typ. | Max.       | Unit          |
|-------------------------|------------|----------------|---|--------------------|------|------------|---------------|
| Resolution              |            |                |   |                    |      | 8          | Bits          |
| Linearity error         |            |                | $T_a = 25^\circ\text{C}$<br>$V_{DD} = AV_{DD} = AV_{REF} = 5.0\text{V}$ |                    |      | $\pm 1$    | LSB           |
| Absolute error          |            |                | $V_{DD} = AV_{SS} = 0\text{V}$  |                    |      | $\pm 2$    | LSB           |
| Conversion time         | $t_{CONV}$ |                |   | $160/f_{ADC}^{*1}$ |      |            | $\mu\text{s}$ |
| Sampling time           | $t_{SAMP}$ |                |   | $12/f_{ADC}^{*1}$  |      |            | $\mu\text{s}$ |
| Reference input voltage | $V_{REF}$  | $AV_{REF}$     |   | $AV_{DD} - 0.5$    |      | $AV_{DD}$  | V             |
| Analog input voltage    | $V_{IAN}$  | $AN0$ to $AN7$ |   | 0                  |      | $AV_{REF}$ | V             |
| AVREF current           | $I_{REF}$  | $AV_{REF}$     | Operation mode  |                    | 0.6  | 1.0        | mA            |
|                         |            |                | SLEEP mode<br>STOP mode<br>32kHz operation mode                         |                    |      | 10         | $\mu\text{A}$ |

**Fig. 6. Definitions of A/D converter terms**



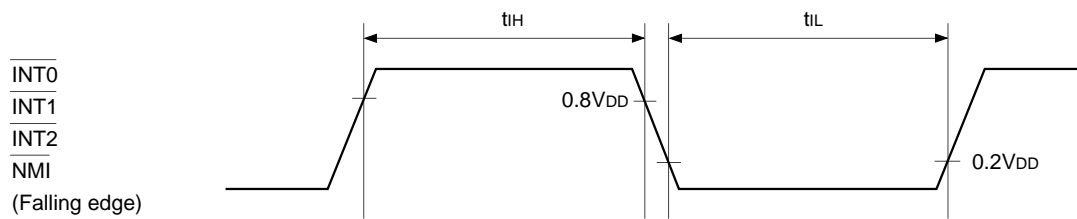
\*1  $f_{ADC}$  indicates the below values due to the contents of bit 0 (ADCCCK) of the ADC operation clock selection register (MSC: 01FFH), bits 7 (PCK1) and 6 (PCK0) of the clock control register (CLC: 00FEH).

| PCK1, PCK0 \ ADCCCK       | 0 ( $\phi/2$ selection)  | 1 ( $\phi$ selection) |
|---------------------------|--------------------------|-----------------------|
|                           | 00 ( $\phi = f_{EX}/2$ ) | $f_{ADC} = f_c/2$     |
| 01 ( $\phi = f_{EX}/4$ )  | $f_{ADC} = f_c/4$        | $f_{ADC} = f_c/2$     |
| 11 ( $\phi = f_{EX}/16$ ) | $f_{ADC} = f_c/16$       | $f_{ADC} = f_c/8$     |

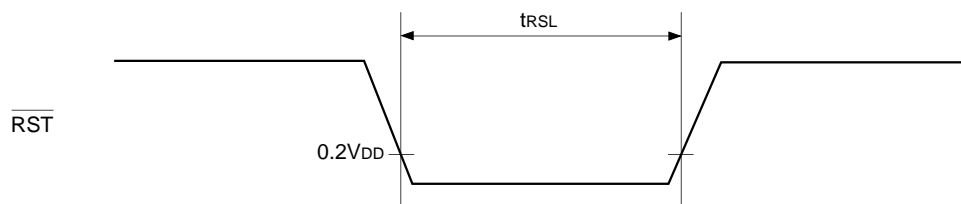
**(4) Interruption, reset input** ( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$  reference)

| Item  | Symbol               | Pin   | Condition | Min.     | Max. | Unit          |
|---|----------------------|---|-----------|----------|------|---------------|
| External interruption high and low level widths | $t_{IH}$<br>$t_{IL}$ | $\overline{\text{INT0}}$<br>$\overline{\text{INT1}}$<br>$\overline{\text{INT2}}$<br>$\overline{\text{NMI}}$ |           | 1        |      | $\mu\text{s}$ |
| Reset input low level width                     | $t_{RSL}$            | $\overline{\text{RST}}$   |           | $32/f_c$ |      | $\mu\text{s}$ |

**Fig. 7. Interruption input timing**



**Fig. 8. Reset input timing**



Analog Circuit Characteristics

(1) Amplifier circuit reference voltage characteristics

( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = \text{AMPV}_{DD} = 5.0\text{V}$ ,  $V_{SS} = \text{AMPV}_{SS} = 0\text{V}$  reference)

| Item                           | Symbol   | Pin     | Conditions                              | Min.  | Typ.  | Max. | Unit |
|--------------------------------|----------|---------|---|-------|-------|------|------|
| Reference level output voltage | $V_{OR}$ | VREFOUT |   | 2.2   | 2.4   | 2.6  | V    |
|                                |          | CTLAG   |   | 2.15  | 2.35  | 2.55 | V    |
| Reference level output current | $I_{OR}$ | VREFOUT | $V_{REFOUT} = V_{REFOUT} + 0.5\text{V}$ | 3.50  | 6.5   |      | mA   |
|                                |          |         | $V_{REFOUT} = V_{REFOUT} - 0.5\text{V}$ | -0.30 | -0.85 |      | mA   |
|                                |          | CTLAG   | $CTLAG = CTLAG + 0.5\text{V}$           | 2.80  | 5.5   |      | mA   |
|                                |          |         | $CTLAG = CTLAG - 0.5\text{V}$           | -0.30 | -0.85 |      | mA   |

(2) CTL 1st amplifier characteristics

( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = \text{AMPV}_{DD} = 5.0\text{V}$ ,  $V_{SS} = \text{AMPV}_{SS} = 0\text{V}$ , CTLAG reference)

| Item  | Symbol       | Pin                      | Conditions  | Min. | Typ. | Max. | Unit       |
|---|--------------|--------------------------|---|------|------|------|------------|
| Voltage gain *1                                   | $A_{VCTL1}$  | RECCTL (+)<br>CTLFAMPO*2 | Gain = 16dB<br>RECCTL (-) = 0V  | 12.5 | 14.5 | 16.5 | dB         |
|   |              |                          | Gain = 27dB<br>RECCTL (-) = 0V  | 23.5 | 25.5 | 27.5 | dB         |
|   |              |                          | Gain = 42dB<br>RECCTL (-) = 0V  | 39.0 | 41.5 | 44.0 | dB         |
|   |              |                          | Gain = 58dB<br>RECCTL (-) = 0V  | 54.5 | 57.0 | 59.5 | dB         |
| Offset voltage                                    | $V_{OSCTL1}$ |                          | CTLAMP (+) and CTLAMP (-)<br>= open                                   | -40  | 0    | +40  | mV         |
| Input resistance                                  | $R_{INCTL1}$ | CTLAMP (+)               | Charge switch OFF<br>CTLAMP (+) = +0.2V                               | 26.0 | 44.5 |      | k $\Omega$ |
|   |              | CTLAMP (-)               | Charge switch OFF<br>CTLAMP (-) = +0.2V                               | 1.20 | 2.0  |      | k $\Omega$ |
| Charge switch ON resistance                       | $R_{CCCTL1}$ | CTLAMP (+)               | Charge switch ON<br>CTLAMP (+) = +0.5V                                |      | 560  | 1010 | $\Omega$   |
|   |              | CTLAMP (-)               | Charge switch ON<br>CTLAMP (-) = +0.5V                                |      | 560  | 1010 | $\Omega$   |
| RECCTL and CTLCIN connection switch ON resistance | $R_{READ}$   | RECCTL (+)<br>CTLCIN (+) | During CTL read operation,<br>CTLCIN (+) - RECCTL (+) = 0.2V          | 315  | 400  | 770  | $\Omega$   |
|   |              | RECCTL (-)<br>CTLCIN (-) | During CTL read operation,<br>CTLCIN (-) - RECCTL (-) = 0.2V          | 315  | 400  | 770  | $\Omega$   |
| CTLCIN 0V fix switch ON resistance                | $R_{WRITE}$  | CTLCIN (+)               | During CTL write operation,<br>CTLCIN (+) = AMPV <sub>SS</sub> + 0.2V |      | 250  | 310  | $\Omega$   |
|   |              | CTLCIN (-)               | During CTL write operation,<br>CTLCIN (-) = AMPV <sub>SS</sub> + 0.2V |      | 250  | 310  | $\Omega$   |

\*1 When CTLCIN (+), CTLAMP (+) pins and CTLCIN (-), CTLAMP (-) pins are AC coupled, and then the signal is input from RECCTL (+) pin.

\*2 The result after measuring output waveform of CTLFAMPO pin or voltage value.

**Note)** The gain increases by approximately 1.5dB when the AC coupling capacitor (47 $\mu\text{F}$ ) is connected to CTLAMP (+) and CTLAMP (-) pins, and the signal is input from CTLAMP (+) and CTLAMP (-) pins.



**(3) CTL 2nd amplifier characteristics**

(Ta = -20 to +75°C, VDD = AMPVDD = 5.0V, VSS = AMPVSS = 0V, CTLAG reference)

| Item                        | Symbol              | Pin                                      | Conditions                               | Min.                                  | Typ. | Max.              | Unit              |
|-----------------------------|---------------------|--|--|---------------------------------------|------|-------------------|-------------------|
| Voltage gain*1, *2          | AVCTL2              | CTLSAMPI                                 | Gain = 5dB                               | 4.8                                   | 5.8  | 6.8               | dB                |
|                             |                     |  | Gain = 11dB                              | 10.4                                  | 11.5 | 12.6              | dB                |
|                             |                     |  | Gain = 16dB                              | 15.3                                  | 16.5 | 17.7              | dB                |
|                             |                     |  | Gain = 20dB                              | 19.3                                  | 20.5 | 21.7              | dB                |
| LPF cut-off frequency*1, *2 | fCCTL               |  | fDC - 3dB                                | 15.0                                  | 25.0 | 40.0              | kHz               |
| Offset voltage*2            | VO_SCTL2            |  | CTLSAMPI = open                          | -50                                   | 0    | +50               | mV                |
| Comparator level*2          | VCCTL               |  | Comparator level = +100mV <sub>0-p</sub> | 70.0                                  | 100  | 130               | mV <sub>0-p</sub> |
|                             |                     |  | Comparator level = +250mV <sub>0-p</sub> | 215                                   | 245  | 275               | mV <sub>0-p</sub> |
|                             |                     |  | Comparator level = +400mV <sub>0-p</sub> | 370                                   | 400  | 430               | mV <sub>0-p</sub> |
|                             |                     |  | Comparator level = -100mV <sub>0-p</sub> | -70.0                                 | -100 | -130              | mV <sub>0-p</sub> |
|                             |                     | Comparator level = -250mV <sub>0-p</sub> | -220                                     | -250                                  | -280 | mV <sub>0-p</sub> |                   |
|                             |                     | Comparator level = -400mV <sub>0-p</sub> | -370                                     | -400                                  | -430 | mV <sub>0-p</sub> |                   |
|                             |                     | Input resistance                         | R <sub>IN</sub> CTL2                     | Charge switch OFF<br>CTLSAMPI = +0.2V | 10.0 | 18.0              |                   |
| Charge switch ON resistance | R <sub>C</sub> CTL2 | Charge switch ON<br>CTLSAMPI = +0.5V     |  | 770                                   | 1140 | Ω                 |                   |

\*1 When the signal is input with the AC coupling capacitor (47μF) connected to CTLSAMPI pin.

\*2 The result after measuring the output waveform of amplifier internal low-pass filter or voltage value.

**(4) CTLAMP characteristics (1st amplifier + 2nd amplifier)**

(Ta = -20 to +75°C, VDD = AMPVDD = 5.0V, VSS = AMPVSS = 0V reference)

| Item                         | Symbol              | Pin        | Conditions  | Min.  | Typ. | Max. | Unit              |
|------------------------------|---------------------|------------|---|-------|------|------|-------------------|
| Voltage gain*1               | AVCTL               | RECCTL (+) | CTL 1st amplifier gain = 16dB<br>CTL 2nd amplifier gain = 20dB<br>RECCTL (-) = 0V   | 31.8  | 35.0 | 38.2 | dB                |
| Input amplitude (peak value) | V <sub>PK</sub> CTL |            | RECCTL (-) = 0V   |       |      | ±300 | mV <sub>0-p</sub> |
| Input sensitivity            | V <sub>S</sub> CTL  |            | CTL 1st amplifier gain = 58dB<br>CTL 2nd amplifier gain = 20dB<br>Comparator level = +400mV <sub>0-p</sub><br>-400mV <sub>0-p</sub> |       | 0.08 | 0.10 | mV <sub>0-p</sub> |
| Input dead band              | V <sub>NS</sub> CTL |            | RECCTL (-) = 0V   | 0.015 | 0.04 |      | mV <sub>0-p</sub> |

\*1 As for other combinations of the amplifier gains, CTL 1st amplifier and CTL 2nd amplifier are added respectively.

**Note)** The result when the signal is input from RECCTL (+) pin with CTL 1st amplifier + CTL 2nd amplifier after performing AC coupling of CTLCIN (+), CTLAMP (+) pins and CTLCIN (-), CTLAMP (-) pins, and CTLFAMPO, CTLSAMPI pins.

## (5) CFGAMP characteristics

(Ta = -20 to +75°C, V<sub>DD</sub> = AMPV<sub>DD</sub> = 5.0V, V<sub>SS</sub> = AMPV<sub>DD</sub> = 0V, VREFOUT reference)

| Item                               | Symbol             | Pins                             | Conditions                                 | Min. | Typ. | Max.             | Unit  |
|------------------------------------|--------------------|----------------------------------|--|------|------|------------------|-------|
| Voltage gain*1, *2                 | A <sub>VCFG</sub>  | CFG                              | Gain = 0dB                                 | -0.3 | 0.6  | 2.2              | dB    |
|                                    |                    |                                  | Gain = 20dB                                | 19.2 | 20.8 | 22.4             | dB    |
|                                    |                    |                                  | Gain = 34dB                                | 33.2 | 34.8 | 36.4             | dB    |
|                                    |                    |                                  | Gain = 38dB                                | 37.0 | 38.7 | 40.4             | dB    |
| LPF cut-off frequency*1, *2        | f <sub>CCFG</sub>  |                                  | f <sub>dc</sub> - 3dB                      | 30.0 | 55.0 | 80.0             | kHz   |
| Offset voltage*2                   | V <sub>OFCFG</sub> |                                  | CFG = open                                 | -50  | 0    | +50              | mV    |
| Comparator judgment level width*2  | V <sub>CCFG</sub>  |                                  | Comparator schmitt width = 320mVp-p        | 260  | 320  | 360              | mVp-p |
|                                    |                    |                                  | Comparator schmitt width = 160mVp-p        | 110  | 155  | 200              | mVp-p |
| Input sensitivity*1                | V <sub>SCFG</sub>  |                                  | Gain = 38dB<br>Comparator level = 320mVp-p |      | 4.20 | 5.00             | mVp-p |
|                                    |                    |                                  | Gain = 38dB<br>Comparator level = 160mVp-p |      | 2.10 | 2.40             | mVp-p |
| Input dead band*1                  | V <sub>NSCFG</sub> |                                  | Gain = 38dB<br>Comparator level = 320mVp-p | 3.40 | 4.10 |                  | mVp-p |
|                                    |                    |                                  | Gain = 38dB<br>Comparator level = 160mVp-p | 1.50 | 2.00 |                  | mVp-p |
| Input resistance                   | R <sub>INCFG</sub> | Charge switch OFF<br>CFG = +0.2V | 5.5  | 8.3  |      | kΩ               |       |
| Charge switch ON resistance        | R <sub>CCFG</sub>  | Charge switch ON<br>CFG = +0.5V  |  | 455  | 710  | Ω                |       |
| Digital output waveform duty*1, *3 | D <sub>TYCFG</sub> | CFG = sine wave with 50% duty    | 48.0                                       | 50.0 | 52.0 | %                |       |
| Input amplitude (peak value)*1     | V <sub>PKCFG</sub> |                                  |  |      | ±2.4 | V <sub>0-p</sub> |       |

\*1 When the signal is input with the AC coupling capacitor (47μF) connected to CFG pin.

\*2 The result after measuring the output waveform of amplifier internal low-pass filter or voltage value.

\*3 The result after measuring the digital signal waveform output from the amplifier circuit.

## (6) DFGAMP characteristics

(Ta = -20 to +75°C, V<sub>DD</sub> = AMPV<sub>DD</sub> = 5.0V, V<sub>SS</sub> = AMPV<sub>SS</sub> = 0V, VREFOUT reference)

| Item  | Symbol             | Pins                             | Conditions                                 | Min. | Typ. | Max.             | Unit  |
|---|--------------------|----------------------------------|--|------|------|------------------|-------|
| Voltage gain* <sup>1</sup> , * <sup>2</sup>                 | A <sub>VDFG</sub>  | DFG                              | Gain = 0dB                                 | -0.3 | 0.6  | 2.2              | dB    |
|   |                    |                                  | Gain = 20dB                                | 19.2 | 20.8 | 22.4             | dB    |
|   |                    |                                  | Gain = 34dB                                | 33.2 | 34.8 | 36.4             | dB    |
|   |                    |                                  | Gain = 38dB                                | 37.0 | 38.7 | 40.4             | dB    |
| LPF cut-off frequency* <sup>1</sup> , * <sup>2</sup>        | f <sub>CDFG</sub>  |                                  | f <sub>DC</sub> - 3dB                      | 30.0 | 55.0 | 80.0             | kHz   |
| Offset voltage* <sup>2</sup>                                | V <sub>OSDFG</sub> |                                  | DFG = open                                 | -50  | 0    | +50              | mV    |
| Comparator judgment level width* <sup>2</sup>               | V <sub>CDFG</sub>  |                                  | Comparator schmitt width = 320mVp-p        | 260  | 320  | 360              | mVp-p |
|   |                    |                                  | Comparator schmitt width = 160mVp-p        | 110  | 155  | 200              | mVp-p |
| Input sensitivity* <sup>1</sup>                             | V <sub>SDFG</sub>  |                                  | Gain = 38dB<br>Comparator level = 320mVp-p |      | 4.20 | 5.00             | mVp-p |
|   |                    |                                  | Gain = 38dB<br>Comparator level = 160mVp-p |      | 2.10 | 2.40             | mVp-p |
| Input dead band* <sup>1</sup>                               | V <sub>NSDFG</sub> |                                  | Gain = 38dB<br>Comparator level = 320mVp-p | 3.40 | 4.10 |                  | mVp-p |
|   |                    |                                  | Gain = 38dB<br>Comparator level = 160mVp-p | 1.50 | 2.00 |                  | mVp-p |
| Input resistance  | R <sub>INDFG</sub> | Charge switch OFF<br>DFG = +0.2V | 5.5  | 8.3  |      | kΩ               |       |
| Charge switch ON resistance                                 | R <sub>CDFG</sub>  | Charge switch ON<br>DFG = +0.5V  |  | 455  | 710  | Ω                |       |
| Digital output waveform duty* <sup>1</sup> , * <sup>3</sup> | D <sub>TYDFG</sub> | CFG = sine wave of 50% duty      | 48.0                                       | 50.0 | 52.0 | %                |       |
| Input amplitude (peak value)* <sup>1</sup>                  | V <sub>PKDFG</sub> |                                  |  |      | ±2.4 | V <sub>o-p</sub> |       |

\*<sup>1</sup> When the signal is input with the AC coupling capacitor (47μF) connected to DFG pin.\*<sup>2</sup> The result after measuring the output waveform of amplifier internal low-pass filter or voltage value.\*<sup>3</sup> The result after measuring the digital signal waveform output from the amplifier circuit.

**(7) DPGAMP characteristics**

(Ta = -20 to +75°C, VDD = AMPVDD = 5.0V, VSS = AMPVSS = 0V, VREFOUT reference)

| Item   | Symbol | Pins | Conditions   | Min.  | Typ.   | Max. | Unit              |
|--|--------|------|--|-------|--|------|-------------------|
| Voltage gain*1, *2   | AVDPG  | DPG  |  | 11.1  | 12.0   | 13.2 | dB                |
| LPF cut-off frequency*1, *2                                      | fCDPG  |      | fDC - 3dB  | 30.0  | 55.0   | 85.0 | kHz               |
| Offset voltage*2   | VOSDPG |      | DFG = open   | -35   | 0  | +35  | mV                |
| Comparator level*2   | VCDPG  |      | Comparator level = 600mV <sub>0-p</sub>                          | 570   | 605  | 640  | mV <sub>0-p</sub> |
|  |        |      | Comparator level = 400mV <sub>0-p</sub>                          | 370   | 400  | 432  | mV <sub>0-p</sub> |
|  |        |      | Comparator level = 200mV <sub>0-p</sub>                          | 175   | 200  | 220  | mV <sub>0-p</sub> |
|  |        |      | Comparator level = 100mV <sub>0-p</sub>                          | 72    | 100  | 125  | mV <sub>0-p</sub> |
|  |        |      | Comparator level = -600mV <sub>0-p</sub>                         | -572  | -605   | -643 | mV <sub>0-p</sub> |
|  |        |      | Comparator level = -400mV <sub>0-p</sub>                         | -368  | -400   | -438 | mV <sub>0-p</sub> |
|  |        |      | Comparator level = -200mV <sub>0-p</sub>                         | -174  | -200   | -223 | mV <sub>0-p</sub> |
|  |        |      | Comparator level = -100mV <sub>0-p</sub>                         | -71   | -100   | -124 | mV <sub>0-p</sub> |
|  |        |      | Input sensitivity*1  | VSDPG | Comparator level = 600mV <sub>0-p</sub> , 200mV <sub>0-p</sub> |      | 150               |
| Comparator level = 400mV <sub>0-p</sub> , 100mV <sub>0-p</sub>   |        |      |  |       | 100  | 120  | mV <sub>0-p</sub> |
| Comparator level = -600mV <sub>0-p</sub> , -200mV <sub>0-p</sub> |        |      |  |       | -155   | -185 | mV <sub>0-p</sub> |
| Comparator level = -400mV <sub>0-p</sub> , -100mV <sub>0-p</sub> |        |      |  |       | -109   | -130 | mV <sub>0-p</sub> |
| Input dead band*1  | VNSDPG |      | Comparator level = 600mV <sub>0-p</sub> , 200mV <sub>0-p</sub>   | 113   | 142  |      | mV <sub>0-p</sub> |
|  |        |      | Comparator level = 400mV <sub>0-p</sub> , 100mV <sub>0-p</sub>   | 70    | 90   |      | mV <sub>0-p</sub> |
|  |        |      | Comparator level = -600mV <sub>0-p</sub> , -200mV <sub>0-p</sub> | -120  | -150   |      | mV <sub>0-p</sub> |
|  |        |      | Comparator level = -400mV <sub>0-p</sub> , -100mV <sub>0-p</sub> | -80   | -103   |      | mV <sub>0-p</sub> |
| Input resistance   | RINDPG |      | Charge switch OFF<br>DPG = +0.2V                                 | 24.0  | 44.5   |      | kΩ                |
| Charge switch ON resistance                                      | RCDPG  |      | Charge switch ON<br>DPG = +0.5V                                  |       | 450  | 860  | Ω                 |
| Input amplitude (peak value)*1                                   | VPKDPG |      |  |       | ±2.4   | V    |                   |

\*1 When the signal is input with the AC coupling capacitor (47μF) connected to DPG pin.

\*2 The result after measuring the output waveform of amplifier internal low-pass filter or voltage value.

**(8) CTL write circuit characteristics**(Ta = -20 to +75°C, V<sub>DD</sub> = AMPV<sub>DD</sub> = 5.0V, V<sub>SS</sub> = AMPV<sub>SS</sub> = 0V reference)

| Item                  | Symbol            | Pins                     | Conditions                         | Min. | Typ. | Max. | Unit |
|-----------------------|-------------------|--------------------------|------------------------------------|------|------|------|------|
| Output resistance     | R <sub>OH</sub>   | RECCAP                   | RECCAP = AMPV <sub>DD</sub> - 0.5V | 450  | 625  | 1005 | Ω    |
|                       | R <sub>OL</sub>   |                          | RECCAP = AMPV <sub>DD</sub> + 0.5V | 410  | 555  | 840  | Ω    |
| Output current*1      | I <sub>OREC</sub> | RECCTL (+)<br>RECCTL (-) | Write current = 2.0mA              | 1.3  | 2.0  | 2.9  | mA   |
|                       |                   |                          | Write current = 2.5mA              | 1.7  | 2.5  | 3.7  | mA   |
|                       |                   |                          | Write current = 3.0mA              | 2.1  | 3.1  | 4.5  | mA   |
|                       |                   |                          | Write current = 3.5mA              | 2.6  | 3.6  | 5.2  | mA   |
|                       |                   |                          | Write current = 4.0mA              | 2.9  | 4.0  | 5.9  | mA   |
|                       |                   |                          | Write current = 4.5mA              | 3.3  | 4.6  | 6.6  | mA   |
|                       |                   |                          | Write current = 5.0mA              | 3.7  | 5.1  | 7.2  | mA   |
|                       |                   |                          | Write current = 5.5mA              | 4.0  | 5.6  | 8.0  | mA   |
| Write current = 6.0mA | 4.4               | 6.1                      | 8.9                                | mA   |      |      |      |

\*1 The current value which flows when RECCTL (+) pin and RECCTL (-) pin are shorted.

**(9) Amplifier operating current characteristics**(Ta = -20 to +75°C, V<sub>DD</sub> = AMPV<sub>DD</sub> = 5.0V, V<sub>SS</sub> = AMPV<sub>SS</sub> = 0V reference)

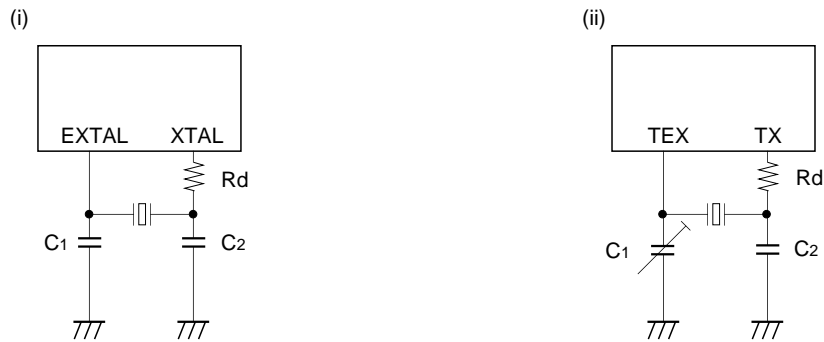
| Item                        | Symbol           | Pins               | Conditions                          | Min. | Typ. | Max. | Unit |
|-----------------------------|------------------|--------------------|-------------------------------------|------|------|------|------|
| Amplifier operating current | I <sub>AMP</sub> | AMPV <sub>DD</sub> | When the amplifier is operating*1   |      | 7.6  | 12.0 | mA   |
|                             |                  |                    | When the amplifier is not operating |      |      | 10   | μA   |

\*1 The CTL recording current is added during CTL write.

**Note)** The amplifier operation and NOT-operation is controlled according to the contents of amplifier power supply control register (ASWC: 05E2H) bits 5, 4, 1 and 0.

Supplement

Fig. 9. Recommended oscillation circuit



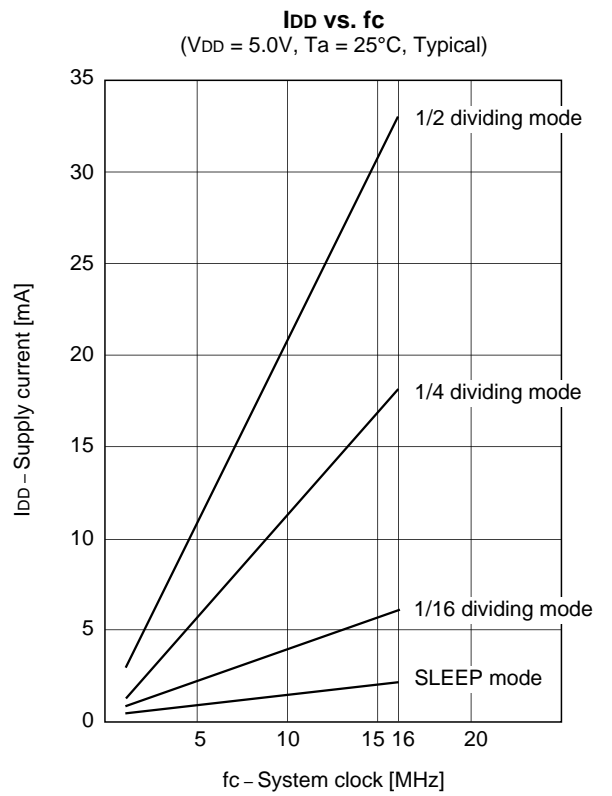
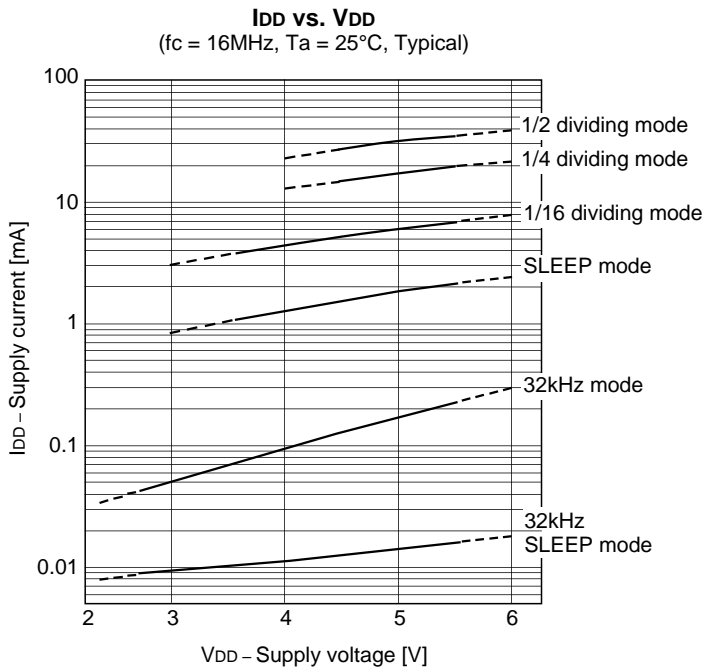
| Manufacturer           | Model        | fc (MHz)  | C1 (pF) | C2 (pF) | Rd ( $\Omega$ ) | Circuit example |
|------------------------|--------------|-----------|---------|---------|-----------------|-----------------|
| RIVER ELETEC CO., LTD. | HC-49/U03    | 8.00      | 10      | 10      | 0               | (i)             |
|                        |              | 10.00     | 5       | 5       |                 |                 |
|                        |              | 12.00     |         |         |                 |                 |
|                        |              | 16.00     |         |         |                 |                 |
| KINSEKI LTD.           | HC-49/U (-S) | 8.00      | 16 (12) | 16 (12) | 0               | (i)             |
|                        |              | 10.00     | 16 (12) | 16 (12) |                 |                 |
|                        |              | 12.00     | 12      | 12      |                 |                 |
|                        |              | 16.00     | 12      | 12      |                 |                 |
|                        | P3           | 32.768kHz | 30      | 18      | 470k            | (ii)            |

Mask option table

| Item                   | Content                    |              |
|------------------------|----------------------------|--------------|
|                        | Reset pin pull-up resistor | Non-existent |
| Input circuit format*1 | CMOS schmitt               | TTL schmitt  |

\*1 The input circuit format can be selected for PE3/SYNC pin.

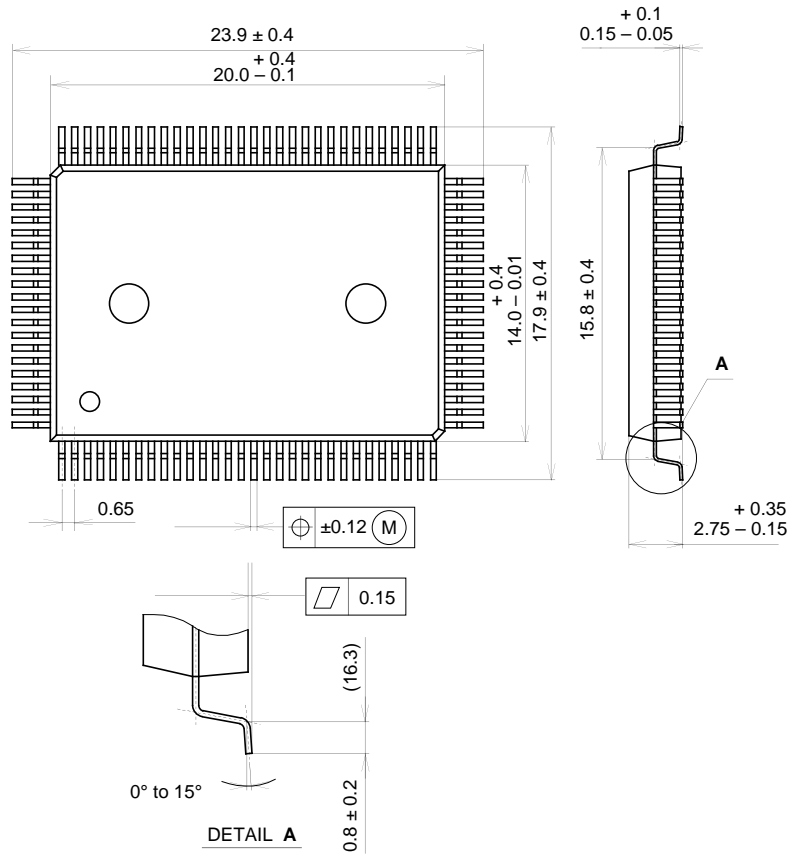
Characteristics Curve



Package Outline

Unit: mm

100PIN QFP (PLASTIC)



PACKAGE STRUCTURE

|            |                  |
|------------|------------------|
| SONY CODE  | QFP-100P-L01     |
| EIAJ CODE  | *QFP100-P-1420-A |
| JEDEC CODE | _____            |

|                  |                   |
|------------------|-------------------|
| PACKAGE MATERIAL | EPOXY RESIN       |
| LEAD TREATMENT   | SOLDER PLATING    |
| LEAD MATERIAL    | COPPER / 42 ALLOY |
| PACKAGE WEIGHT   | 1.4g              |