

# 1-Mbit (1M x 1) Static RAM

## Features

- Pin- and function-compatible with CY7C107B/CY7C1007B
- High speed
  - $t_{AA} = 10 \text{ ns}$
- Low Active Power
  - $I_{CC} = 80 \text{ mA @ } 10 \text{ ns}$
- Low CMOS Standby Power
  - $I_{SB2} = 3 \text{ mA}$
- 2.0V Data Retention
- Automatic power-down when deselected
- CMOS for optimum speed/power
- TTL-compatible inputs and outputs
- CY7C107D available in Pb-free 28-pin 400-Mil wide Molded SOJ package. CY7C1007D available in Pb-free 28-pin 300-Mil wide Molded SOJ package

## Functional Description <sup>[1]</sup>

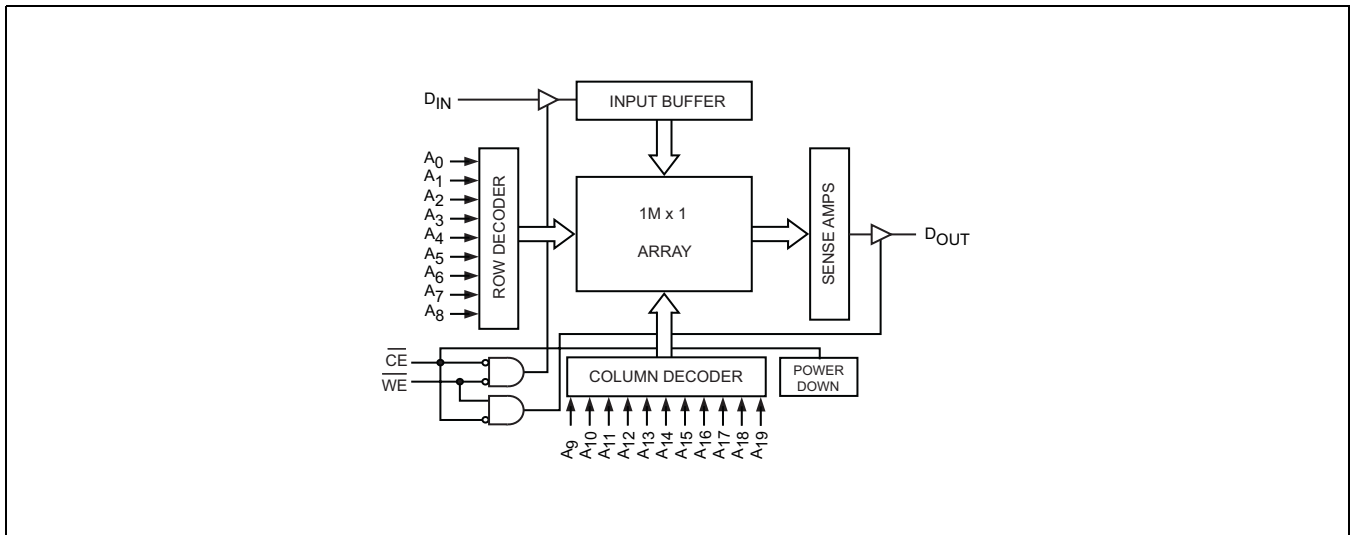
The CY7C107D and CY7C1007D are high-performance CMOS static RAMs organized as 1,048,576 words by 1 bit. Easy memory expansion is provided by an active LOW Chip Enable ( $\overline{CE}$ ) and tri-state drivers. These devices have an automatic power-down feature that reduces power consumption by more than 65% when deselected. The output pin ( $D_{OUT}$ ) is placed in a high-impedance state when:

- Deselected ( $\overline{CE}$  HIGH)
- When the write operation is active ( $\overline{CE}$  and  $\overline{WE}$  LOW)

Write to the device by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. Data on the input pin ( $D_{IN}$ ) is written into the memory location specified on the address pins ( $A_0$  through  $A_{19}$ ).

Read from the device by taking Chip Enable ( $\overline{CE}$ ) LOW while forcing Write Enable ( $\overline{WE}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins appears on the data output ( $D_{OUT}$ ) pin.

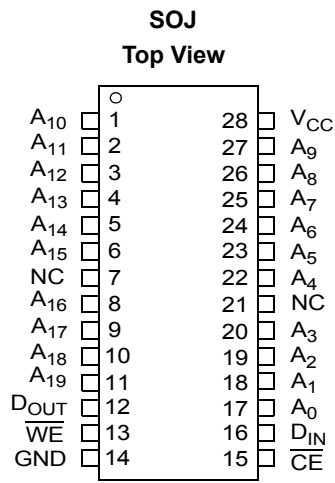
## Logic Block Diagram



### Note

1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at [www.cypress.com](http://www.cypress.com).

**Pin Configuration [2]**



**Selection Guide**

	<b>CY7C107D-10</b> <b>CY7C1007D-10</b>	<b>Unit</b>
Maximum Access Time	10	ns
Maximum Operating Current	80	mA
Maximum CMOS Standby Current, I <sub>SB2</sub>	3	mA

**Note**

2. NC pins are not connected on the die.

### Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied..... -55°C to +125°C

Supply Voltage on V<sub>CC</sub> Relative to GND [3] .... -0.5V to +6.0V

DC Voltage Applied to Outputs in High-Z State [3] ..... -0.5V to V<sub>CC</sub> + 0.5V

DC Input Voltage [3] ..... -0.5V to V<sub>CC</sub> + 0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current ..... > 200 mA

### Operating Range

Range	Ambient Temperature	V <sub>CC</sub>	Speed
Industrial	-40°C to +85°C	5V ± 0.5V	10 ns

### Electrical Characteristics (Over the Operating Range)

Parameter	Description	Test Conditions	7C107D-10 7C1007D-10		Unit
			Min	Max	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -4.0 mA	2.4		V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 8.0 mA		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.5	V
V <sub>IL</sub>	Input LOW Voltage [3]		-0.5	0.8	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1	+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	-1	+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max, I <sub>OUT</sub> = 0 mA, f = f <sub>max</sub> = 1/t <sub>RC</sub>	100 MHz	80	mA
			83 MHz	72	mA
			66 MHz	58	mA
			40 MHz	37	mA
I <sub>SB1</sub>	Automatic $\overline{CE}$ Power-down Current— TTL Inputs	Max V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>max</sub>		10	mA
I <sub>SB2</sub>	Automatic $\overline{CE}$ Power-down Current— CMOS Inputs	Max V <sub>CC</sub> , $\overline{CE} \geq V_{CC} - 0.3V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V, f = 0		3	mA

**Note**

3. V<sub>IL</sub>(min) = -2.0V and V<sub>IH</sub>(max) = V<sub>CC</sub> + 1V for pulse durations of less than 5 ns.

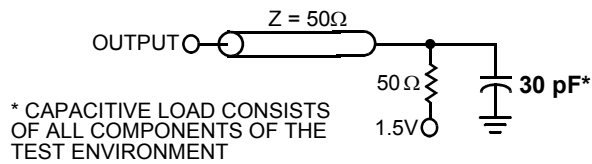
### Capacitance [4]

Parameter	Description	Test Conditions	Max	Unit
$C_{IN}$ : Addresses	Input Capacitance	$T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = 5.0\text{V}$	7	pF
$C_{IN}$ : Controls			10	pF
$C_{OUT}$	Output Capacitance		10	pF

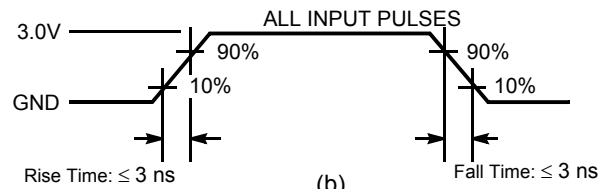
### Thermal Resistance [4]

Parameter	Description	Test Conditions	300-Mil Wide SOJ	400-Mil Wide SOJ	Unit
$\Theta_{JA}$	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	59.16	58.76	$^\circ\text{C/W}$
$\Theta_{JC}$	Thermal Resistance (Junction to Case)		40.84	40.54	$^\circ\text{C/W}$

### AC Test Loads and Waveforms [5]

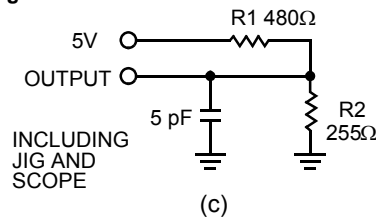


(a)



(b)

#### High-Z characteristics:



(c)

#### Notes

4. Tested initially and after any design or process changes that may affect these parameters.
5. AC characteristics (except High-Z) are tested using the load conditions shown in Figure (a). High-Z characteristics are tested for all speeds using the test load shown in Figure (c).

**Switching Characteristics** (Over the Operating Range) <sup>[6]</sup>

Parameter	Description	7C107D-10 7C1007D-10		Unit
		Min	Max	
<b>Read Cycle</b>				
$t_{power}^{[7]}$	$V_{CC}$ (typical) to the first access	100		$\mu$ s
$t_{RC}$	Read Cycle Time	10		ns
$t_{AA}$	Address to Data Valid		10	ns
$t_{OHA}$	Data Hold from Address Change	3		ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid		10	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low Z <sup>[8]</sup>	3		ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High Z <sup>[8, 9]</sup>		5	ns
$t_{PU}^{[10]}$	$\overline{CE}$ LOW to Power-Up	0		ns
$t_{PD}^{[10]}$	$\overline{CE}$ HIGH to Power-Down		10	ns
<b>Write Cycle</b> <sup>[11]</sup>				
$t_{WC}$	Write Cycle Time	10		ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	7		ns
$t_{AW}$	Address Set-Up to Write End	7		ns
$t_{HA}$	Address Hold from Write End	0		ns
$t_{SA}$	Address Set-Up to Write Start	0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	7		ns
$t_{SD}$	Data Set-Up to Write End	6		ns
$t_{HD}$	Data Hold from Write End	0		ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[8]</sup>	3		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[8, 9]</sup>		6	ns

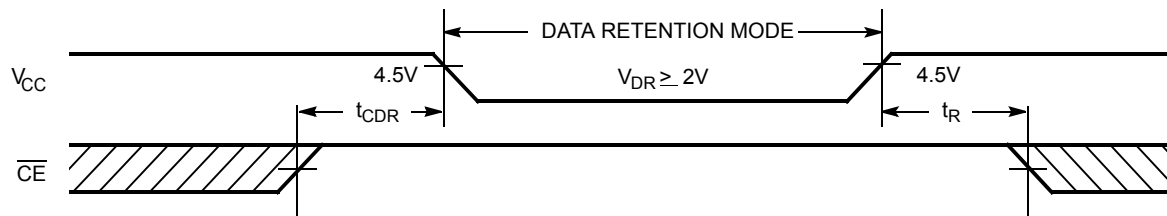
**Notes**

6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
7.  $t_{POWER}$  gives the minimum amount of time that the power supply should be at typical  $V_{CC}$  values until the first memory access can be performed.
8. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$  and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
9.  $t_{HZCE}$  and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (c) of "AC Test Loads and Waveforms [5]" on page 4. Transition is measured when the outputs enter a high impedance state.
10. This parameter is guaranteed by design and is not tested.
11. The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW.  $\overline{CE}$  and  $\overline{WE}$  must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

**Data Retention Characteristics** (Over the Operating Range)

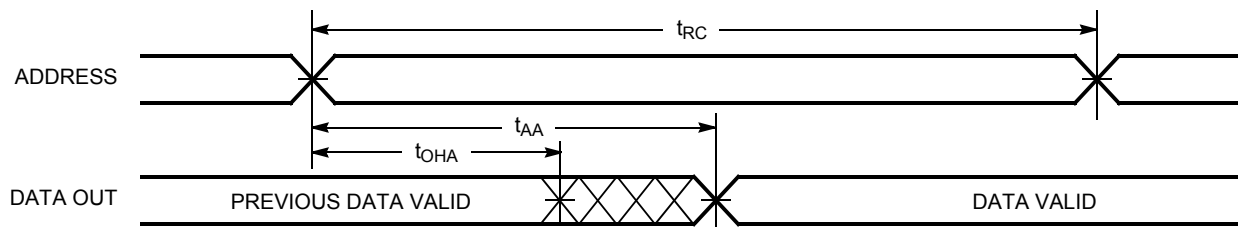
Parameter	Description	Conditions	Min	Max	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		2.0		V
$I_{CCDR}$	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$ , $\overline{CE} \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		3	mA
$t_{CDR}^{[5]}$	Chip Deselect to Data Retention Time		0		ns
$t_R^{[12]}$	Operation Recovery Time		$t_{RC}$		ns

**Data Retention Waveform**

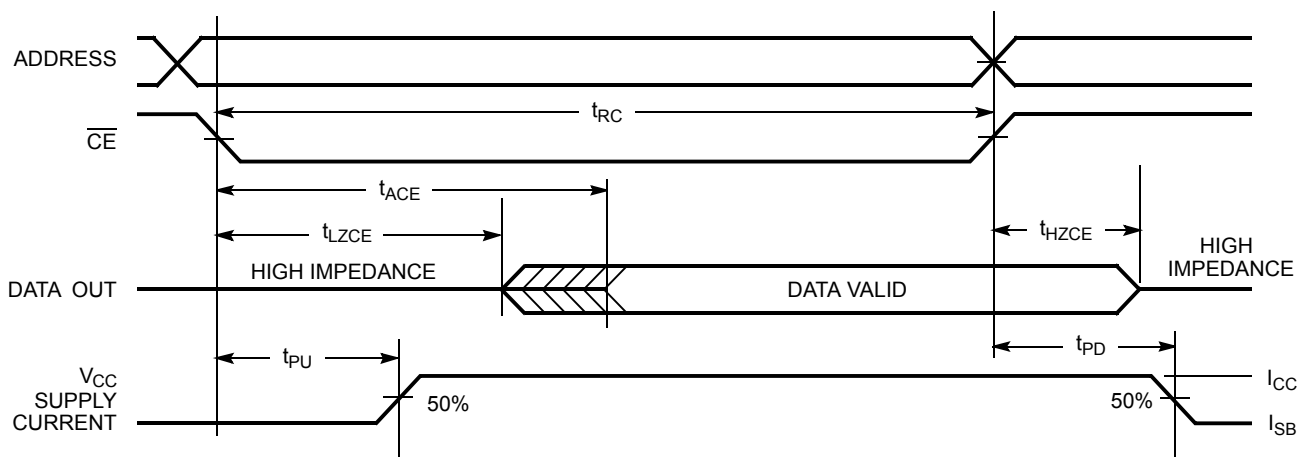


**Switching Waveforms**

**Read Cycle No. 1** (Address Transition Controlled) [13, 14]



**Read Cycle No. 2** [14, 15]

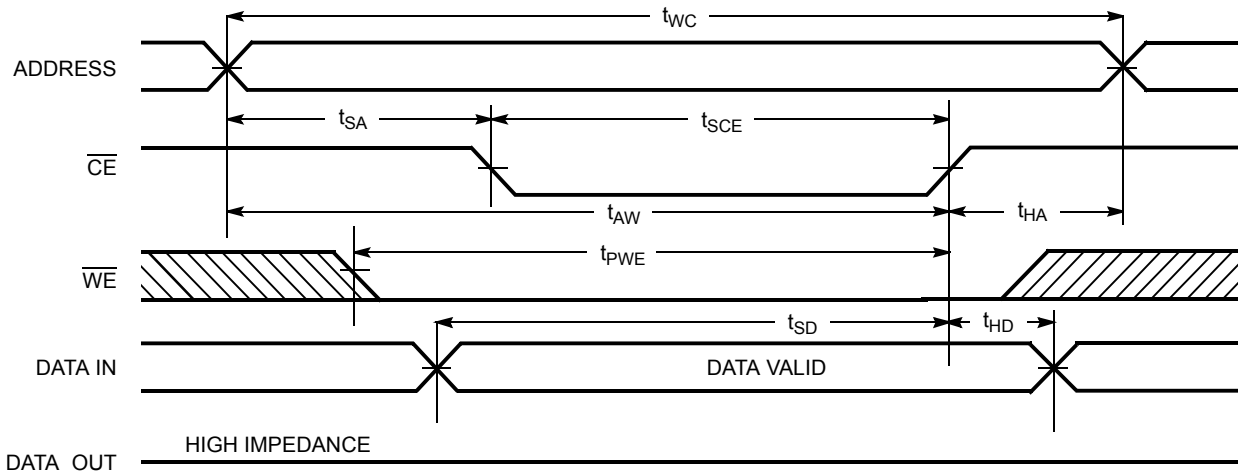


**Notes**

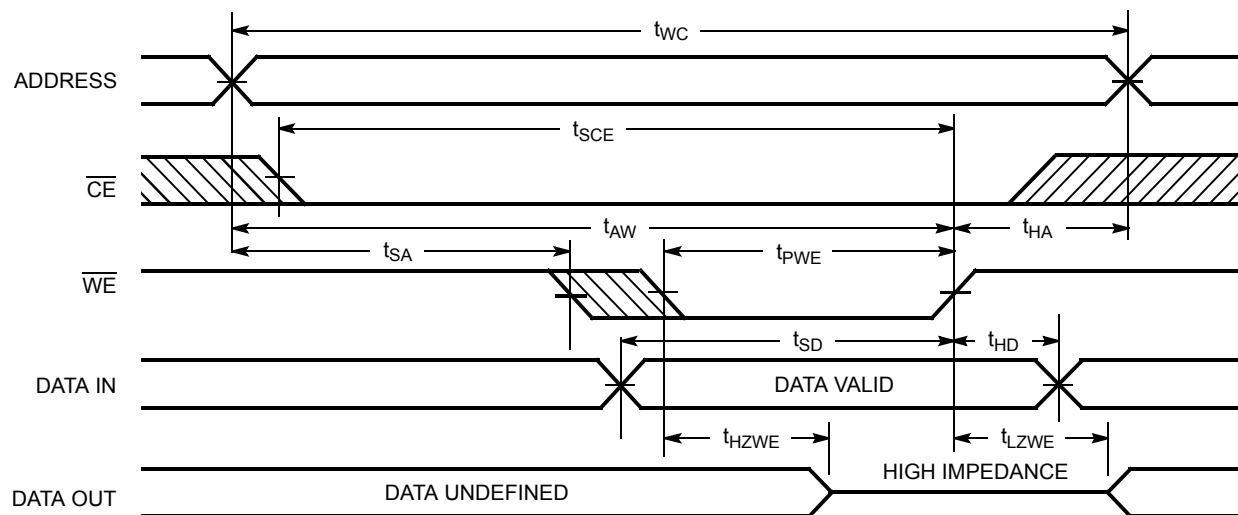
- 12. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \geq 50 \mu s$  or stable at  $V_{CC(min)} \geq 50 \mu s$ .
- 13. Device is continuously selected,  $\overline{CE} = V_{IL}$ .
- 14.  $\overline{WE}$  is HIGH for read cycle.
- 15. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

**Switching Waveforms**(continued)

**Write Cycle No. 1 ( $\overline{CE}$  Controlled)** [16]



**Write Cycle No. 2 ( $\overline{WE}$  Controlled)** [16]



**Truth Table**

$\overline{CE}$	$\overline{WE}$	$D_{OUT}$	Mode	Power
H	X	High Z	Power-Down	Standby ( $I_{SB}$ )
L	H	Data Out	Read	Active ( $I_{CC}$ )
L	L	High Z	Write	Active ( $I_{CC}$ )

**Note**  
16. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.

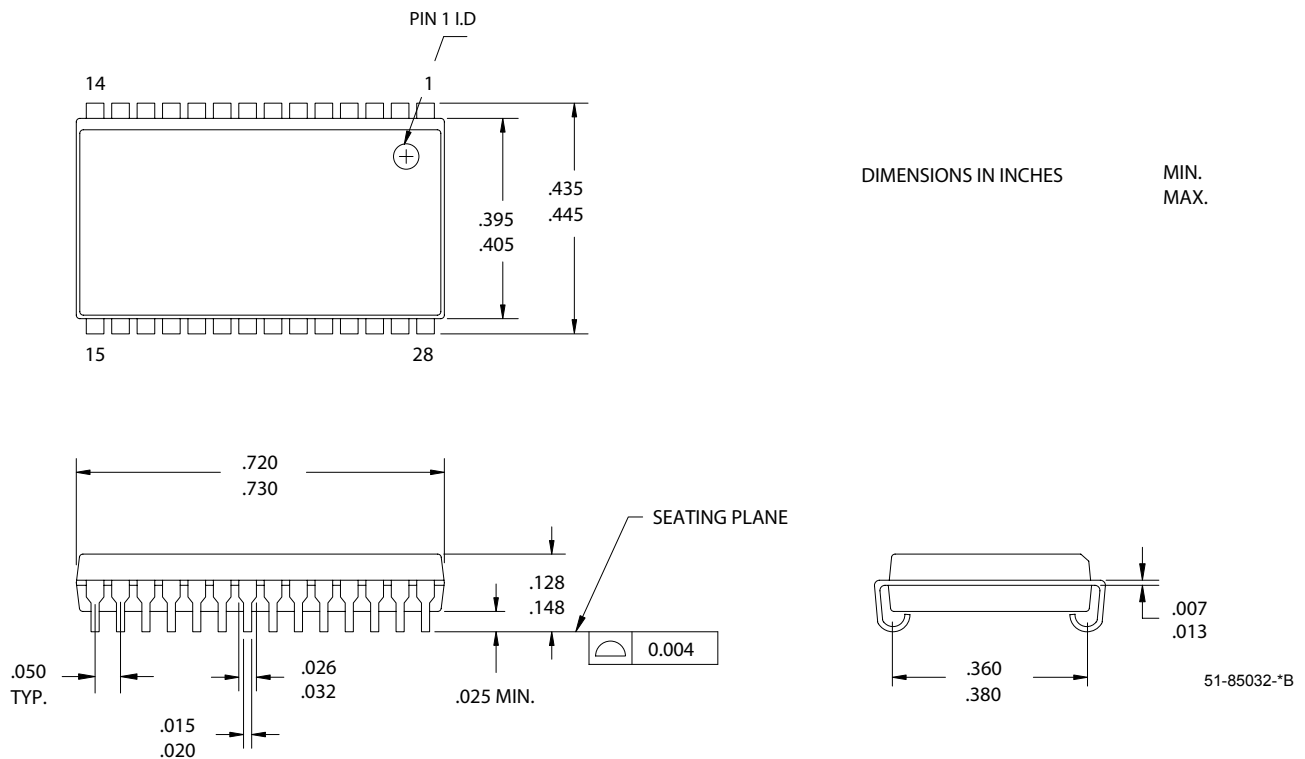
**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C107D-10VXI	51-85032	28-pin (400-Mil) Molded SOJ (Pb-free)	Industrial
	CY7C1007D-10VXI	51-85031	28-pin (300-Mil) Molded SOJ (Pb-free)	

Please contact your local Cypress sales representative for availability of these parts.

**Package Diagrams**

**Figure 1. 28-pin (400-Mil) Molded SOJ, 51-85032**







**Document History Page**

Document Title: CY7C107D/CY7C1007D, 1-Mbit (1M x 1) Static RAM				
Document Number: 38-05469				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	201560	See ECN	SWI	Advance Information data sheet for C9 IPP
*A	233722	See ECN	RKF	DC parameters modified as per EROS (Spec # 01-02165) Pb-free offering in Ordering Information
*B	263769	See ECN	RKF	Added Data Retention Characteristics table Added T <sub>power</sub> Spec in Switching Characteristics Table Shaded Ordering Information
*C	307601	See ECN	RKF	Reduced Speed bins to -10 and -12 ns
*D	560995	See ECN	VKN	Converted from Preliminary to Final Removed Commercial Operating range Removed 12 ns speed bin Added I <sub>CC</sub> values for the frequencies 83MHz, 66MHz and 40MHz Updated Thermal Resistance table Updated Ordering Information Table Changed Overshoot spec from V <sub>CC</sub> +2V to V <sub>CC</sub> +1V in footnote #3
*E	802877	See ECN	VKN	Changed I <sub>CC</sub> specs from 60 mA to 80 mA for 100MHz, 55 mA to 72 mA for 83MHz, 45 mA to 58 mA for 66MHz, 30 mA to 37 mA for 40MHz