



# 128K x 8 Static RAM

## Features

- **High speed**  
—  $t_{AA} = 10 \text{ ns}$
- **Low active power**  
— 1017 mW (max., 12 ns)
- **Low CMOS standby power**  
— 55 mW (max.), 4 mW (Low power version)
- **2.0V Data Retention (Low power version)**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with  $\overline{CE}_1$ ,  $CE_2$ , and  $\overline{OE}$  options**

## Functional Description

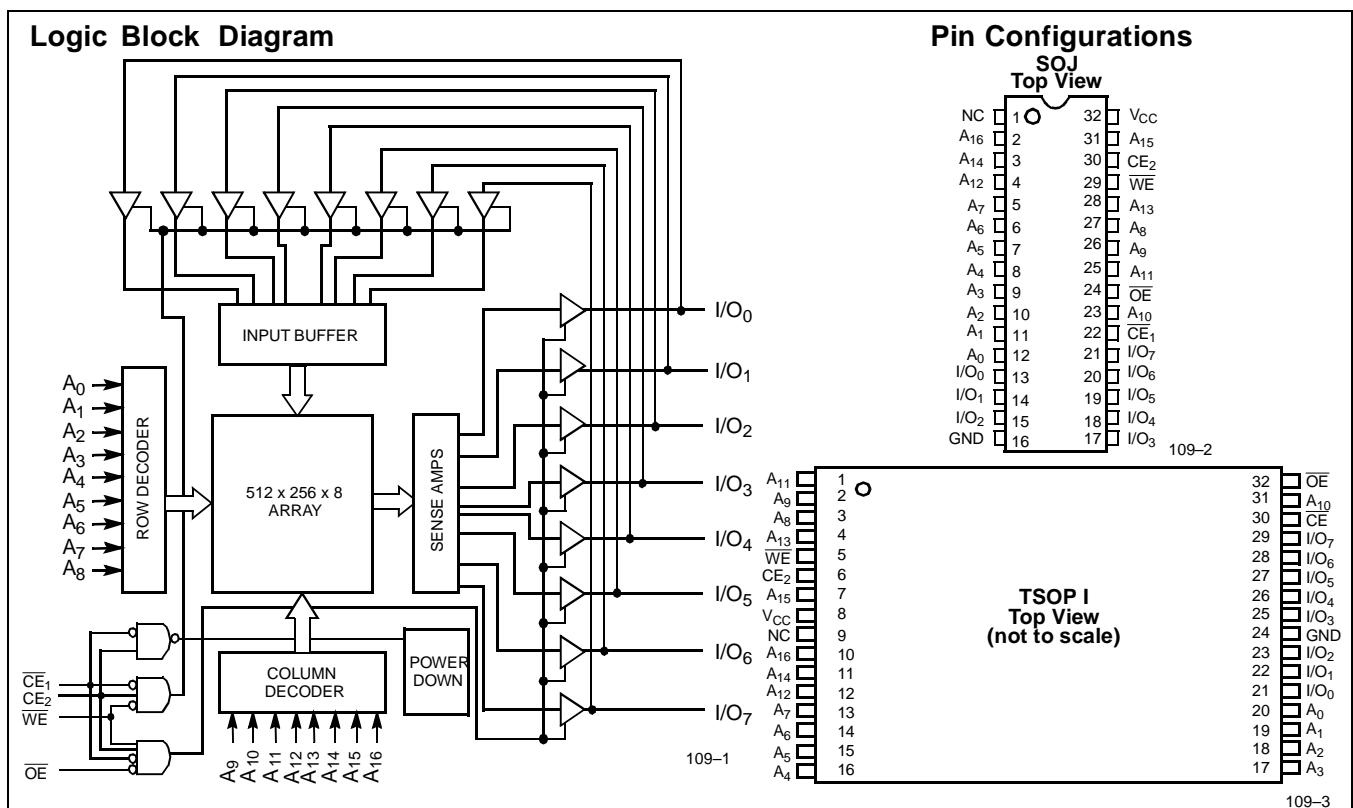
The CY7C109 / CY7C1009 is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ( $\overline{CE}_1$ ), an

active HIGH chip enable ( $CE_2$ ), an active LOW output enable ( $\overline{OE}$ ), and three-state drivers. Writing to the device is accomplished by taking chip enable one ( $\overline{CE}_1$ ) and write enable ( $\overline{WE}$ ) inputs LOW and chip enable two ( $CE_2$ ) input HIGH. Data on the eight I/O pins ( $I/O_0$  through  $I/O_7$ ) is then written into the location specified on the address pins ( $A_0$  through  $A_{16}$ ).

Reading from the device is accomplished by taking chip enable one ( $\overline{CE}_1$ ) and output enable ( $\overline{OE}$ ) LOW while forcing write enable ( $\overline{WE}$ ) and chip enable two ( $CE_2$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins ( $I/O_0$  through  $I/O_7$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW), the outputs are disabled ( $\overline{OE}$  HIGH), or during a write operation ( $\overline{CE}_1$  LOW,  $CE_2$  HIGH, and  $\overline{WE}$  LOW).

The CY7C109 is available in standard 400-mil-wide SOJ and 32-pin TSOP type I packages. The CY7C1009 is available in a 300-mil-wide SOJ package. The CY7C1009 and CY7C109 are functionally equivalent in all other respects.



## Selection Guide

	7C109-10 7C1009-10	7C109-12 7C1009-12	7C109-15 7C1009-15	7C109-20 7C1009-20	7C109-25 7C1009-25	7C109-35 7C1009-35
Maximum Access Time (ns)	10	12	15	20	25	35
Maximum Operating Current (mA)	195	185	155	140	135	125
Maximum CMOS Standby Current (mA)	10	10	10	10	10	10
Maximum CMOS Standby Current (mA) Low Power Version	2	2	2	—	—	—

Shaded areas contain preliminary information.



**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with Power Applied ..... -55°C to +125°C  
 Supply Voltage on V<sub>CC</sub> to Relative GND<sup>[1]</sup> ..... -0.5V to +7.0V  
 DC Voltage Applied to Outputs in High Z State<sup>[1]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V  
 DC Input Voltage<sup>[1]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V  
 Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

**Operating Range**

Range	Ambient Temperature <sup>[2]</sup>	V <sub>CC</sub>
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%

**Electrical Characteristics** Over the Operating Range<sup>[3]</sup>

Parameter	Description	Test Conditions	7C109-10 7C1009-10		7C109-12 7C1009-12		7C109-15 7C1009-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.3	2.2	V <sub>CC</sub> + 0.3	2.2	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage <sup>[1]</sup>		-0.3	0.8	-0.3	0.8	-0.3	0.8	V
I <sub>Ix</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1	+1	-1	+1	-1	+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	-5	+5	-5	+5	-5	+5	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[3]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND		-300		-300		-300	mA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>		195		185		155	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current —TTL Inputs	Max. V <sub>CC</sub> , $\overline{CE}_1 \geq V_{IH}$ or CE <sub>2</sub> ≤ V <sub>IL</sub> , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		45		45		40	mA
I <sub>SB2</sub>	Automatic CE Power-Down Current —CMOS Inputs	Max. V <sub>CC</sub> , CE <sub>1</sub> ≥ V <sub>CC</sub> - 0.3V, or CE <sub>2</sub> ≤ 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V, or V <sub>IN</sub> ≤ 0.3V, f=0		10		10		10	mA
			L	2		2		2	

Shaded areas contain preliminary information.

**Electrical Characteristics** Over the Operating Range (continued)

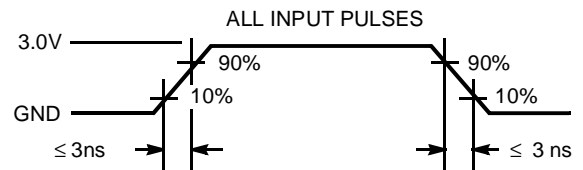
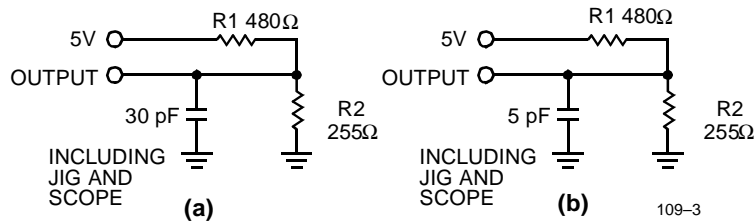
Parameter	Description	Test Conditions	7C109-20 7C1009-20		7C109-25 7C1009-25		7C109-35 7C1009-35		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}$ , $I_{OH} = -4.0 \text{ mA}$	2.4		2.4		2.4		V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}$ , $I_{OL} = 8.0 \text{ mA}$		0.4		0.4		0.4	V
$V_{IH}$	Input HIGH Voltage		2.2	$V_{CC} + 0.3$	2.2	$V_{CC} + 0.3$	2.2	$V_{CC} + 0.3$	V
$V_{IL}$	Input LOW Voltage <sup>[1]</sup>		-0.3	0.8	-0.3	0.8	-0.3	0.8	V
$I_{IX}$	Input Load Current	$GND \leq V_I \leq V_{CC}$	-1	+1	-1	+1	-1	+1	$\mu\text{A}$
$I_{OZ}$	Output Leakage Current	$GND \leq V_I \leq V_{CC}$ , Output Disabled	-5	+5	-5	+5	-5	+5	$\mu\text{A}$
$I_{OS}$	Output Short Circuit Current <sup>[3]</sup>	$V_{CC} = \text{Max.}$ , $V_{OUT} = GND$		-300		-300		-300	mA
$I_{CC}$	$V_{CC}$ Operating Supply Current	$V_{CC} = \text{Max.}$ , $I_{OUT} = 0 \text{ mA}$ , $f = f_{MAX} = 1/t_{RC}$		140		135		125	mA
$I_{SB1}$	Automatic CE Power-Down Current —TTL Inputs	Max. $V_{CC}$ , $CE_1 \geq V_{IH}$ or $CE_2 \leq V_{IL}$ , $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{MAX}$		30		30		25	mA
$I_{SB2}$	Automatic CE Power-Down Current —CMOS Inputs	Max. $V_{CC}$ , $CE_1 \geq V_{CC} - 0.3\text{V}$ , or $CE_2 \leq 0.3\text{V}$ , $V_{IN} \geq V_{CC} - 0.3\text{V}$ , or $V_{IN} \leq 0.3\text{V}$ , $f=0$		10		10		10	mA

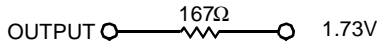
**Capacitance<sup>[4]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ\text{C}$ , $f = 1 \text{ MHz}$ , $V_{CC} = 5.0\text{V}$	9	pF
$C_{OUT}$	Output Capacitance		8	pF

**Notes:**

- $V_{IL}(\text{min.}) = -2.0\text{V}$  for pulse durations of less than 20 ns.
- $T_A$  is the "instant on" case temperature.
- Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.

**AC Test Loads and Waveforms**


Equivalent to: THÉVENIN EQUIVALENT  

 1.73V

**Switching Characteristics**<sup>[3, 5]</sup> Over the Operating Range

Parameter	Description	7C109-10 7C1009-10		7C109-12 7C1009-12		7C109-15 7C1009-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>								
t <sub>RC</sub>	Read Cycle Time	10		12		15		ns
t <sub>AA</sub>	Address to Data Valid		10		12		15	ns
t <sub>OHA</sub>	Data Hold from Address Change	3		3		3		ns
t <sub>ACE</sub>	$\overline{CE}_1$ LOW to Data Valid, CE <sub>2</sub> HIGH to Data Valid		10		12		15	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		5		6		7	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[6, 7]</sup>		5		6		7	ns
t <sub>LZCE</sub>	$\overline{CE}_1$ LOW to Low Z, CE <sub>2</sub> HIGH to Low Z <sup>[7]</sup>	3		3		3		ns
t <sub>HZCE</sub>	$\overline{CE}_1$ HIGH to High Z, CE <sub>2</sub> LOW to High Z <sup>[6, 7]</sup>		5		6		7	ns
t <sub>PU</sub>	$\overline{CE}_1$ LOW to Power-Up, CE <sub>2</sub> HIGH to Power-Up	0		0		0		ns
t <sub>PD</sub>	$\overline{CE}_1$ HIGH to Power-Down, CE <sub>2</sub> LOW to Power-Down		10		12		15	ns
<b>WRITE CYCLE</b> <sup>[8, 9]</sup>								
t <sub>WC</sub>	Write Cycle Time	10		12		15		ns
t <sub>SCE</sub>	$\overline{CE}_1$ LOW to Write End, CE <sub>2</sub> HIGH to Write End	8		10		12		ns
t <sub>AW</sub>	Address Set-Up to Write End	8		10		12		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	8		10		12		ns
t <sub>SD</sub>	Data Set-Up to Write End	6		7		8		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		0		ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[7]</sup>	3		3		3		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[6, 7]</sup>		5		6		7	ns

Shaded areas contain preliminary information.

**Notes:**

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30-pF load capacitance.
- t<sub>HZOE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
- At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}_1$  LOW, CE<sub>2</sub> HIGH, and  $\overline{WE}$  LOW.  $\overline{CE}_1$  and  $\overline{WE}$  must be LOW and CE<sub>2</sub> HIGH to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle no. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of t<sub>HZWE</sub> and T<sub>SD</sub>.

**Switching Characteristics**<sup>[3, 5]</sup> Over the Operating Range

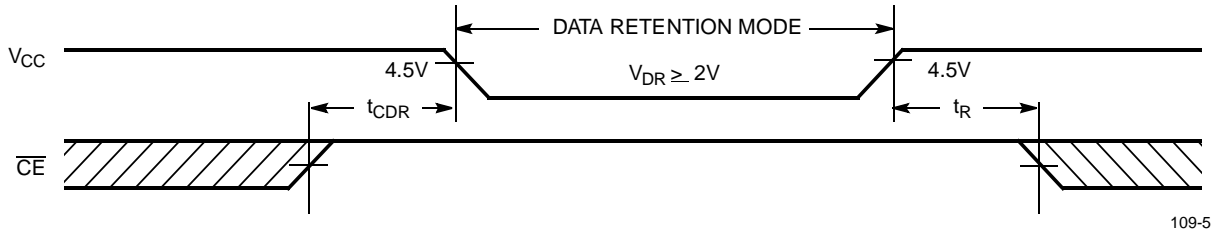
Parameter	Description	7C109-20 7C1009-20		7C109-25 7C1009-25		7C109-35 7C1009-35		Unit
		Min.	Max.	Min.	Max.	Min.	Min.	
<b>READ CYCLE</b>								
t <sub>RC</sub>	Read Cycle Time	20		25		35		ns
t <sub>AA</sub>	Address to Data Valid		20		25		35	ns
t <sub>OHA</sub>	Data Hold from Address Change	3		5		5		ns
t <sub>ACE</sub>	$\overline{CE}_1$ LOW to Data Valid, CE <sub>2</sub> HIGH to Data Valid		20		25		35	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		8		10		15	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[6, 7]</sup>		8		10		15	ns
t <sub>LZCE</sub>	$\overline{CE}_1$ LOW to Low Z, CE <sub>2</sub> HIGH to Low Z <sup>[7]</sup>	3		5		5		ns
t <sub>HZCE</sub>	$\overline{CE}_1$ HIGH to High Z, CE <sub>2</sub> LOW to High Z <sup>[6, 7]</sup>		8		10		15	ns
t <sub>PU</sub>	$\overline{CE}_1$ LOW to Power-Up, CE <sub>2</sub> HIGH to Power-Up	0		0		0		ns
t <sub>PD</sub>	$\overline{CE}_1$ HIGH to Power-Down, CE <sub>2</sub> LOW to Power-Down		20		25		35	ns
<b>WRITE CYCLE</b> <sup>[8]</sup>								
t <sub>WC</sub>	Write Cycle Time	20		25		35		ns
t <sub>SCE</sub>	$\overline{CE}_1$ LOW to Write End, CE <sub>2</sub> HIGH to Write End	15		20		25		ns
t <sub>AW</sub>	Address Set-Up to Write End	15		20		25		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	12		15		20		ns
t <sub>SD</sub>	Data Set-Up to Write End	10		15		20		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		0		ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[7]</sup>	3		5		5		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[6, 7]</sup>		8		10		15	ns

**Data Retention Characteristics** Over the Operating Range (L Version Only)

Parameter	Description	Conditions	Min.	Max	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention	No input may exceed V <sub>CC</sub> + 0.5V V <sub>CC</sub> = V <sub>DR</sub> = 2.0V, $\overline{CE}_1 \geq V_{CC} - 0.3V$ or CE <sub>2</sub> ≤ 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V	2.0		V
I <sub>CCDR</sub>	Data Retention Current			50	μA
t <sub>CDR</sub>	Chip Deselect to Data Retention Time		0		ns
t <sub>R</sub>	Operation Recovery Time		t <sub>RC</sub>		ns

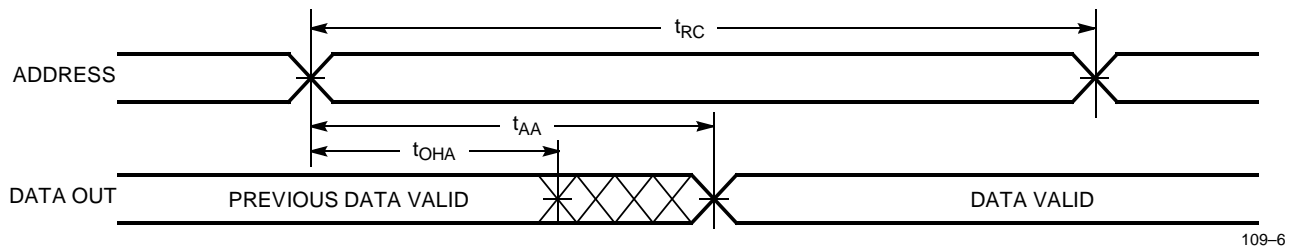
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**Data Retention Waveform**

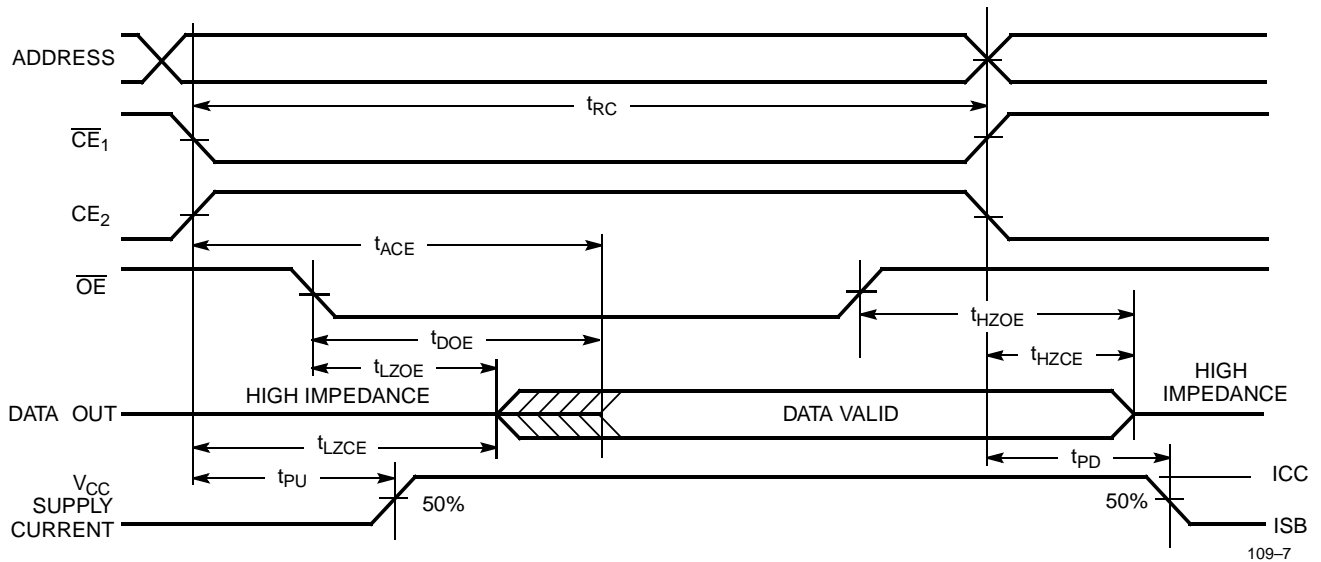


**Switching Waveforms**

**Read Cycle No. 1<sup>[10, 11]</sup>**



**Read Cycle No. 2 ( $\overline{OE}$  Controlled)<sup>[11, 12]</sup>**

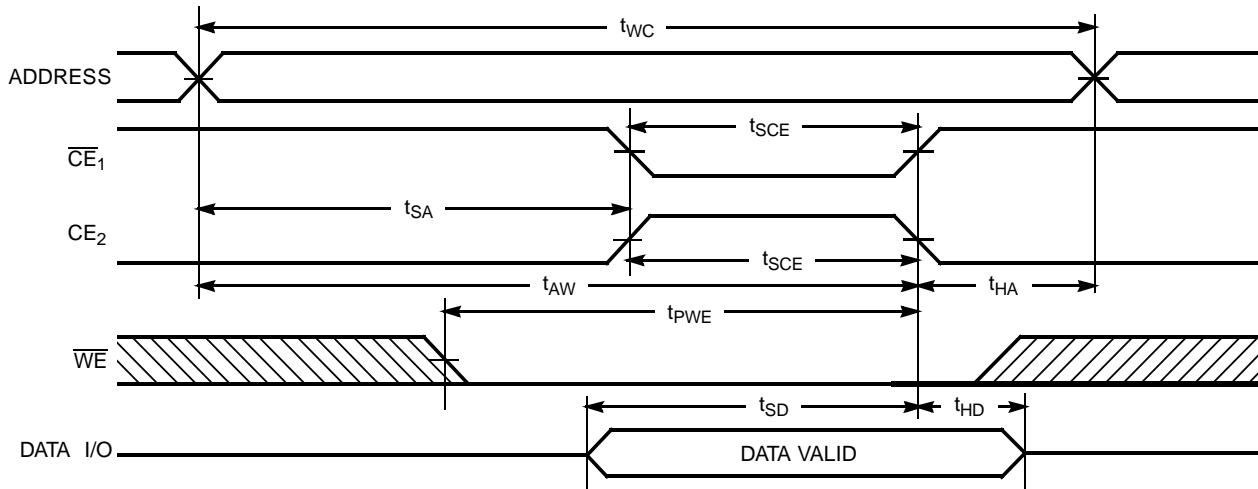


**Notes:**

- 10. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $CE_2 = V_{IH}$ .
- 11.  $\overline{WE}$  is HIGH for read cycle.
- 12. Address valid prior to or coincident with  $\overline{CE}_1$  transition LOW and  $CE_2$  transition HIGH.

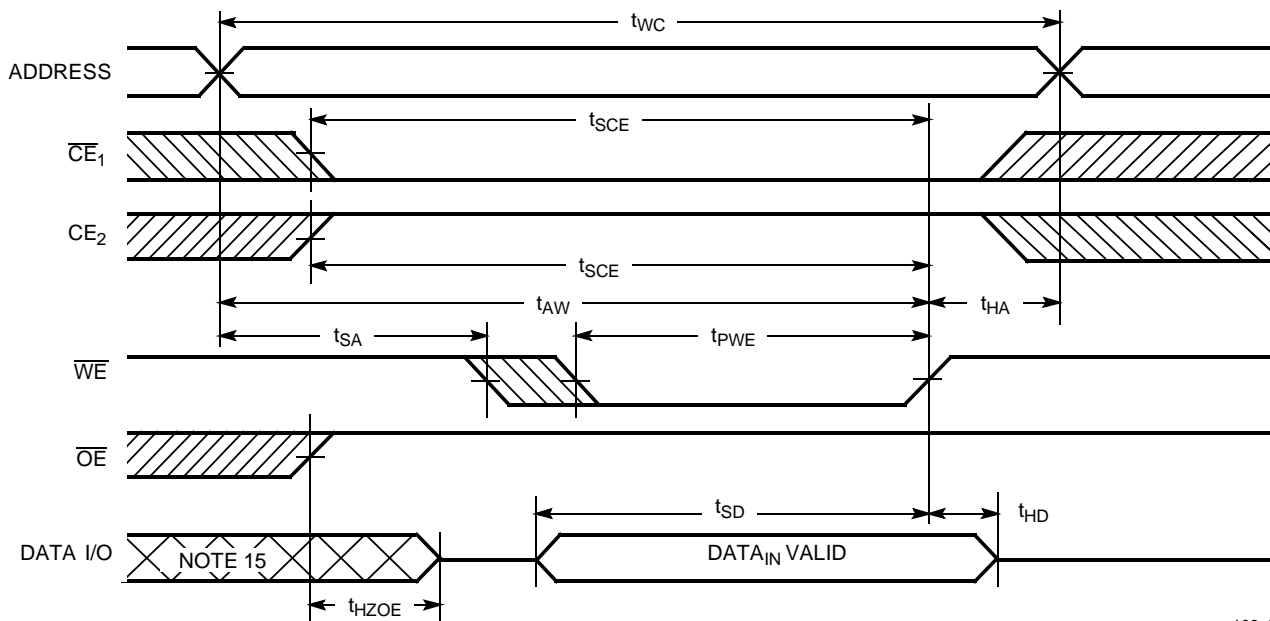
**Switching Waveforms (continued)**

**Write Cycle No. 1 ( $\overline{CE}_1$  or  $CE_2$  Controlled)<sup>[13, 14]</sup>**



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**Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  HIGH During Write)<sup>[13, 14]</sup>**

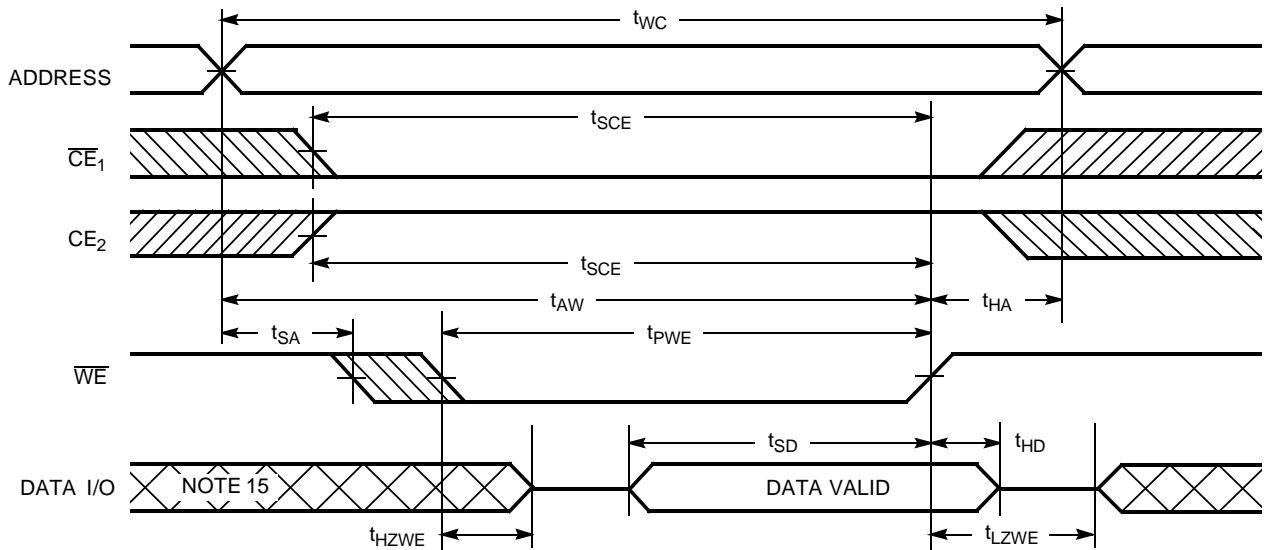


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**Notes:**

- 13. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
- 14. If  $\overline{CE}_1$  goes HIGH or  $CE_2$  goes LOW simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.

**Switching Waveforms** (continued)

**Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[14]</sup>**


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**Note:**

15. During this period the I/Os are in the output state and input signals should not be applied.

**Truth Table**

$\overline{CE}_1$	$CE_2$	OE	WE	I/O <sub>0</sub> - I/O <sub>7</sub>	Mode	Power
H	X	X	X	High Z	Power-Down	Standby ( $I_{SB}$ )
X	L	X	X	High Z	Power-Down	Standby ( $I_{SB}$ )
L	H	L	H	Data Out	Read	Active ( $I_{CC}$ )
L	H	X	L	Data In	Write	Active ( $I_{CC}$ )
L	H	H	H	High Z	Selected, Outputs Disabled	Active ( $I_{CC}$ )



**Ordering Information**

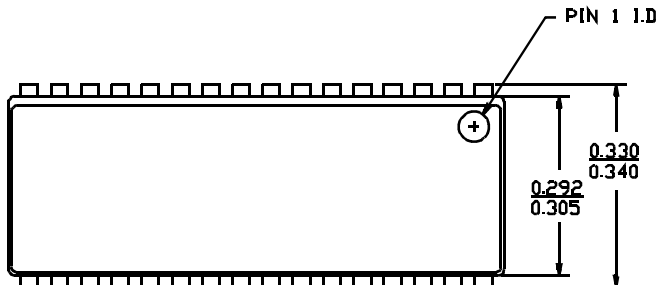
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C109-10VC	V33	32-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1009-10VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C1009L-10VC	V32	32-Lead (300-Mil) Molded SOJ	
12	CY7C109-12VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C1009-12VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C1009L-12VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C109-12ZC	Z32	32-Lead TSOP Type I	
15	CY7C109-15VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C1009-15VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C1009L-15VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C109-15ZC	Z32	32-Lead TSOP Type I	
20	CY7C109-20VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C1009-20VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C109-20VI	V33	32-Lead (400-Mil) Molded SOJ	Commercial
	CY7C109-20ZC	Z32	32-Lead TSOP Type I	Industrial
	CY7C109-20ZI	Z32	32-Lead TSOP Type I	Commercial
25	CY7C109-25VC	V33	32-Lead (400-Mil) Molded SOJ	Industrial
	CY7C1009-25VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C109-25VI	V33	32-Lead (400-Mil) Molded SOJ	Commercial
	CY7C109-25ZC	Z32	32-Lead TSOP Type I	Industrial
	CY7C109-25ZI	Z32	32-Lead TSOP Type I	Commercial
35	CY7C109-35VC	V33	32-Lead (400-Mil) Molded SOJ	Industrial
	CY7C1009-35VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C109-35VI	V33	32-Lead (400-Mil) Molded SOJ	Commercial

Shaded areas contain preliminary information.

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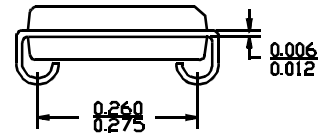
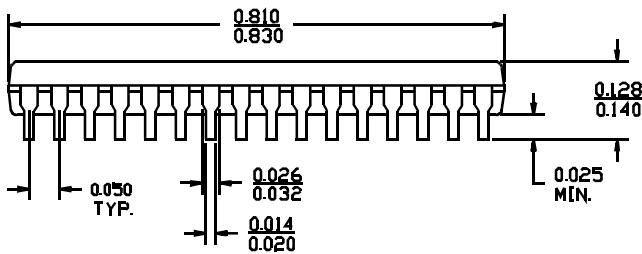
**Package Diagrams**

**32-Lead (300-Mil) Molded SOJ V32**



DIMENSIONS IN INCHES MIN.  
MAX.

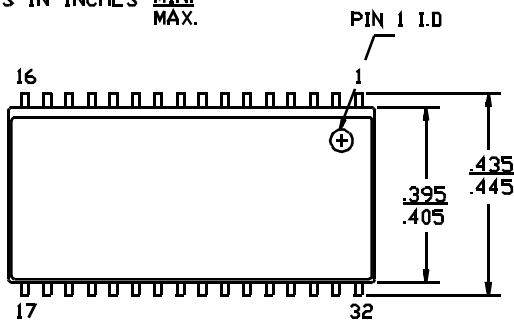
LEAD COPLANARITY 0.004 MAX.



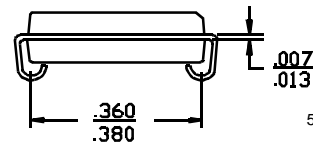
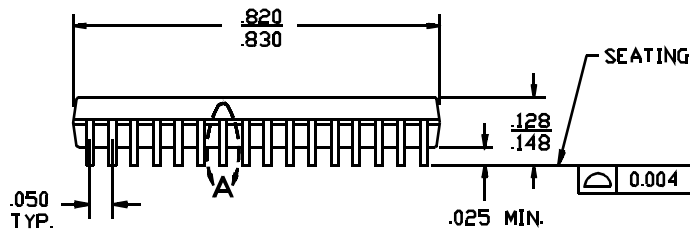
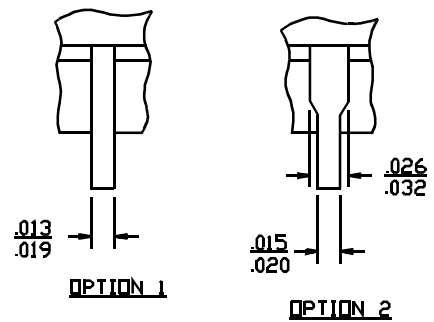
51-85041-A

**32-Lead (400-Mil) Molded SOJ V33**

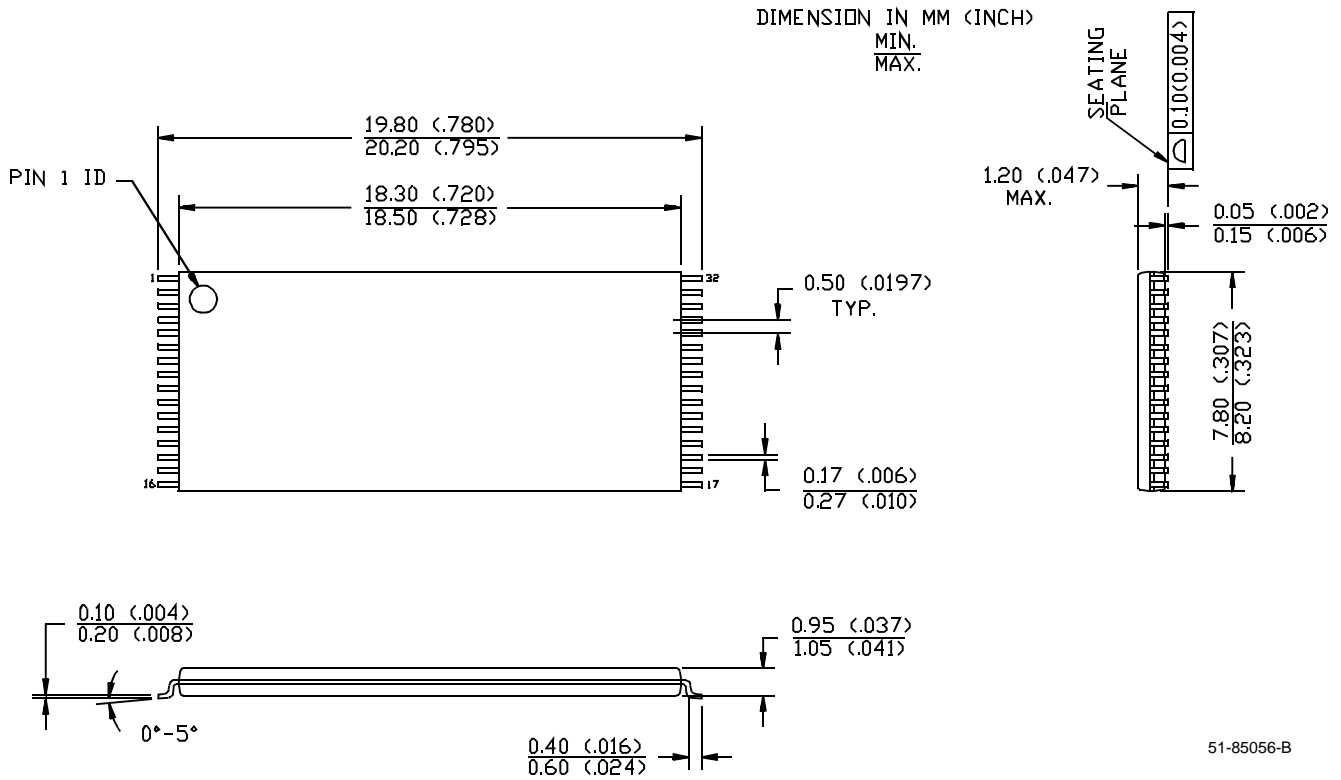
DIMENSIONS IN INCHES MIN.  
MAX.



**DETAIL A**  
**EXTERNAL LEAD DESIGN**



51-85033-A

**Package Diagrams (continued)**
**32-Lead Thin Small Outline Package Z32**


51-85056-B