CY7C1297A/ GVT7164B18

64K X 18 Synchronous Burst SRAM

Features

- **Fast access times: 9 and 10 ns**
- **Fast clock speed: 66 and 50 MHz**
- **Provide high performance 2-1-1-1 access rate**
- **Fast $\overline{OE}$ access times: 5 and 6 ns**
- **Single +3.3V –5% and +10% power supply**
- **5V tolerant inputs except I/Os**
- **Clamp diodes to V_{SSQ} at all inputs and outputs**
- **Common data inputs and data outputs**
- **Byte Write Enable and Global Write control**
- **Three chip enables for depth expansion and address pipeline**
- **Address, data, and control registers**
- **Internally self-timed Write Cycle**
- **Burst control pins (interleaved or linear burst sequence)**
- **Automatic power-down for portable applications**
- **High-density, high-speed packages**
- **Low-capacitive bus loading**
- **High 30-pF output drive capability at rated access time**

Functional Description

The Cypress Synchronous Burst SRAM family employs high-speed, low-power CMOS designs using advanced double-layer polysilicon, double-layer metal technology. Each memory cell consists of four transistors and two high-valued resistors.

The CY7C1297A/GVT7164B18 SRAM integrates 65536 × 18 SRAM cells with advanced synchronous peripheral circuitry and a two-bit counter for internal burst operation. All synchronous inputs are gated by registers controlled by a positive-edge-triggered Clock Input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining Chip Enable ($\overline{CE}$), depth-expansion Chip Enables (CE2 and $\overline{CE2}$), Burst Control inputs ($\overline{ADSC}$, $\overline{ADSP}$, and $\overline{ADV}$), Write Enables ($\overline{WEL}$, $\overline{WEH}$, and $\overline{BWE}$), and Global Write ($\overline{GW}$).

Asynchronous inputs include the Output Enable ($\overline{OE}$), Burst Mode Control (MODE), and Sleep Mode Control (ZZ). The data outputs (DQ), enabled by $\overline{OE}$, are also asynchronous.

Addresses and chip enables are registered with either Address Status Processor ($\overline{ADSP}$) or Address Status Controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be internally generated as controlled by the Burst Advance pin ($\overline{ADV}$).

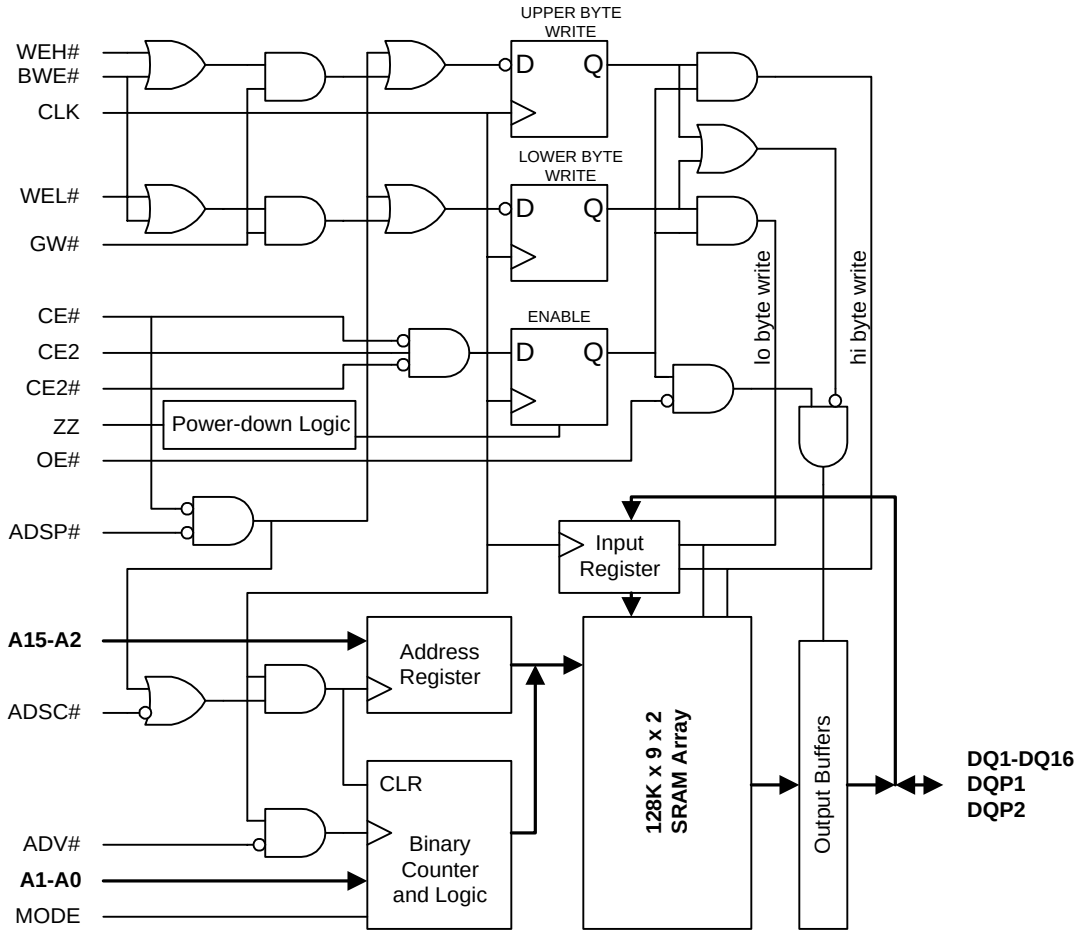
Address, data inputs, and Read controls are registered on-chip to initiate self-timed Write cycle. Write cycles can be one or two bytes wide as controlled by the Read control inputs. Individual byte enables allow individual bytes to be written. $\overline{WEL}$ controls DQ1–DQ8 and DQP1. $\overline{WEH}$ controls DQ9–DQ16 and DQP2. $\overline{WEL}$ and $\overline{WEH}$ can be active only with $\overline{BWE}$ being LOW. $\overline{GW}$ being LOW causes all bytes to be written.

The CY7C1297A/GVT7164B18 operates from a +3.3V power supply. All inputs and outputs are TTL-compatible. The device is ideally suited for 486, Pentium®, 680 × 0, and PowerPC™ systems and for systems that benefit from a wide synchronous data bus.

Selection Guide

	7C1297A-66 7164B18-9	7C1297A-50 7164B18-10	7C1297A1-50 7164B18-12	Unit
Maximum Access Time	9.0	10.0	10.0	ns
Maximum Operating Current	240	240	240	mA
Maximum CMOS Standby Current	2	2	2	mA

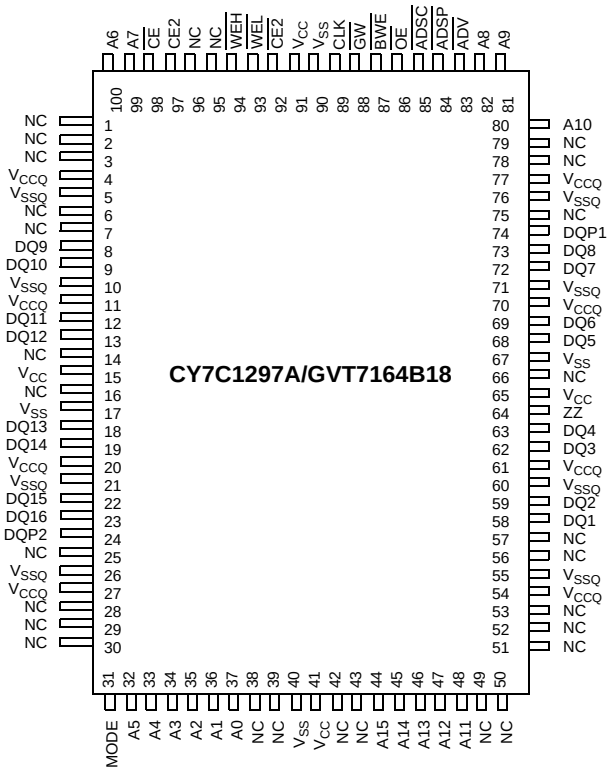
Functional Block Diagram—64Kx18[1]



Note:
1. The functional block diagram illustrates simplified device operation. See Truth Table, pin descriptions, and timing diagrams for detailed information.

Pin Configuration

100-pin TQFP
Top View



Pin Descriptions

QFP Pins	Pin Name	Type	Description
37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 80, 48, 47, 46, 45, 44	A0–A16	Input-Synchronous	**Addresses**: These inputs are registered and must meet the set-up and hold times around the rising edge of CLK. The burst counter generates internal addresses associated with A0 and A1, during burst and wait cycles.
93, 94	$\overline{WEL}$, $\overline{WEH}$	Input-Synchronous	**Byte Write Enables**: A byte Read enable is LOW for a Write cycle and HIGH for a Read cycle. WEL controls DQ1–DQ8 and DQP1. WEH controls DQ9–DQ16 and DQP2. Data I/O are high impedance if either of these inputs are LOW, conditioned by $\overline{BWE}$ LOW.
87	$\overline{BWE}$	Input-Synchronous	**Write Enable**: This active LOW input gates byte Read operations and must meet the set-up and hold times around the rising edge of CLK.
88	$\overline{GW}$	Input-Synchronous	**Global Write**: This active LOW input allows a full 18-bit Write to occur independent of the $\overline{BWE}$ and $\overline{WEn}$ lines and must meet the set-up and hold times around the rising edge of CLK.
89	CLK	Input-Synchronous	**Clock**: This signal registers the addresses, data, chip enables, Write control and burst control inputs on its rising edge. All synchronous inputs must meet set-up and hold times around the clock's rising edge.
98	$\overline{CE}$	Input-Synchronous	**Chip Enable**: This active LOW input is used to enable the device and to gate $\overline{ADSP}$.
92	$\overline{CE2}$	Input-Synchronous	**Chip Enable**: This active LOW input is used to enable the device.
97	CE2	Input-Synchronous	**Chip Enable**: This active HIGH input is used to enable the device.

Pin Descriptions (continued)

QFP Pins	Pin Name	Type	Description
86	$\overline{OE}$	Input	**Output Enable**: This active LOW asynchronous input enables the data output drivers.
83	$\overline{ADV}$	Input-Synchronous	**Address Advance**: This active LOW input is used to control the internal burst counter. A HIGH on this pin generates wait cycle (no address advance).
84	$\overline{ADSP}$	Input-Synchronous	**Address Status Processor**: This active LOW input, along with $\overline{CE}$ being LOW, causes a new external address to be registered and a Read cycle is initiated using the new address.
85	$\overline{ADSC}$	Input-Synchronous	**Address Status Controller**: This active LOW input causes device to be deselected or selected along with new external address to be registered. A Read or Write cycle is initiated depending upon Write control inputs.
31	MODE	Input-Static	**Mode**: This input selects the burst sequence. A LOW on this pin selects Linear Burst. A NC or HIGH on this pin selects Interleaved Burst.
64	ZZ	Input-Asynchronous	**Snooze**: This active HIGH input puts the device in low power consumption standby mode. For normal operation, this input has to be either LOW or NC (No Connect).
58, 59, 62, 63, 68, 69, 72, 73, 8, 9, 12, 13, 18, 19, 22, 23	DQ1–DQ16	Input/ Output	**Data Inputs/Outputs**: Low Byte is DQ1–DQ8. High Byte is DQ9–DQ16. Input data must meet set-up and hold times around the rising edge of CLK.
74, 24	DQP1, DQP2	Input/ Output	**Parity Inputs/Outputs**: DQP1 is parity bit for DQ1–DQ8 and DQP2 is parity bit for DQ9–DQ16.
15, 41, 65, 91	V_{CC}	Supply	**Power Supply**: +3.3V –5% and +10%
14, 17, 40, 67, 90	V_{SS}	Ground	**Ground**: GND.
4, 11, 20, 27, 54, 61, 70, 77	V_{CCQ}	I/O Supply	**Output Buffer Supply**: +2.375 to 3.6V
5, 10, 21, 26, 55, 60, 71, 76	V_{SSQ}	I/O Ground	**Output Buffer Ground**: GND
1–3, 6, 7, 14, 16, 25, 28–30, 38, 39, 42, 43, 49–53, 56, 57, 66, 75, 78, 79, 80, 95, 96	NC	–	**No Connect**: These signals are not internally connected.

Burst Address Table (MODE = NC/V_{CC})

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
A...A00	A...A01	A...A10	A...A11
A...A01	A...A00	A...A11	A...A10
A...A10	A...A11	A...A00	A...A01
A...A11	A...A10	A...A01	A...A00

Burst Address Table (MODE = GND)

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
A...A00	A...A01	A...A10	A...A11
A...A01	A...A10	A...A11	A...A00
A...A10	A...A11	A...A00	A...A01
A...A11	A...A00	A...A01	A...A10

Truth Table[2, 3, 4, 5, 6, 7, 8]

Operation	Address Used	$\overline{CE}$	$\overline{CE2}$	CE2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected Cycle, Power Down	None	H	X	X	X	L	X	X	X	L–H	High-Z
Deselected Cycle, Power Down	None	L	X	L	L	X	X	X	X	L–H	High-Z
Deselected Cycle, Power Down	None	L	H	X	L	X	X	X	X	L–H	High-Z
Deselected Cycle, Power Down	None	L	X	L	H	L	X	X	X	L–H	High-Z
Deselected Cycle, Power Down	None	L	H	X	H	L	X	X	X	L–H	High-Z
Read Cycle, Begin Burst	External	L	L	H	L	X	X	X	L	L–H	Q
Read Cycle, Begin Burst	External	L	L	H	L	X	X	X	H	L–H	High-Z
Write Cycle, Begin Burst	External	L	L	H	H	L	X	L	X	L–H	D
Read Cycle, Begin Burst	External	L	L	H	H	L	X	H	L	L–H	Q
Read Cycle, Begin Burst	External	L	L	H	H	L	X	H	H	L–H	High-Z
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	L	L–H	Q
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	L–H	High-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	L	L–H	Q
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	L–H	High-Z
Write Cycle, Continue Burst	Next	X	X	X	H	H	L	L	X	L–H	D
Write Cycle, Continue Burst	Next	H	X	X	X	H	L	L	X	L–H	D
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	L	L–H	Q
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	L–H	High-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	L–H	Q
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	L–H	High-Z
Write Cycle, Suspend Burst	Current	X	X	X	H	H	H	L	X	L–H	D
Write Cycle, Suspend Burst	Current	H	X	X	X	H	H	L	X	L–H	D

Partial Truth Table for Read/Write

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{WEH}$	$\overline{WEL}$
Read	H	H	X	X
Read	H	L	H	H
Write one byte	H	L	L	H
Write all bytes	H	L	L	L
Write all bytes	L	X	X	X

Notes:

2. X means "don't care." H means logic HIGH. L means logic LOW. $\overline{WRITE}$ = L means [$\overline{BWE}$ + $\overline{WEL}$*$\overline{WEH}$]*$\overline{GW}$ equals LOW. $\overline{WRITE}$ = H means [$\overline{BWE}$ + WEL*WEH]*GW equals HIGH.
3. $\overline{WEL}$ enables Write to DQ1–DQ8 and DQP1. $\overline{WEH}$ enables Write to DQ9–DQ16 and DQP2.
4. All inputs except $\overline{OE}$ must meet set-up and hold times around the rising edge (LOW to HIGH) of CLK.
5. Suspending burst generates wait cycle.
6. For a Write operation following a Read operation, $\overline{OE}$ must be HIGH before the input data required setup time plus High-Z time for $\overline{OE}$ and staying HIGH throughout the input data hold time.
7. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
8. $\overline{ADSP}$ LOW along with chip being selected always initiates a Read cycle at the L–H edge of CLK. A Write cycle can be performed by setting $\overline{WRITE}$ LOW for the CLK L–H edge of the subsequent wait cycle. Refer to Write timing diagram for clarification.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Voltage on V_{CC} Supply Relative to V_{SS} ..... –0.5V to +4.6V

V_{IN} .....–0.5V to V_{CC}+0.5V

Storage Temperature (plastic) .....–55°C to +125°C

Junction Temperature .....+125°C

Power Dissipation..... 1.4W

Short Circuit Output Current..... 100 mA

Operating Range

Range	Ambient Temperature[9]	V_{CC}[10,11]
Com'l	0°C to +70°C	3.3V –5%/+10%

Electrical Characteristics Over the Operating Range[12]

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{IH}	Input High (Logic 1) Voltage[13, 14]		2.0	V_{CCQ}+0.3	V
V_{Il}	Input Low (Logic 0) Voltage[13, 14]		–0.3	0.8	V
IL_I	Input Leakage Current[15]	$0V \le V_{IN} \le V_{CC}$	–2	2	µA
IL_O	Output Leakage Current	Output(s) disabled, $0V \le V_{OUT} \le V_{CC}$	–2	2	µA
V_{OH}	Output High Voltage[13, 16]	I_{OH} = –4.0 mA	2.4		V
V_{OL}	Output Low Voltage[13, 16]	I_{OL} = 8.0 mA		0.4	V
V_{CC}	Supply Voltage[13]		3.1	3.6	V

Parameter	Description	Conditions	Typ.	66 MHz -9	50 MHz -10	50 MHz -12	Unit
I_{CC}	Power Supply Current: Operating[17, 18, 19]	Device selected; all inputs $\le V_{IL}$ or $\ge V_{IH}$; cycle time $\ge t_{KC}$ min.; V_{CC} = Max.; outputs open	150	240	240	200	mA
I_{SB1}	Power Supply Current: Idle[18, 19]	Device selected; $\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$, $\overline{GW}$, $\overline{BWE}$ $\ge V_{IH}$; all other inputs $\le V_{IL}$ or $\ge V_{IH}$; V_{CC} = Max.; cycle time $\ge t_{KC}$ min.; outputs open	15	40	40	30	mA
I_{SB2}	CMOS Standby[18, 19]	Device deselected; V_{CC} = Max.; all inputs $\le V_{SS}$ + 0.2 or $\ge V_{CC}$ – 0.2; all inputs static; CLK frequency = 0	0.2	2	2	2	mA
I_{SB3}	TTL Standby[18, 19]	Device deselected; all inputs $\le V_{IL}$ or $\ge V_{IH}$; all inputs static; V_{CC} = Max.; CLK frequency = 0	4	10	10	10	mA
I_{SB4}	Clock Running[18, 19]	Device deselected; all inputs $\le V_{IL}$ or $\ge V_{IH}$; V_{CC} = Max.; CLK cycle time $\ge t_{KC}$ min.	15	40	40	30	mA

Capacitance[20]

Parameter	Description	Test Conditions	Typ.	Max.	Unit
C_I	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	3	4	pF
C_O	Input/Output Capacitance (DQ)		6	7	pF

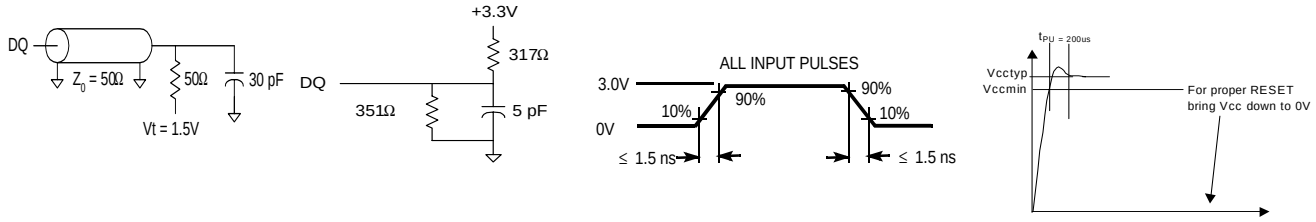
Notes:

9. T_A is the case temperature.
10. Please refer to waveform (d)
11. Power Supply ramp-up should be monotonic.
12. Values in table are associated with the operating frequencies listed.
13. All voltages referenced to V_{SS} (GND).
14. Overshoot: $V_{IH} \le +6.0V$ for $t \le t_{KC}/2$.
    Undershoot: $V_{IL} \le –2.0V$ for $t \le t_{KC}/2$.
15. MODE pin has an internal pull-up and ZZ pin has an internal pull-down. These two pins exhibit an input leakage current of ±30 µA.
16. AC I/O curves are available upon request.
17. I_{CC} is given with no output current. I_{CC} increases with greater output loading and faster cycle times.
18. "Device Deselected" means the device is in Power-down mode as defined in the truth table. "Device Selected" means the device is active.
19. Typical values are measured at 3.3V, 25°C, and 20-ns cycle time.
20. This parameter is sampled.

Thermal Resistance

Description	Test Conditions	Symbol	TQFP Typ.	Unit
Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 4.25 x 1.125 inch, four-layer PCB	Θ_{JA}	20	°C/W
Thermal Resistance (Junction to Case)		Θ_{JC}	91	°C/W

AC Test Loads and Waveforms[21]



(a) **(b)** **(c)** **(d)**

Capacitance Derating[22]

Description	Symbol	Typ.	Max.	Unit
Clock to Output Valid	Δt_{KQ}	0.016		ns / pF

Switching Characteristics Over the Operating Range[23]

Parameter	Description	66 MHz -9		50 MHz -10		50 MHz -12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Clock								
t_{KC}	Clock Cycle Time	15		15		20		ns
t_{KH}	Clock HIGH Time	4		5		6		ns
t_{KL}	Clock LOW Time	4		5		6		ns
Output Times								
t_{KQ}	Clock to Output Valid		9		10		12	ns
t_{KQX}	Clock to Output Invalid	3		3		3		ns
t_{KQLZ}	Clock to Output in Low-Z[24, 25]	3		3		3		ns
t_{KQHZ}	Clock to Output in High-Z[24, 25]		5		5		6	ns
t_{OEQ}	OE to Output Valid[26]		5		5		6	ns
t_{OELZ}	OE to Output in Low-Z[24, 25]	0		0		0		ns
t_{OEHZ}	OE to Output in High-Z[24, 25]		5		5		6	ns
Set-up Times								
t_S	Address, Controls, and Data In[27]	2.5		2.5		3		ns
Hold Times								
t_H	Address, Controls, and Data In[27]	0.5		0.5		0.5		ns

Switching Characteristics Over the Operating Range[23]

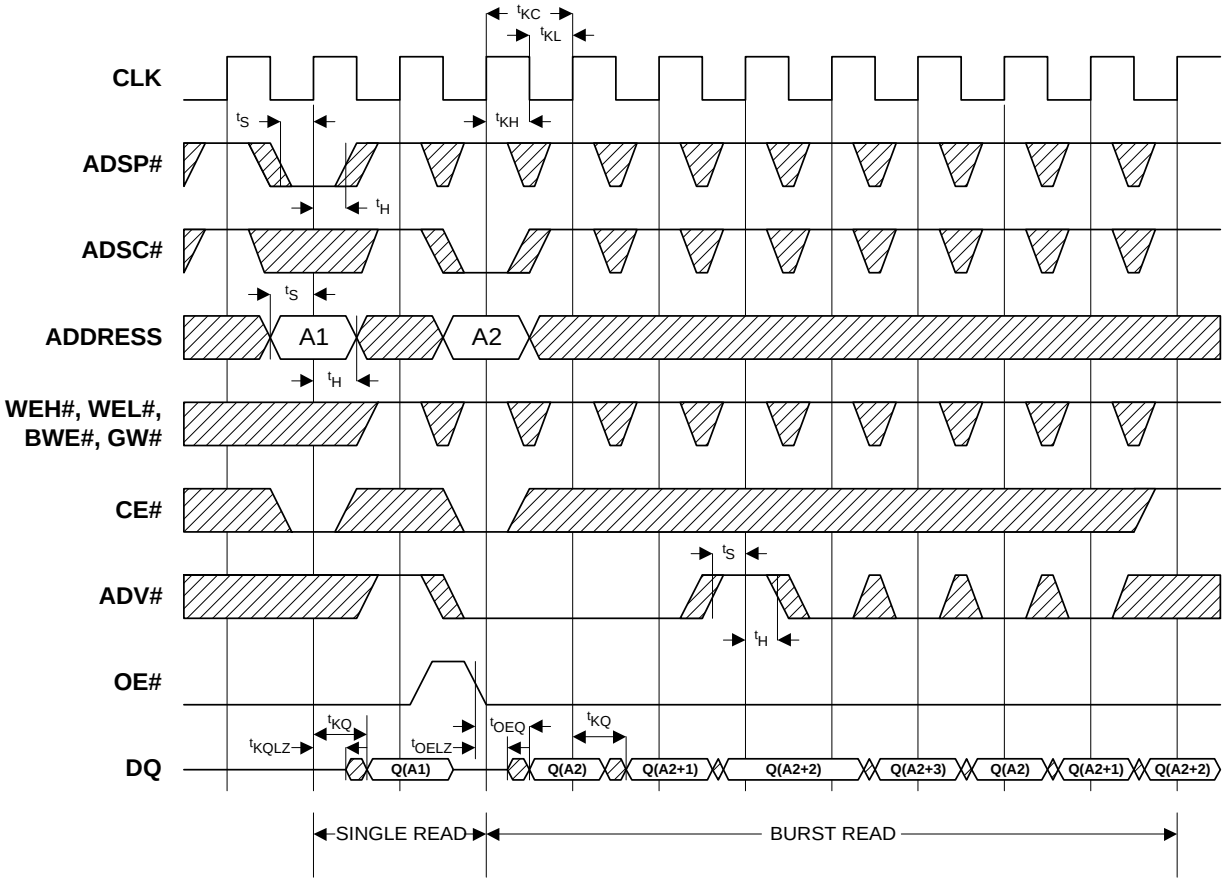
Parameter	Description	66 MHz -9		50 MHz -10		50 MHz -12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	

Notes:

21. Overshoot: VIH(AC) <VDD + 1.5V for t <tTCYC/2; undershoot: VIL(AC) < 0.5V for t <tTCYC/2; power-up: VIH < 2.6V and VDD <2.4V and VDDQ < 1.4V for t<200 ms.)
22. Capacitance derating applies to capacitance different from the load capacitance shown in part (a) of AC Test Loads. Values in table are associated with the operating frequencies listed.
23. Test conditions as specified with the output loading as shown in part (a) of AC Test Loads unless otherwise noted.
24. Output loading is specified with C_L = 5 pF as in AC Test Loads.
25. At any given temperature and voltage condition, t_{KQHZ} is less than t_{KQLZ} and t_{OEHZ} is less than t_{OELZ}.
26. $\overline{OE}$ is a “don’t care” when a byte Write enable is sampled LOW.
27. This is a synchronous device. All synchronous inputs must meet specified set-up and hold time, except for “don’t care” as defined in the truth table.

Timing Diagrams

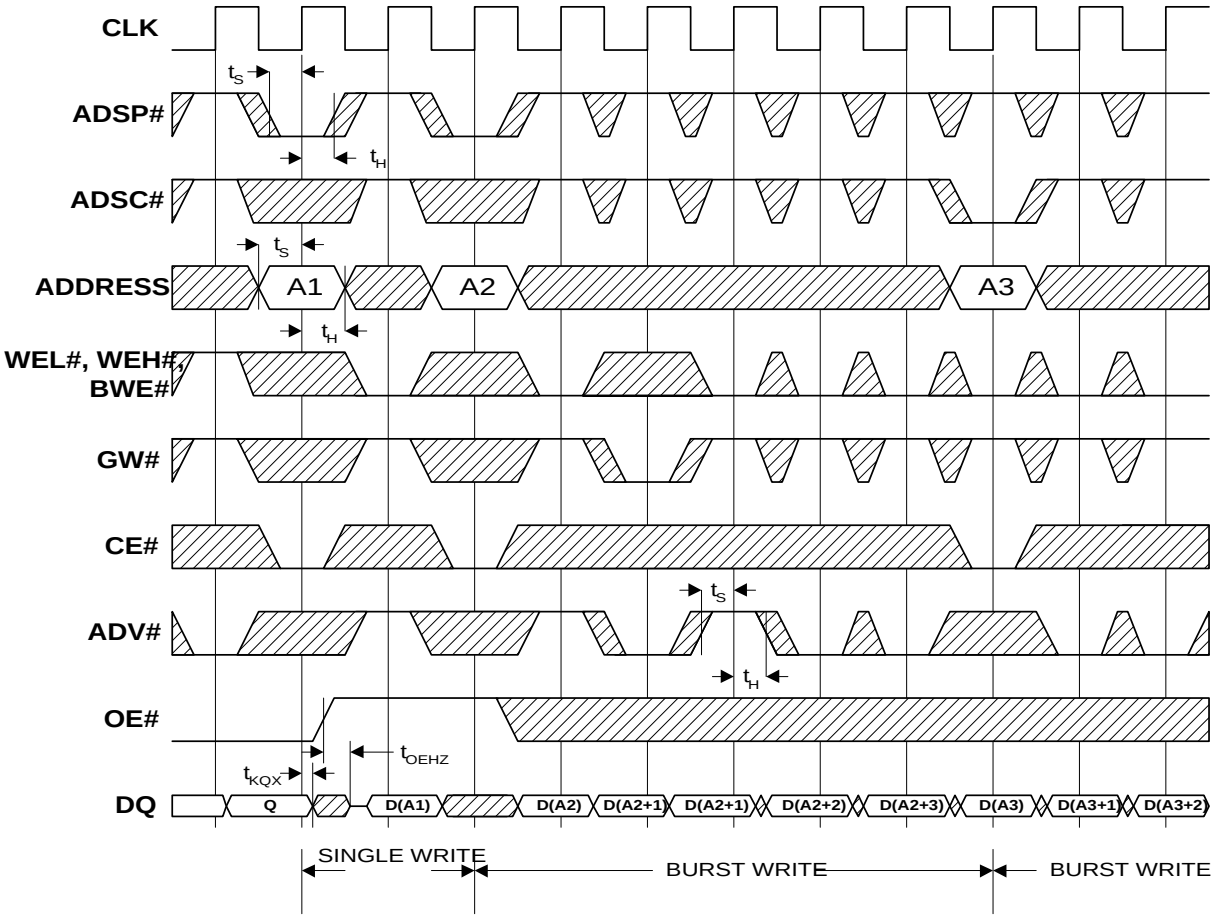
Read Timing[28]



Note:
28. $\overline{CE}$ active in this timing diagram means that all chip enables $\overline{CE}$, CE2, and $\overline{CE2}$ are active.

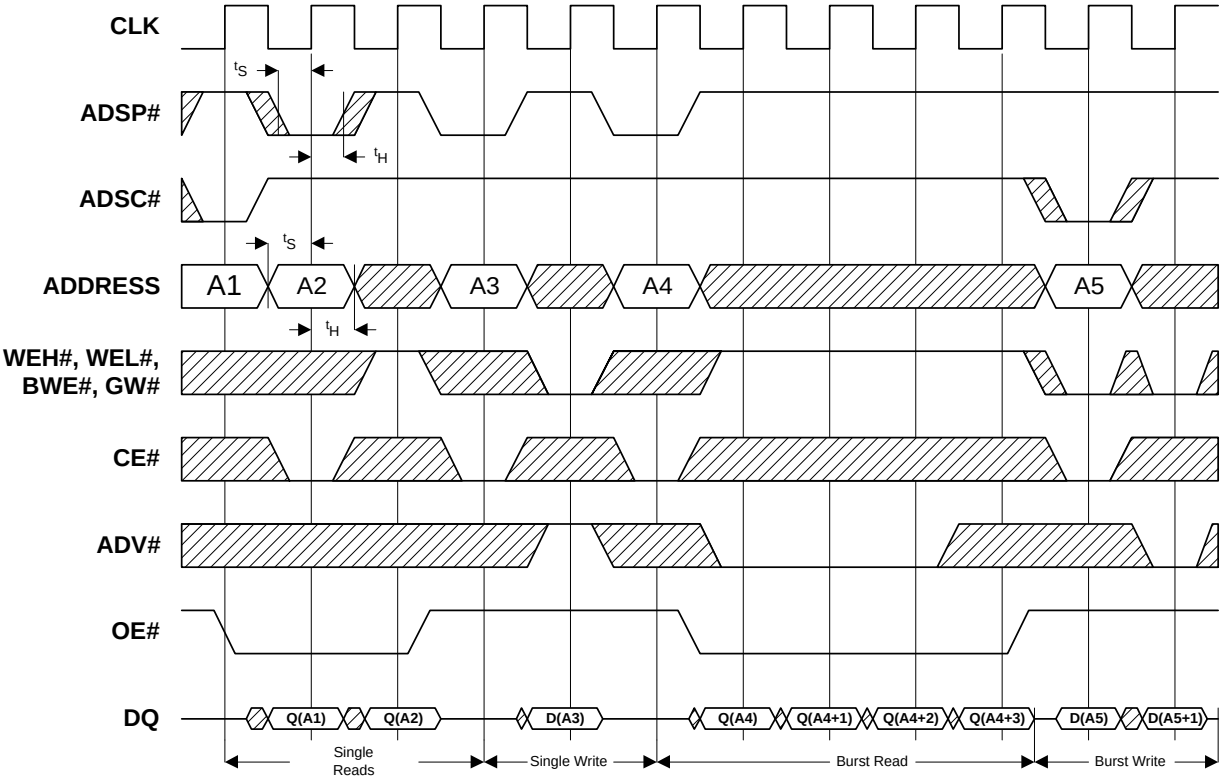
Timing Diagrams (continued)

Write Timing[28]



Timing Diagrams (continued)

Read/Write Timing[28]

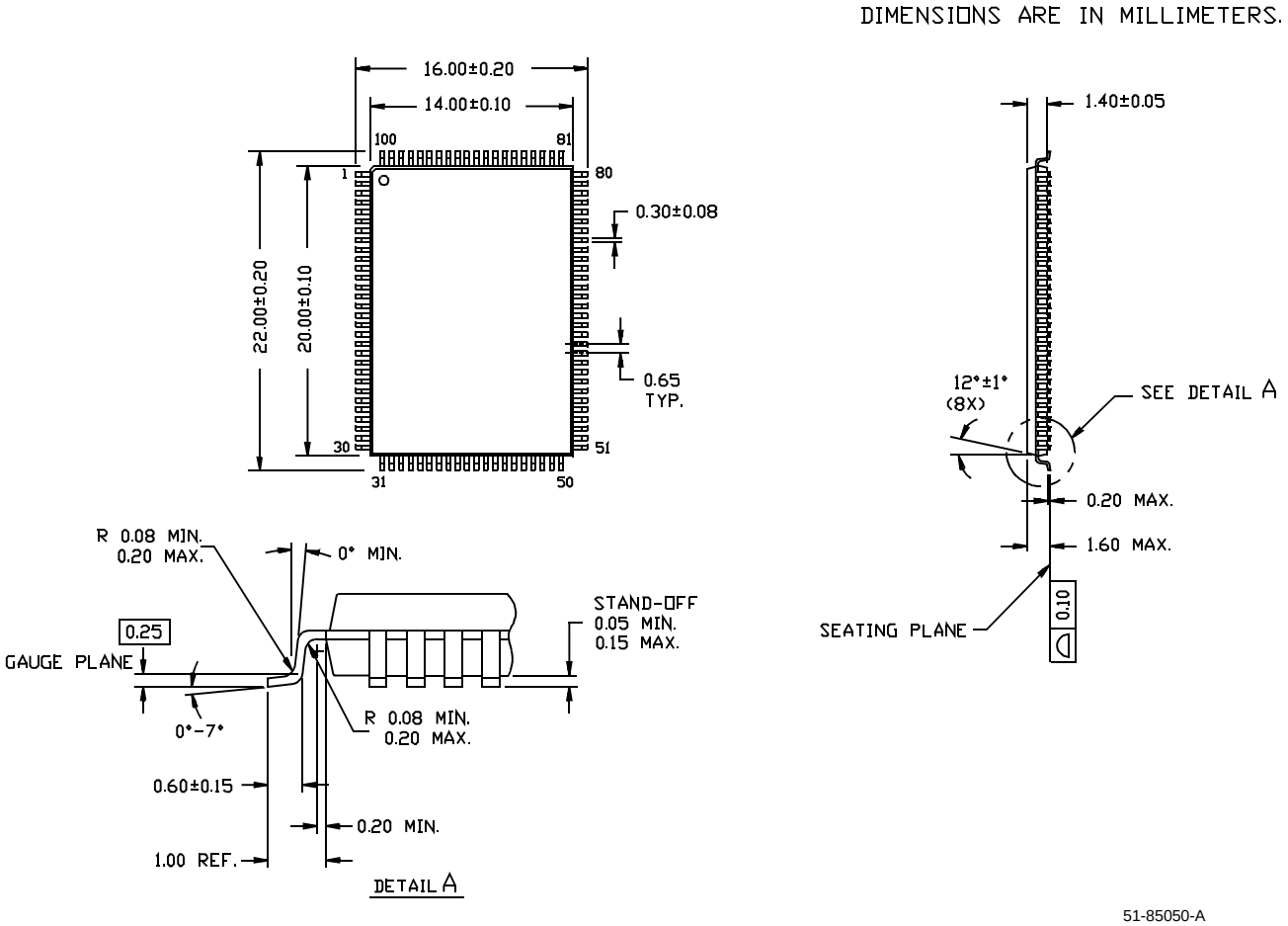


Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
66	CY7C1297A-66AC/ GVT7164B18T-9	A101	100-lead Thin Quad Flat Pack	Commercial
50	CY7C1297A-50AC/ GVT7164B18T-10	A101	100-lead Thin Quad Flat Pack	Commercial
	CY7C1297A1-50AC/ GVT7164B18T-12	A101	100-lead Thin Quad Flat Pack	Commercial

Package Diagram

100-pin Thin Plastic Quad Flatpack (14 × 20 × 1.4 mm) A101



Document Title: CY7C1297A/GVT7164B18 64K × 18 Synchronous Burst SRAM Document Number: 38-05204				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	112434	02/06/02	KOM	Change CY part number from CY7C1314A to CY7C1297A
*A	123141	01/19/03	RBI	Add Power up Requirements to Operating Conditions Information