



# 4-Mb (128K x 32) Pipelined DCD Sync SRAM

## Features

- Registered inputs and outputs for pipelined operation
- Optimal for performance (Double-Cycle deselect)
  - Depth expansion without wait state
- 128K x 32-bit common I/O architecture
- 3.3V -5% and +10% core power supply (V<sub>DD</sub>)
- 3.3V / 2.5V I/O supply (V<sub>DDQ</sub>)
- Fast clock-to-output times
  - 2.6 ns (for 250-MHz device)
  - 2.6 ns (for 225-MHz device)
  - 2.8 ns (for 200-MHz device)
  - 3.5 ns (for 166-MHz device)
  - 4.0 ns (for 133-MHz device)
  - 4.5 ns (for 100-MHz device)
- Provide high-performance 3-1-1-1 access rate
- User-selectable burst counter supporting Intel® Pentium® interleaved or linear burst sequences
- Separate processor and controller address strobes
- Synchronous self-timed writes
- Asynchronous Output Enable
- JEDEC-standard 100-pin TQFP package and pinout
- “ZZ” Sleep Mode option

## Functional Description<sup>[1]</sup>

The CY7C1340F SRAM integrates 131,072 x 32 SRAM cells with advanced synchronous peripheral circuitry and a two-bit counter for internal burst operation. All synchronous inputs are gated by registers controlled by a positive-edge-triggered Clock Input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining Chip Enable ( $\overline{CE}_1$ ), depth-expansion Chip Enables ( $\overline{CE}_2$  and  $\overline{CE}_3$ ), Burst Control inputs ( $\overline{ADSC}$ ,  $\overline{ADSP}$ , and  $\overline{ADV}$ ), Write Enables ( $\overline{BW}_{[A:D]}$ , and  $\overline{BWE}$ ), and Global Write ( $\overline{GW}$ ). Asynchronous inputs include the Output Enable ( $\overline{OE}$ ) and the ZZ pin.

Addresses and chip enables are registered at rising edge of clock when either Address Strobe Processor ( $\overline{ADSP}$ ) or Address Strobe Controller ( $\overline{ADSC}$ ) are active. Subsequent burst addresses can be internally generated as controlled by the Advance pin ( $\overline{ADV}$ ).

Address, data inputs, and write controls are registered on-chip to initiate a self-timed Write cycle. This part supports Byte Write operations (see Pin Descriptions and Truth Table for further details). Write cycles can be one to four bytes wide as controlled by the byte write control inputs.  $\overline{GW}$  active LOW causes all bytes to be written. This device incorporates an additional pipelined enable register which delays turning off the output buffers an additional cycle when a deselect is executed. This feature allows depth expansion without penalizing system performance.

The CY7C1340F operates from a +3.3V core power supply while all outputs operate with a +3.3V or a +2.5V supply. All inputs and outputs are JEDEC-standard JESD8-5-compatible.

## Selection Guide

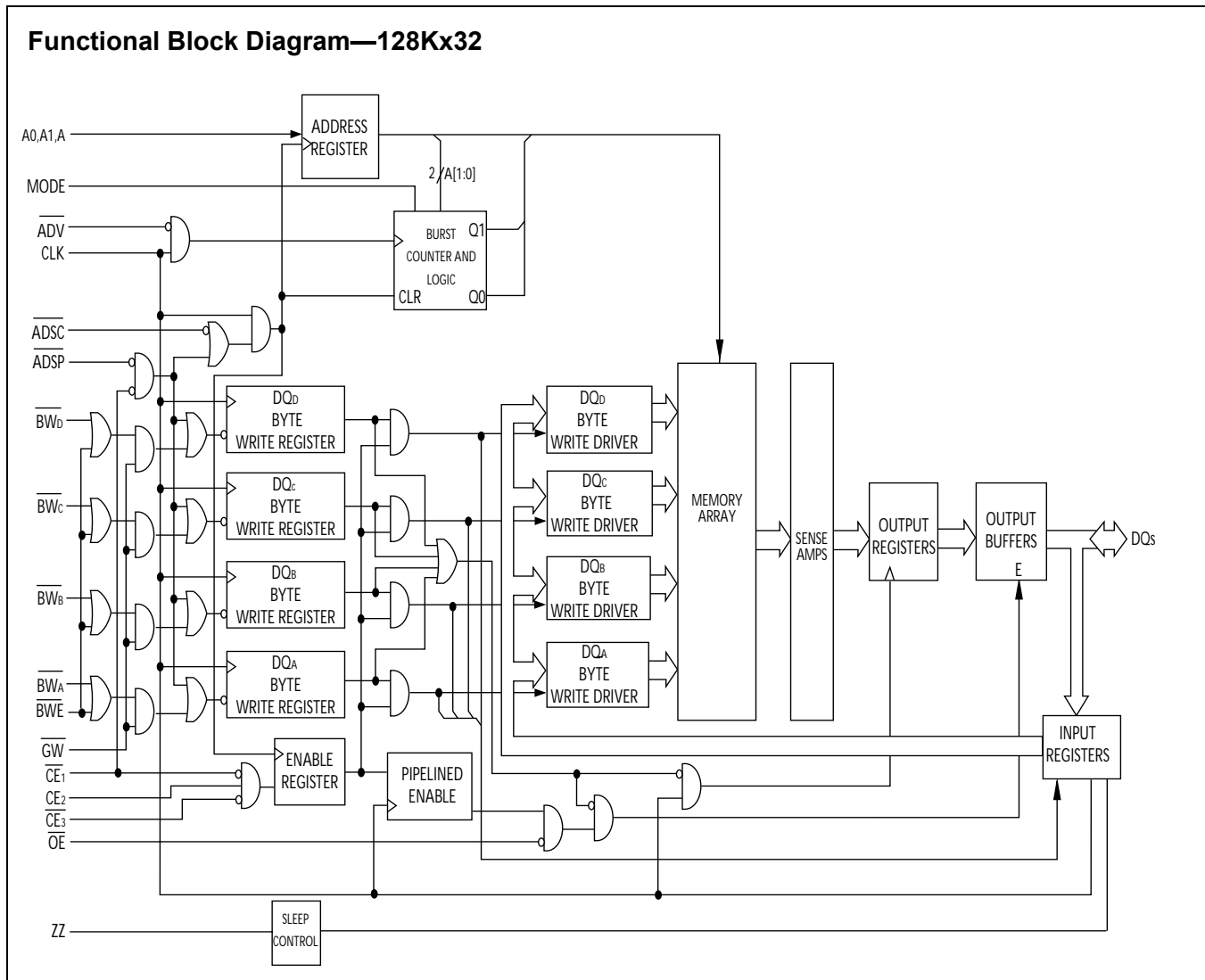
	250 MHz	225 MHz	200 MHz	166 MHz	133 MHz	100 MHz	Unit
Maximum Access Time	2.6	2.6	2.8	3.5	4.0	4.5	ns
Maximum Operating Current	325	290	265	240	225	205	mA
Maximum CMOS Standby Current	40	40	40	40	40	40	mA

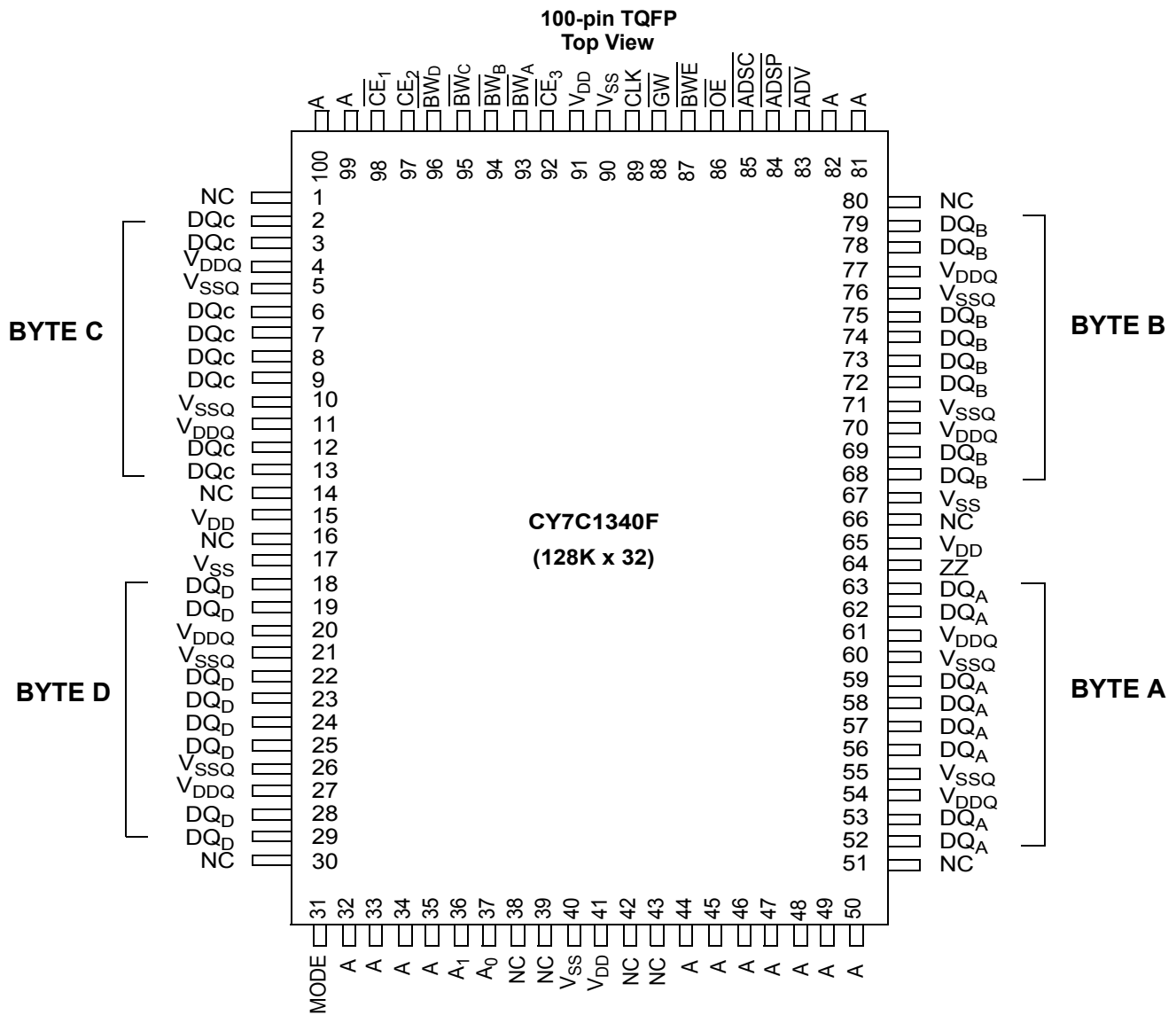
Shaded areas contain advance information.  
Please contact your local Cypress sales representative for availability of these parts.

### Note:

1. For best-practices recommendations, please refer to the Cypress application note *System Design Guidelines* on [www.cypress.com](http://www.cypress.com).

**Functional Block Diagram—128Kx32**



**Pin Configurations**


**Pin Descriptions**

Pin	TQFP	Type	Description
A <sub>0</sub> , A <sub>1</sub> , A	37,36,32,33 34,35,44,45, 46,47,48,49, 50,81,82,99, 100	Input- Synchronous	<b>Address Inputs used to select one of the 128K address locations.</b> Sampled at the rising edge of the CLK if ADSP or ADSC is active LOW, and CE <sub>1</sub> , CE <sub>2</sub> , and CE <sub>3</sub> are sampled active. A <sub>[1:0]</sub> are fed to the two-bit counter.
BW <sub>A</sub> , BW <sub>B</sub> , BW <sub>C</sub> , BW <sub>D</sub>	93,94,95,96	Input- Synchronous	<b>Byte Write Select Inputs, active LOW.</b> Qualified with $\overline{BWE}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{GW}$	88	Input- Synchronous	<b>Global Write Enable Input, active LOW.</b> When asserted LOW on the rising edge of CLK, a global write is conducted (ALL bytes are written, regardless of the values on BW <sub>[A:D]</sub> and BWE).
$\overline{BWE}$	87	Input- Synchronous	<b>Byte Write Enable Input, active LOW.</b> Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
CLK	89	Input- Clock	<b>Clock Input.</b> Used to capture all synchronous inputs to the device. Also used to increment the burst counter when ADV is asserted LOW, during a burst operation.
$\overline{CE}_1$	98	Input- Synchronous	<b>Chip Enable 1 Input, active LOW.</b> Sampled on the rising edge of CLK. Used in conjunction with CE <sub>2</sub> and CE <sub>3</sub> to select/deselect the device. ADSP is ignored if CE <sub>1</sub> is HIGH.
CE <sub>2</sub>	97	Input- Synchronous	<b>Chip Enable 2 Input, active HIGH.</b> Sampled on the rising edge of CLK. Used in conjunction with CE <sub>1</sub> and CE <sub>3</sub> to select/deselect the device.
$\overline{CE}_3$	92	Input- Synchronous	<b>Chip Enable 3 Input, active LOW.</b> Sampled on the rising edge of CLK. Used in conjunction with CE <sub>1</sub> and CE <sub>2</sub> to select/deselect the device.
$\overline{OE}$	86	Input- Asynchronous	<b>Output Enable, asynchronous input, active LOW.</b> Controls the direction of the DQ pins. When LOW, the DQ pins behave as outputs. When deasserted HIGH, DQ pins are three-stated, and act as input data pins. $\overline{OE}$ is masked during the first clock of a read cycle when emerging from a deselected state.
$\overline{ADV}$	83	Input- Synchronous	<b>Advance Input signal, sampled on the rising edge of CLK, active LOW.</b> When asserted, it automatically increments the address in a burst cycle.
$\overline{ADSP}$	84	Input- Synchronous	<b>Address Strobe from Processor, sampled on the rising edge of CLK, active LOW.</b> When asserted LOW, addresses presented to the device are captured in the address registers. A <sub>[1:0]</sub> are also loaded into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized. ADSP is ignored when $\overline{CE}_1$ is deasserted HIGH.
$\overline{ADSC}$	85	Input- Synchronous	<b>Address Strobe from Controller, sampled on the rising edge of CLK, active LOW.</b> When asserted LOW, addresses presented to the device are captured in the address registers. A <sub>[1:0]</sub> are also loaded into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized.
ZZ	64	Input- Asynchronous	<b>ZZ "sleep" Input, active HIGH.</b> When asserted HIGH places the device in a non-time-critical "sleep" condition with data integrity preserved. For normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull-down.
DQs	52,53,56,57, 58,59,62,63 68,69,72,73, 74,75,78,79 2,3,6,7,8,9, 12,13 18,19,22,23, 24,25,28,29	I/O- Synchronous	<b>Bidirectional Data I/O lines.</b> As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$ . When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQs are placed in a three-state condition.
V <sub>DD</sub>	15,41,65, 91	Power Supply	<b>Power supply inputs to the core of the device.</b>
V <sub>SS</sub>	17,40,67, 90	Ground	<b>Ground for the core of the device.</b>
V <sub>DDQ</sub>	4,11,20,27, 54,61,70,77	I/O Power Supply	<b>Power supply for the I/O circuitry.</b>

**Pin Descriptions** (continued)

Pin	TQFP	Type	Description
V <sub>SSQ</sub>	5,10,21,26, 55,60,71,76	I/O Ground	<b>Ground for the I/O circuitry.</b>
MODE	31	Input-Static	<b>Selects Burst Order.</b> When tied to GND selects linear burst sequence. When tied to V <sub>DD</sub> or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation. Mode Pin has an internal pull-up.
NC	14,16,38,39, 42,43,66,1, 30,51,80		<b>No Connects.</b> Not internally connected to the die.

**Functional Overview**

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock.

The CY7C1340F supports secondary cache in systems utilizing either a linear or interleaved burst sequence. The interleaved burst order supports Pentium and i486™ processors. The linear burst sequence is suited for processors that utilize a linear burst sequence. The burst order is user selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the Processor Address Strobe (ADSP) or the Controller Address Strobe (ADSC). Address advancement through the burst sequence is controlled by the ADV input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the Byte Write Enable (BWE) and Byte Write Select (BW<sub>[A:D]</sub>) inputs. A Global Write Enable (GW) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self-timed write circuitry.

Synchronous Chip Selects  $\overline{CE}_1$ , CE<sub>2</sub>,  $\overline{CE}_3$  and an asynchronous Output Enable (OE) provide for easy bank selection and output three-state control. ADSP is ignored if  $\overline{CE}_1$  is HIGH.

**Single Read Accesses**

This access is initiated when the following conditions are satisfied at clock rise: (1)  $\overline{ADSP}$  or  $\overline{ADSC}$  is asserted LOW, (2) chip selects are all asserted active, and (3) the write signals (GW, BWE) are all deasserted HIGH. ADSP is ignored if  $\overline{CE}_1$  is HIGH. The address presented to the address inputs is stored into the address advancement logic and the Address Register while being presented to the memory core. The corresponding data is allowed to propagate to the input of the Output Registers. At the rising edge of the next clock the data is allowed to propagate through the output register and onto the data bus within  $t_{co}$  if  $\overline{OE}$  is active LOW. The only exception occurs when the SRAM is emerging from a deselected state to a selected state, its outputs are always three-stated during the first cycle of the access. After the first cycle of the access, the outputs are controlled by the OE signal. Consecutive single read cycles are supported.

The CY7C1340F is a double-cycle deselect part. Once the SRAM is deselected at clock rise by the chip select and either  $\overline{ADSP}$  or  $\overline{ADSC}$  signals, its output will three-state immediately after the next clock rise.

**Single Write Accesses Initiated by  $\overline{ADSP}$** 

This access is initiated when both of the following conditions are satisfied at clock rise: (1) ADSP is asserted LOW, and (2) chip select is asserted active. The address presented is loaded into the address register and the address advancement logic while being delivered to the memory core. The write signals (GW, BWE, and BW<sub>[A:D]</sub>) and ADV inputs are ignored during this first cycle.

ADSP triggered write accesses require two clock cycles to complete. If GW is asserted LOW on the second clock rise, the data presented to the DQx inputs is written into the corresponding address location in the memory core. If GW is HIGH, then the write operation is controlled by  $\overline{BWE}$  and  $\overline{BW}_{[A:D]}$  signals. The CY7C1340F provides byte write capability that is described in the Write Cycle Description table. Asserting the Byte Write Enable input (BWE) with the selected Byte Write input will selectively write to only the desired bytes. Bytes not selected during a byte write operation will remain unaltered. A synchronous self-timed write mechanism has been provided to simplify the write operations.

Because the CY7C1340F is a common I/O device, the Output Enable (OE) must be deasserted HIGH before presenting data to the DQ inputs. Doing so will three-state the output drivers. As a safety precaution, DQ are automatically three-stated whenever a write cycle is detected, regardless of the state of OE.

**Single Write Accesses Initiated by  $\overline{ADSC}$** 

ADSC write accesses are initiated when the following conditions are satisfied: (1) ADSC is asserted LOW, (2) ADSP is deasserted HIGH, (3) chip select is asserted active, and (4) the appropriate combination of the write inputs (GW, BWE, and BW<sub>[A:D]</sub>) are asserted active to conduct a write to the desired byte(s). ADSC triggered write accesses require a single clock cycle to complete. The address presented is loaded into the address register and the address advancement logic while being delivered to the memory core. The ADV input is ignored during this cycle. If a global write is conducted, the data presented to the DQx is written into the corresponding address location in the memory core. If a byte write is conducted, only the selected bytes are written. Bytes not selected during a byte write operation will remain unaltered. A synchronous self-timed write mechanism has been provided to simplify the write operations.

Because the CY7C1340F is a common I/O device, the Output Enable (OE) must be deasserted HIGH before presenting data to the DQx inputs. Doing so will three-state the output drivers. As a safety precaution, DQx are automatically three-stated whenever a write cycle is detected, regardless of the state of OE.

### Burst Sequences

The CY7C1340F provides a two-bit wraparound counter, fed by  $A_{[1:0]}$ , that implements either an interleaved or linear burst sequence. The interleaved burst sequence is designed specifically to support Intel Pentium applications. The linear burst sequence is designed to support processors that follow a linear burst sequence. The burst sequence is user selectable through the MODE input. Both read and write burst operations are supported.

Asserting  $\overline{ADV}$  LOW at clock rise will automatically increment the burst counter to the next address in the burst sequence. Both read and write burst operations are supported.

### Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the “sleep” mode. CEs, ADSP, and ADSC must remain inactive for the duration of  $t_{ZZREC}$  after the ZZ input returns LOW.

### ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min.	Max.	Unit
$I_{DDZZ}$	Snooze mode standby current	$ZZ \geq V_{DD} - 0.2V$		40	mA
$t_{ZZ}$	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2V$		$2t_{CYC}$	ns
$t_{ZZREC}$	ZZ recovery time	$ZZ \leq 0.2V$	$2t_{CYC}$		ns
$t_{ZZI}$	ZZ Active to snooze current	This parameter is sampled		$2t_{CYC}$	ns
$t_{RZZI}$	ZZ inactive to exit snooze current	This parameter is sampled	0		ns

### Interleaved Burst Address Table (MODE = Floating or $V_{DD}$ )

First Address A1, A0	Second Address A1, A0	Third Address A1, A0	Fourth Address A1, A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

### Linear Burst Address Table (MODE = GND)

First Address A1, A0	Second Address A1, A0	Third Address A1, A0	Fourth Address A1, A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

**Truth Table** [2, 3, 4, 5, 6]

Operation	Address Used	$\overline{CE}_1$	$CE_2$	$\overline{CE}_3$	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected Cycle, Power Down	None	H	X	X	L	X	L	X	X	X	L-H	Three-State
Deselected Cycle, Power Down	None	L	L	X	L	L	X	X	X	X	L-H	Three-State
Deselected Cycle, Power Down	None	L	X	H	L	L	X	X	X	X	L-H	Three-State
Deselected Cycle, Power Down	None	L	L	X	L	H	L	X	X	X	L-H	Three-State
Deselected Cycle, Power Down	None	L	X	H	L	H	L	X	X	X	L-H	Three-State
ZZ Mode, Power-Down	None	X	X	X	H	X	X	X	X	X	X	Three-State
Read Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	L	L-H	Q
Read Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	H	L-H	Three-State
Write Cycle, Begin Burst	External	L	H	L	L	H	L	X	L	X	L-H	D
Read Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	L	L-H	Q
Read Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	H	L-H	Three-State
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L-H	Three-State
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L-H	Three-State
Write Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
Write Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L-H	Three-State
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L-H	Three-State
Write Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
Write Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

**Partial Truth Table for Read/Write**[2, 7]

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BW}_A$	$\overline{BW}_B$	$\overline{BW}_C$	$\overline{BW}_D$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write byte A - $DQ_A$	H	L	L	H	H	H
Write byte B - $DQ_B$	H	L	H	L	H	H
Write byte C - $DQ_C$	H	L	H	H	L	H
Write byte D - $DQ_D$	H	L	H	H	H	L
Write all bytes	H	L	L	L	L	L
Write all bytes	L	X	X	X	X	X

**Notes:**

- X = "Don't Care." H = Logic HIGH, L = Logic LOW.
- $\overline{WRITE} = L$  when any one or more Byte Write enable signals ( $\overline{BW}_A$ ,  $\overline{BW}_B$ ,  $\overline{BW}_C$ ,  $\overline{BW}_D$ ) and  $\overline{BWE} = L$  or  $\overline{GW} = L$ .  $\overline{WRITE} = H$  when all Byte write enable signals ( $\overline{BW}_A$ ,  $\overline{BW}_B$ ,  $\overline{BW}_C$ ,  $\overline{BW}_D$ ),  $\overline{BWE}$ ,  $\overline{GW} = H$ .
- The DQ pins are controlled by the current cycle and the  $\overline{OE}$  signal.  $\overline{OE}$  is asynchronous and is not sampled with the clock.
- The SRAM always initiates a read cycle when  $\overline{ADSP}$  is asserted, regardless of the state of  $\overline{GW}$ ,  $\overline{BWE}$ , or  $\overline{BW}_{[A:D]}$ . Writes may occur only on subsequent clocks after the  $\overline{ADSP}$  or with the assertion of  $\overline{ADSC}$ . As a result,  $\overline{OE}$  must be driven HIGH prior to the start of the write cycle to allow the outputs to three-state.  $\overline{OE}$  is a don't care for the remainder of the write cycle.
- $\overline{OE}$  is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle all data bits are three-state when  $\overline{OE}$  is inactive or when the device is deselected, and all data bits behave as output when  $\overline{OE}$  is active (LOW).
- Table only lists a partial listing of the byte write combinations. Any combination of  $\overline{BW}_{[A:D]}$  is valid. Appropriate write will be done based on which byte write is active.

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°  
 Ambient Temperature with Power Applied.....-55°C to +125°C  
 Supply Voltage on V<sub>DD</sub> Relative to GND..... -0.5V to +4.6V  
 DC Voltage Applied to Outputs in Three-State ..... -0.5V to V<sub>DDQ</sub> + 0.5V  
 DC Input Voltage.....-0.5V to V<sub>DD</sub> + 0.5V  
 Current into Outputs (LOW) .....20 mA

Static Discharge Voltage..... >2001V  
 (per MIL-STD-883, Method 3015)

Latch -up Current..... >200 mA

**Operating Range**

Range	Ambient Temperature (T <sub>A</sub> )	V <sub>DD</sub>	V <sub>DDQ</sub>
Commercial	0°C to +70°C	3.3V -5%/+10%	2.5V -5% to V <sub>DD</sub>
Industrial	-40°C to +85°C		

**Electrical Characteristics Over the Operating Range<sup>[8, 9]</sup>**

Parameter	Description	Test Conditions	Min.	Max.	Unit
V <sub>DD</sub>	Power Supply Voltage		3.135	3.6	V
V <sub>DDQ</sub>	I/O Supply Voltage		2.375	V <sub>DD</sub>	V
V <sub>OH</sub>	Output HIGH Voltage	V <sub>DDQ</sub> = 3.3V, V <sub>DD</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		V
		V <sub>DDQ</sub> = 2.5V, V <sub>DD</sub> = Min., I <sub>OH</sub> = -2.0 mA	2.0		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>DDQ</sub> = 3.3V, V <sub>DD</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4	V
		V <sub>DDQ</sub> = 2.5V, V <sub>DD</sub> = Min., I <sub>OL</sub> = 2.0 mA		0.4	V
V <sub>IH</sub>	Input HIGH Voltage <sup>[8]</sup>	V <sub>DDQ</sub> = 3.3V	2.0	V <sub>DD</sub> + 0.3V	V
		V <sub>DDQ</sub> = 2.5V	1.7	V <sub>DD</sub> + 0.3V	V
V <sub>IL</sub>	Input LOW Voltage <sup>[8]</sup>	V <sub>DDQ</sub> = 3.3V	-0.3	0.8	V
		V <sub>DDQ</sub> = 2.5V	-0.3	0.7	V
I <sub>X</sub>	Input Load Current except ZZ and MODE	GND ≤ V <sub>I</sub> ≤ V <sub>DDQ</sub>	-5	5	μA
		Input Current of MODE	Input = V <sub>SS</sub>	-30	
	Input Current of ZZ	Input = V <sub>DD</sub>		5	μA
		Input = V <sub>SS</sub>	-5		μA
	Input = V <sub>DD</sub>		30	μA	
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>DDQ</sub> , Output Disabled	-5	5	μA
I <sub>DD</sub>	V <sub>DD</sub> Operating Supply Current	V <sub>DD</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>CYC</sub>	4-ns cycle, 250 MHz	325	mA
			4.4-ns cycle, 225 MHz	290	mA
			5-ns cycle, 200 MHz	265	mA
			6-ns cycle, 166 MHz	240	mA
			7.5-ns cycle, 133 MHz	225	mA
			10-ns cycle, 100 MHz	205	mA
I <sub>SB1</sub>	Automatic CE Power-down Current—TTL Inputs	V <sub>DD</sub> = Max., Device Deselected, V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub> = 1/t <sub>CYC</sub>	4-ns cycle, 250 MHz	120	mA
			4.4-ns cycle, 225 MHz	115	mA
			5-ns cycle, 200 MHz	110	mA
			6-ns cycle, 166 MHz	100	mA
			7.5-ns cycle, 133 MHz	90	mA
			10-ns cycle, 100 MHz	80	mA

Shaded areas contain advance information.

**Notes:**

- Overshoot: V<sub>IH</sub>(AC) < V<sub>DD</sub> + 1.5V (Pulse width less than t<sub>CYC</sub>/2), undershoot: V<sub>IL</sub>(AC) > -2V (Pulse width less than t<sub>CYC</sub>/2).
- T<sub>Power-up</sub>: Assumes a linear ramp from 0v to V<sub>DD</sub>(min.) within 200 ms. During this time V<sub>IH</sub> ≤ V<sub>DD</sub> and V<sub>DDQ</sub> ≤ V<sub>DD</sub>.



**Electrical Characteristics** Over the Operating Range<sup>[8, 9]</sup>

Parameter	Description	Test Conditions		Min.	Max.	Unit
I <sub>SB2</sub>	Automatic CE Power-down Current—CMOS Inputs	V <sub>DD</sub> = Max., Device Deselected, V <sub>IN</sub> ≤ 0.3V or V <sub>IN</sub> ≥ V <sub>DDQ</sub> - 0.3V, f = 0	All speeds		40	mA
I <sub>SB3</sub>	Automatic CE Power-down Current—CMOS Inputs	V <sub>DD</sub> = Max., Device Deselected, or V <sub>IN</sub> ≤ 0.3V or V <sub>IN</sub> ≥ V <sub>DDQ</sub> - 0.3V, f = f <sub>MAX</sub> = 1/t <sub>CYC</sub>	4-ns cycle, 250 MHz		105	mA
			4.4-ns cycle, 225 MHz		100	mA
			5-ns cycle, 200 MHz		95	mA
			6-ns cycle, 166 MHz		85	mA
			7.5-ns cycle, 133 MHz		75	mA
			10-ns cycle, 100 MHz		65	mA
I <sub>SB4</sub>	Automatic CE Power-down Current—TTL Inputs	V <sub>DD</sub> = Max., Device Deselected, V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = 0	All speeds		45	mA

**Thermal Characteristics**<sup>[10]</sup>

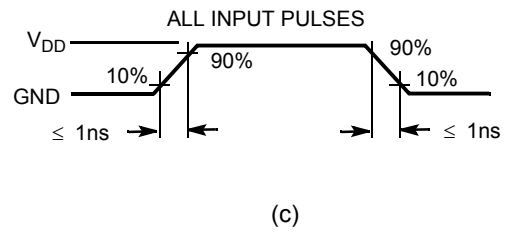
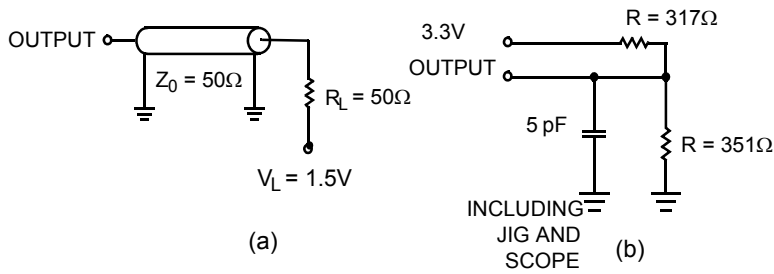
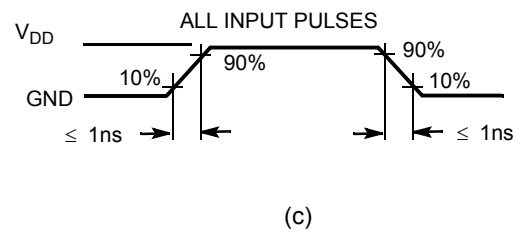
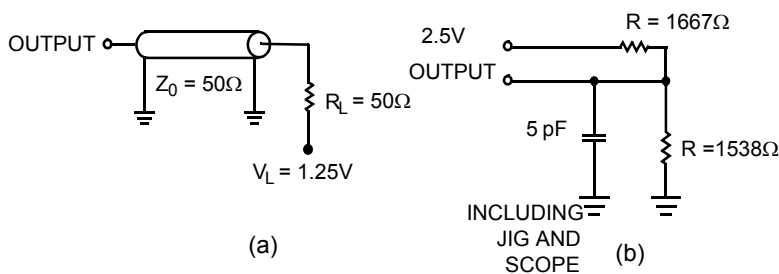
Parameter	Description	Test Conditions	TQFP Package	Unit
Θ <sub>JA</sub>	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	41.83	°C/W
Θ <sub>JC</sub>	Thermal Resistance (Junction to case)		9.99	°C/W

**Capacitance**<sup>[10]</sup>

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>DD</sub> = 3.3V, V <sub>DDQ</sub> = 3.3V	5	pF
C <sub>CLK</sub>	Clock Input Capacitance		5	pF
C <sub>I/O</sub>	Input/Output Capacitance		5	pF

**Note:**

10. Tested initially and after any design or process change that may affect these parameters.

**AC Test Loads and Waveforms**
**3.3V I/O Test Load**

**2.5V I/O Test Load**


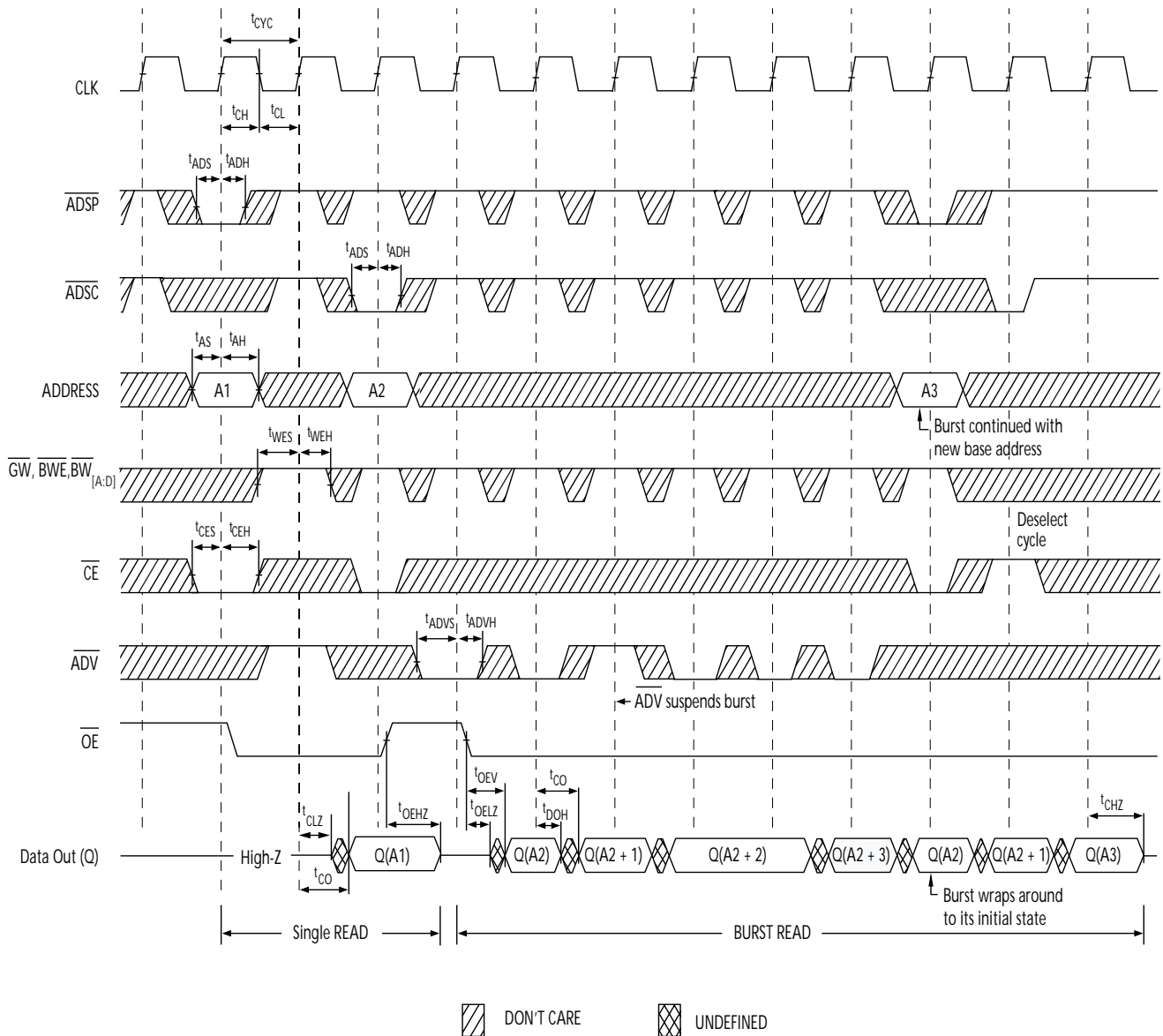
**Switching Characteristics** Over the Operating Range [15, 16]

Parameter	Description	250 MHz		225 MHz		200 MHz		166 MHz		133 MHz		100 MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{POWER}$	$V_{DD}$ (Typical) to the first Access <sup>[11]</sup>	1.0		1.0		1.0		1.0		1.0		1.0		ms
<b>Clock</b>														
$t_{CYC}$	Clock Cycle Time	4.0		4.4		5.0		6.0		7.5		10		ns
$t_{CH}$	Clock HIGH	1.7		2.0		2.0		2.5		3.0		3.5		ns
$t_{CL}$	Clock LOW	1.7		2.0		2.0		2.5		3.0		3.5		ns
<b>Output Times</b>														
$t_{CO}$	Data Output Valid After CLK Rise		2.6		2.6		2.8		3.5		4.0		4.5	ns
$t_{DOH}$	Data Output Hold After CLK Rise	1.0		1.0		1.0		2.0		2.0		2.0		ns
$t_{CLZ}$	Clock to Low-Z <sup>[12, 13, 14]</sup>	0		0		0		0		0		0		ns
$t_{CHZ}$	Clock to High-Z <sup>[12, 13, 14]</sup>		2.6		2.6		2.8		3.5		4.0		4.5	ns
$t_{OEV}$	$\overline{OE}$ LOW to Output Valid		2.6		2.6		2.8		3.5		4.5		4.5	ns
$t_{OELZ}$	$\overline{OE}$ LOW to Output Low-Z <sup>[12, 13, 14]</sup>	0		0		0		0		0		0		ns
$t_{OEHZ}$	$\overline{OE}$ HIGH to Output High-Z <sup>[12, 13, 14]</sup>		2.6		2.6		2.8		3.5		4.0		4.5	ns
<b>Set-up Times</b>														
$t_{AS}$	Address Set-up Before CLK Rise	0.8		1.2		1.2		1.5		1.5		1.5		ns
$t_{ADS}$	$\overline{ADSC}$ , $\overline{ADSP}$ Set-up Before CLK Rise	0.8		1.2		1.2		1.5		1.5		1.5		ns
$t_{ADVS}$	$\overline{ADV}$ Set-up Before CLK Rise	0.8		1.2		1.2		1.5		1.5		1.5		ns
$t_{WES}$	$\overline{GW}$ , $\overline{BWE}$ , $\overline{BW}_{[A:D]}$ Set-up Before CLK Rise	0.8		1.2		1.2		1.5		1.5		1.5		ns
$t_{DS}$	Data Input Set-up Before CLK Rise	0.8		1.2		1.2		1.5		1.5		1.5		ns
$t_{CES}$	Chip Enable Set-up Before CLK Rise	0.8		1.2		1.2		1.5		1.5		1.5		ns
<b>Hold Times</b>														
$t_{AH}$	Address Hold After CLK Rise	0.4		0.5		0.5		0.5		0.5		0.5		ns
$t_{ADH}$	$\overline{ADSP}$ , $\overline{ADSC}$ Hold After CLK Rise	0.4		0.5		0.5		0.5		0.5		0.5		ns
$t_{ADVH}$	$\overline{ADV}$ Hold After CLK Rise	0.4		0.5		0.5		0.5		0.5		0.5		ns
$t_{WEH}$	$\overline{GW}$ , $\overline{BWE}$ , $\overline{BW}_{[A:D]}$ Hold After CLK Rise	0.4		0.5		0.5		0.5		0.5		0.5		ns
$t_{DH}$	Data Input Hold After CLK Rise	0.4		0.5		0.5		0.5		0.5		0.5		ns
$t_{CEH}$	Chip Enable Hold After CLK Rise	0.4		0.5		0.5		0.5		0.5		0.5		ns

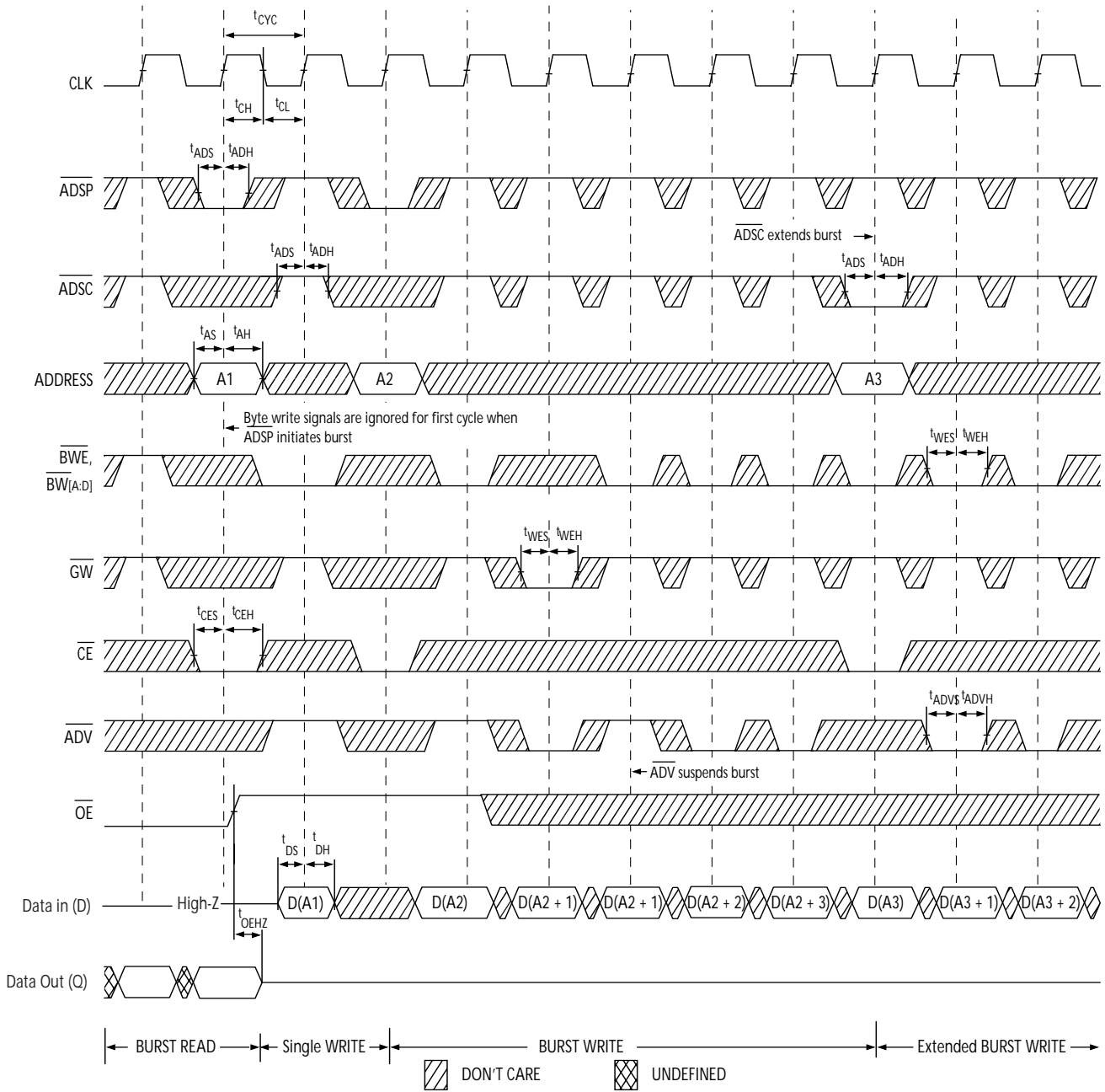
Shaded areas contain advance information.

**Notes:**

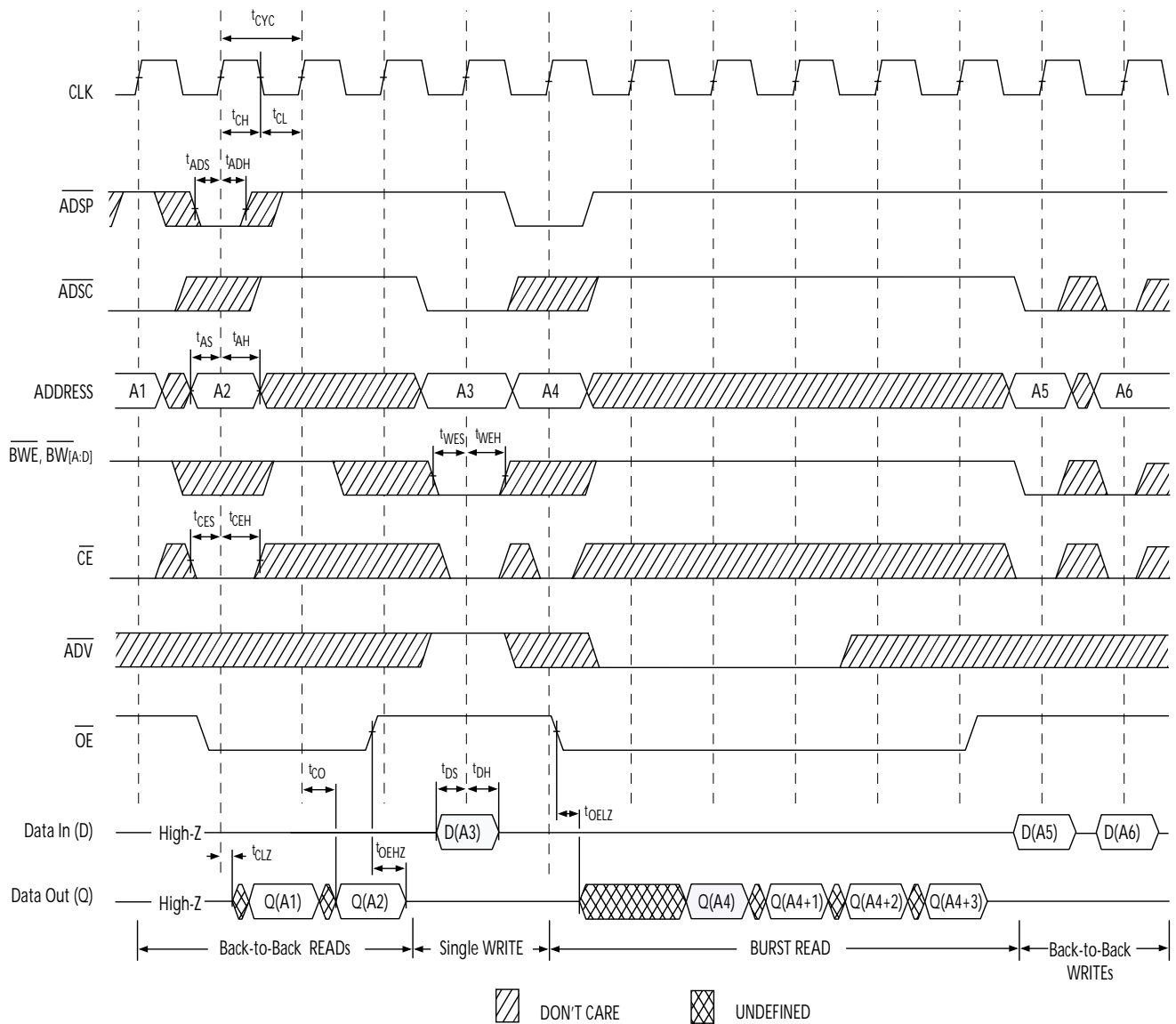
- This part has a voltage regulator internally;  $t_{POWER}$  is the time that the power needs to be supplied above  $V_{DD}$  minimum initially before a read or write operation can be initiated.
- $t_{CHZ}$ ,  $t_{CLZ}$ ,  $t_{OELZ}$ , and  $t_{OEHZ}$  are specified with AC test conditions shown in part (b) of AC Test Loads. Transition is measured  $\pm 200$  mV from steady-state voltage.
- At any given voltage and temperature,  $t_{OEHZ}$  is less than  $t_{OELZ}$  and  $t_{CHZ}$  is less than  $t_{CLZ}$  to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High-Z prior to Low-Z under the same system conditions.
- This parameter is sampled and not 100% tested.
- Timing reference level is 1.5V when  $V_{DDQ} = 3.3V$  and is 1.25V when  $V_{DDQ} = 2.5V$ .
- Test conditions shown in (a) of AC Test Loads unless otherwise noted.

**Switching Waveforms**
**Read Timing<sup>[17]</sup>**

**Note:**

 17. On this diagram, when  $\overline{CE}$  is LOW:  $\overline{CE}_1$  is LOW,  $CE_2$  is HIGH and  $\overline{CE}_3$  is LOW. When  $\overline{CE}$  is HIGH:  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW or  $\overline{CE}_3$  is HIGH.

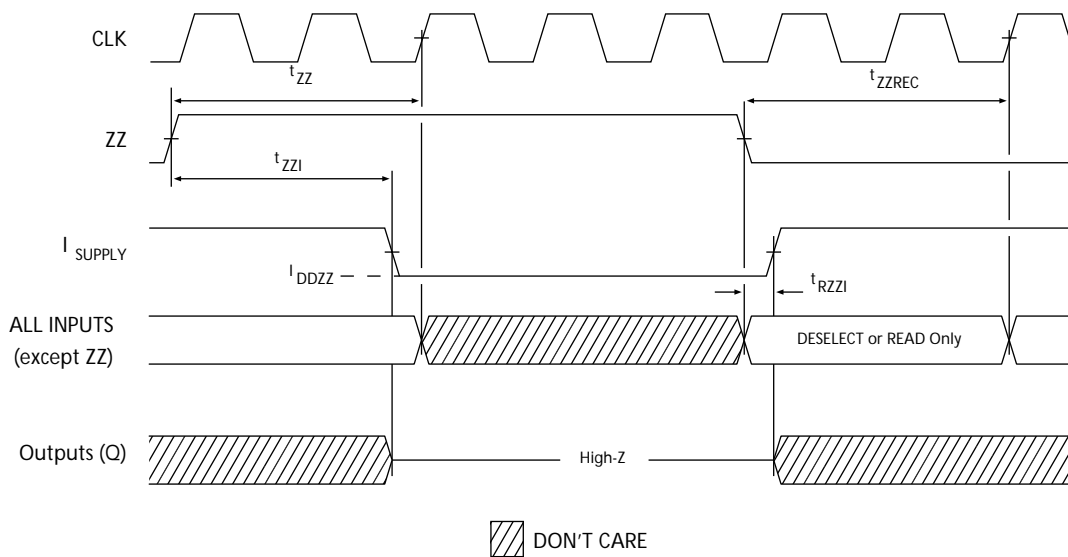
**Switching Waveforms (continued)**
**Write Timing<sup>[17, 18]</sup>**

**Note:**

18. Full width write can be initiated by either  $\overline{GW}$  LOW; or by  $\overline{GW}$  HIGH,  $\overline{BWE}$  LOW and  $\overline{BW}_{[A:D]}$  LOW.

**Switching Waveforms (continued)**
**Read/Write Timing<sup>[17, 19, 20]</sup>**

**Notes:**

19. The data bus (Q) remains in high-Z following a WRITE cycle, unless a new read access is initiated by  $\overline{ADSP}$  or  $\overline{ADSC}$ .
20.  $\overline{GW}$  is HIGH.

**Switching Waveforms** (continued)

**ZZ Mode Timing** [21, 22]

**Notes:**

21. Device must be deselected when entering ZZ mode. See truth table for all possible signal conditions to deselect the device.

22. DQs are in high-Z when exiting ZZ sleep mode.

**Ordering Information**

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
250	CY7C1340F-250AC	A101	100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack	Commercial
	CY7C1340F-250AI	A101	100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack	Industrial
225	CY7C1340F-225AC	A101	100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack	Commercial
	CY7C1340F-225AI	A101	100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack	Industrial
200	CY7C1340F-200AC	A101	100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack	Commercial
	CY7C1340F-200AI	A101	100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack	Industrial
166	CY7C1340F-166AC	A101	100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack	Commercial
	CY7C1340F-166AI	A101	100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack	Industrial
133	CY7C1340F-133AC	A101	100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack	Commercial
	CY7C1340F-133AI	A101	100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack	Industrial
100	CY7C1340F-100AC	A101	100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack	Commercial
	CY7C1340F-100AI	A101	100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack	Industrial

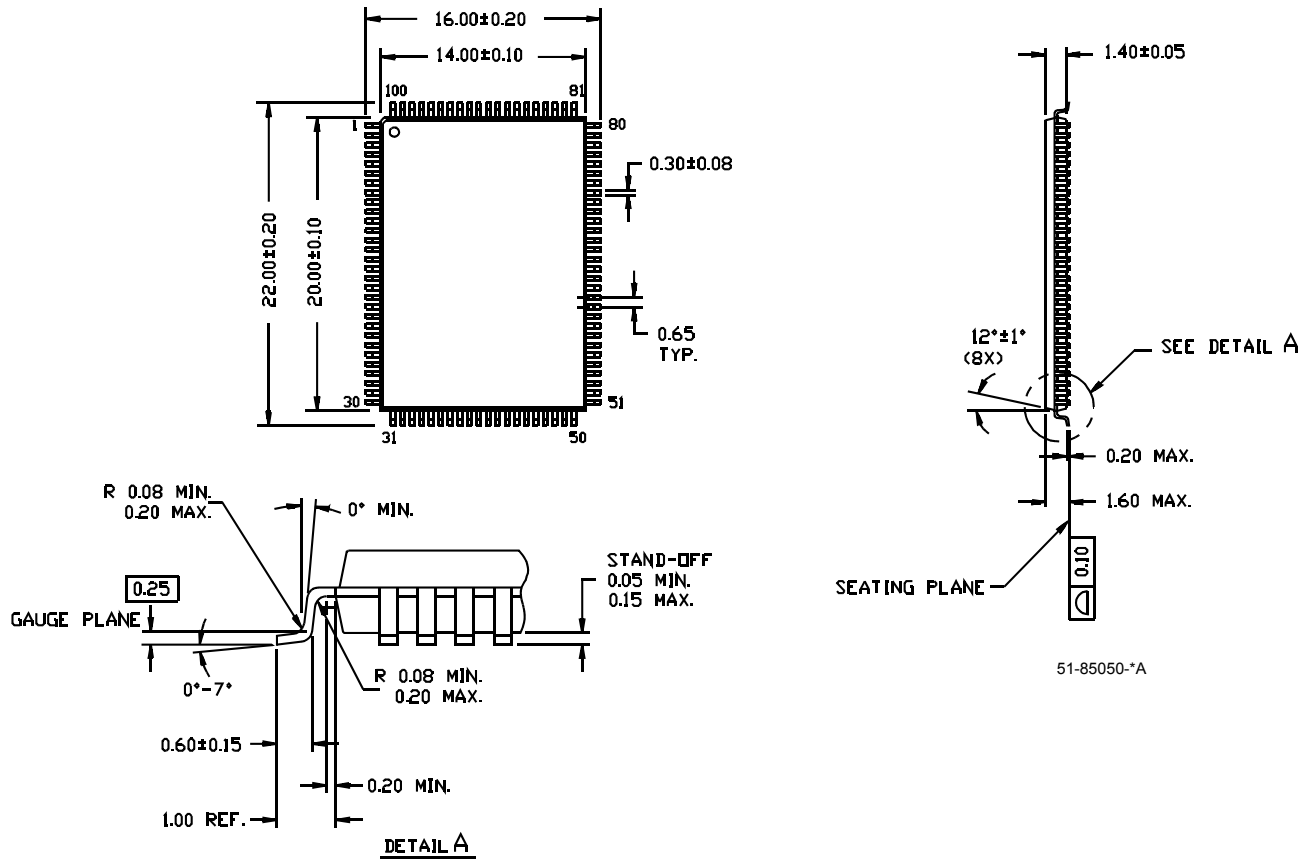
Shaded area contains advance information.

Please contact your local Cypress sales representative for availability of these parts.

Package Diagram

100-pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A101

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**Document History Page**

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<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	119827	12/16/02	HGK	New Data Sheet
*A	200143	See ECN	SWI	Final Data Sheet