CY7C197BN

256 Kb (256K x 1) Static RAM

Features

- Fast access time: 12 ns
- Wide voltage range: 5.0V ± 10% (4.5V to 5.5V)
- CMOS for optimum speed and power
- TTL compatible inputs and outputs
- Available in 24-lead DIP and 24-lead SOJ

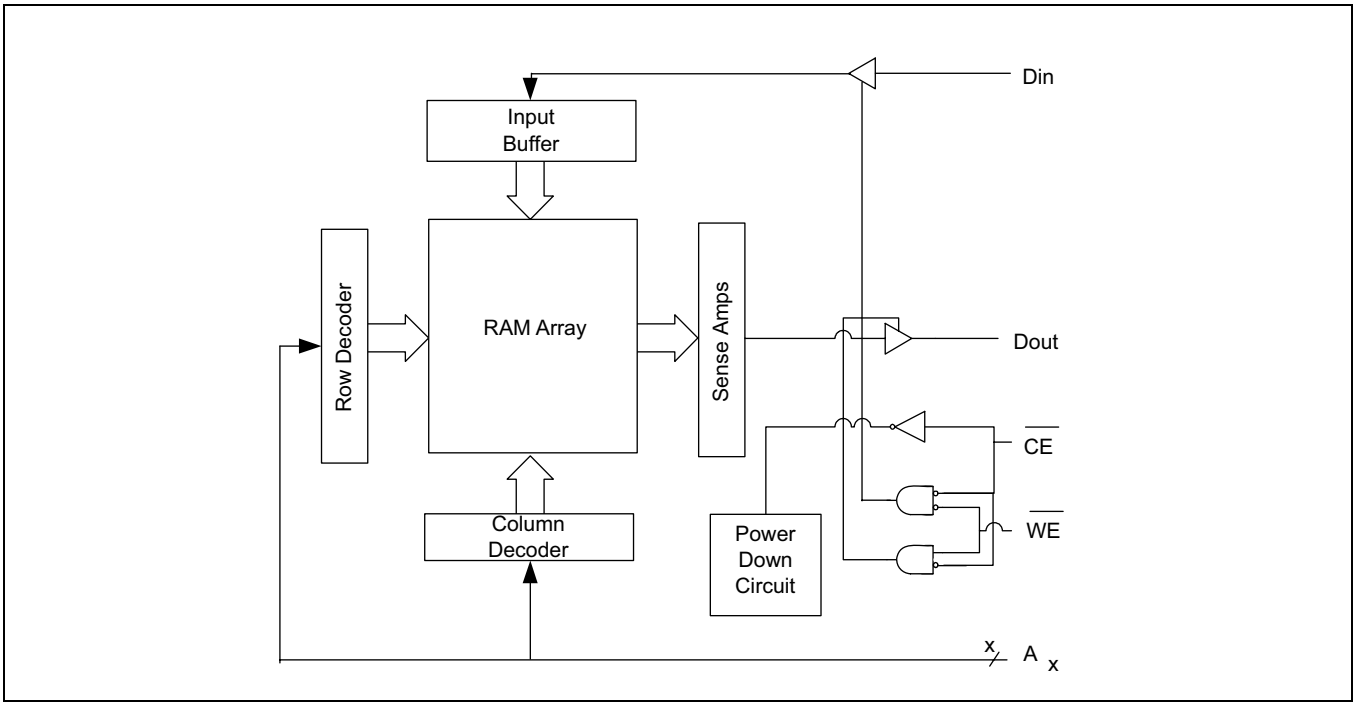
General Description [1]

The CY7C197BN is a high performance CMOS Asynchronous SRAM organized as 256K × 1 bits that supports an asynchronous memory interface. The device features an automatic power down feature that significantly reduces power consumption when deselected.

See the "Truth Table" on page 7 for a complete description of Read and Write modes.

The CY7C197BN is available in 24-lead DIP and 24-lead SOJ package(s).

Logic Block Diagram



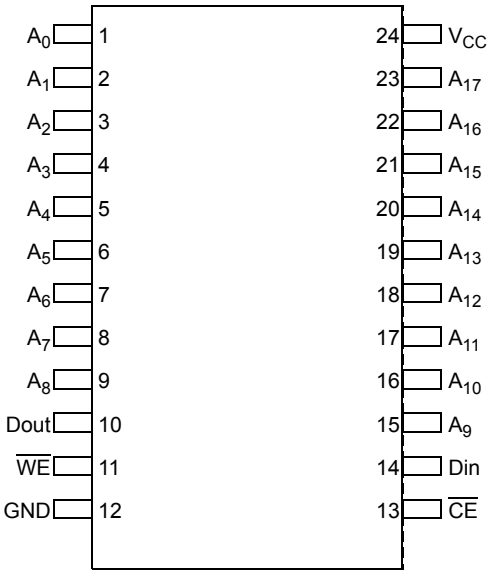
Product Portfolio

	-12	-15	-25	Unit
Maximum Access Time	12	15	25	ns
Maximum Operating Current	150	150	95	mA
Maximum CMOS Standby Current	10	10	10	mA

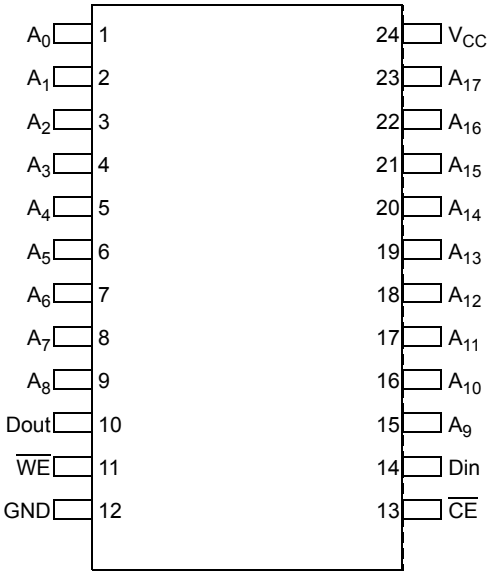
Notes
1. For best practice recommendations, refer to the Cypress application note *System Design Guidelines* on www.cypress.com.

Pin Layout and Specification

24-lead DIP (6.6 × 31.8 × 3.5 mm)



24-lead SOJ (8 × 15 × 3.5 mm)



Pin Description

Pin	Type	Description	DIP	SOJ
A_X	Input	Address Inputs	1, 2, 3, 4, 5, 6, 7, 8, 9, 15, 16, 17, 18, 19, 20, 21, 22, 23	1, 2, 3, 4, 5, 6, 7, 8, 9, 15, 16, 17, 18, 19, 20, 21, 22, 23
$\overline{CE}$	Control	Chip Enable	13	13
Din	Input	Data Input Pins	14	14
Dout	Output	Data Output Pins	10	10
V_{CC}	Supply	Power (5.0V)	24	24
$\overline{WE}$	Control	Write Enable	11	11

Maximum Ratings

Exceeding the maximum rating may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage on V_{CC} to Relative GND..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[2] .....–0.5V to V_{CC} +0.5V

DC Input Voltage[2].....–0.5V to V_{CC} +0.5V

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage.....2001V (per MIL-STD-883, Method 3015)

Latch Up Current .....>200 mA

Operating Range

Range	Ambient Temperature[3]	V_{CC}
Commercial	0°C to 70°C	5.0V ± 10%

DC Electrical Characteristics[2]

Parameter	Description	Condition	12 and 15 ns		25 ns		Unit
			Min	Max	Min	Max	
V_{IH}	Input HIGH Voltage		2.2	V_{CC}+0.3	2.2	V_{CC}+0.3	V
V_{IL}	Input LOW Voltage		–0.3	0.8	–0.3	0.8	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = –4.0 mA	2.4	–	2.4	–	V
V_{OL}	Output LOW Voltage	V_{CC} = Min, Iol = 8.0 mA	–	0.4	–	0.4	V
I_{OZ}	Output Leakage Current	GND ≤ Vi ≤ V_{CC}, Output Disabled	–5	+5	–5	+5	µA
I_{IX}	Input Leakage Current	GND ≤ Vi ≤ V_{CC}	–5	+5	–5	+5	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max, I_{OUT} = 0 mA, f = F_{MAX} = $1/t_{RC}$	–	150	–	95	mA
I_{SB1}	Automatic $\overline{CE}$ Power Down Current TTL Inputs	V_{CC} = Max, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = F_{MAX}	–	30	–	30	mA
I_{SB2}	Automatic $\overline{CE}$ Power Down Current CMOS Inputs	V_{CC} = Max, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V or V_{IN} < 0.3V, f = 0	–	10	–	10	mA

Capacitance[4]

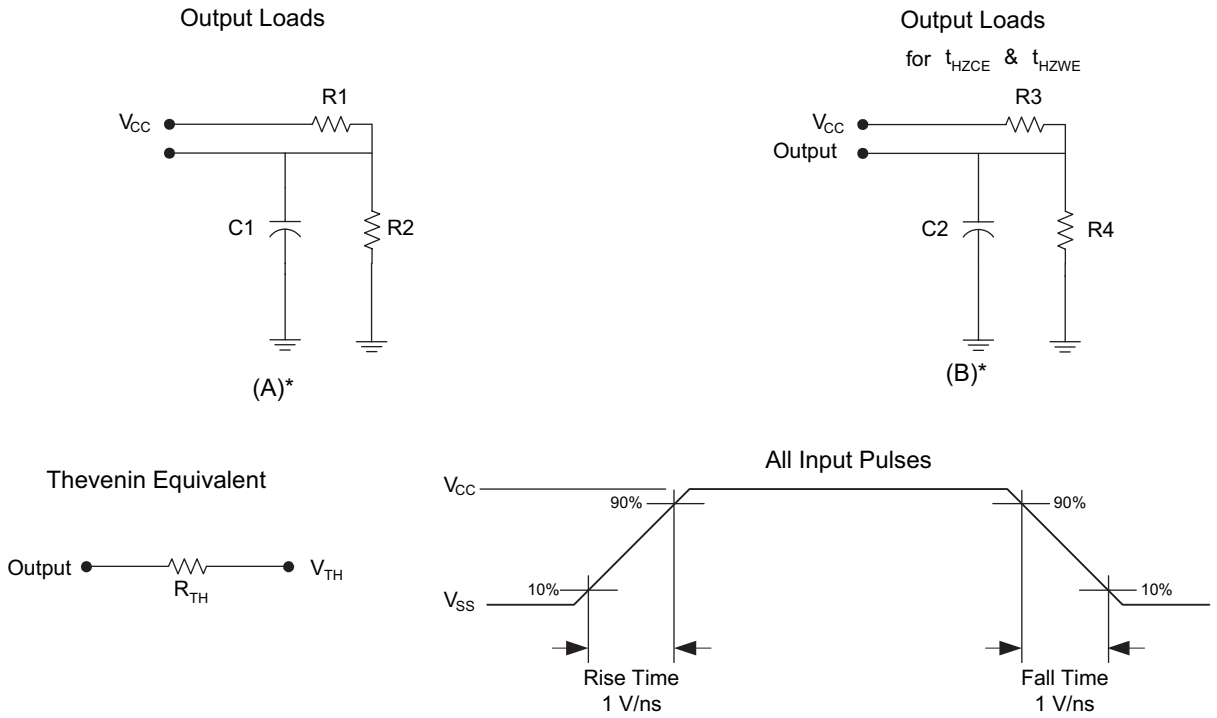
Parameter	Description	Conditions	Max (ALL – PACKAGES)	Unit
C_{IN}	Input Capacitance	T_A = 25C, f = 1 MHz, V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		10	

Thermal Resistance[4]

Parameter	Description	Conditions	24 DIP	24 SOJ	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 x 4.5 square inches, two-layer printed circuit board	75.69	84.15	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		33.80	37.56	

Notes
2. V_{IL}(min) = –2.0V for pulse durations of less than 20 ns.
3. T_A is the "instant on" case temperature
4. Tested initially and after any design or process change that may affect these parameters

AC Test Loads[5]



* including scope and jig capacitance

AC Test Conditions

Parameter	Description	Nom.	Unit
C1	Capacitor 1	30	pF
C2	Capacitor 2	5	
R1	Resistor 1	480	Ω
R2	Resistor 2	255	
R3	Resistor 3	480	
R4	Resistor 4	255	
R_{TH}	Resistor Thevenin	167	
V_{TH}	Voltage Thevenin	1.73	V

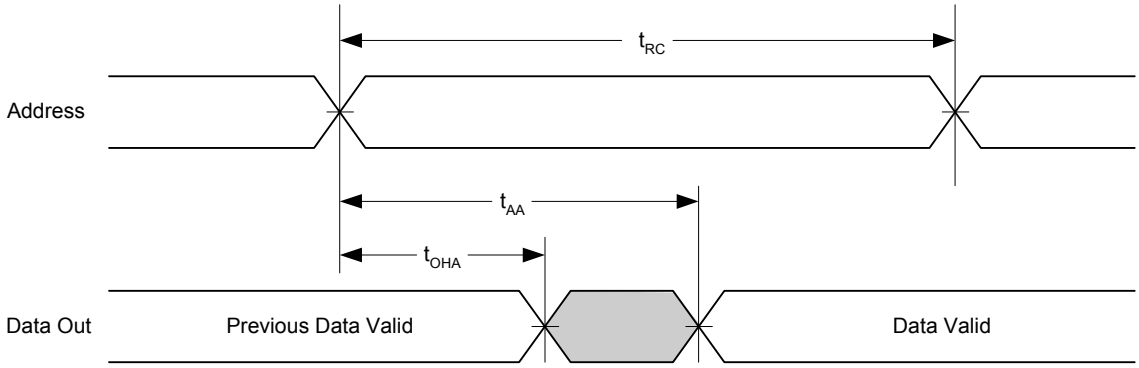
Note
5. Test Conditions assume a transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V

AC Electrical Characteristics[4, 6, 7, 8]

Parameter	Description	12 ns		15 ns		25 ns		Unit
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	12	–	15	–	25	–	ns
t_{AA}	Address to Data Valid	–	12	–	15	–	25	ns
t_{OHA}	Data Hold from Address Change	3	–	3	–	3	–	ns
t_{ACE}	$\overline{CE}$ to Data Valid	–	12	–	15	–	25	ns
t_{LZCE}	$\overline{CE}$ to Low Z	3	–	3	–	3	–	ns
t_{HZCE}	$\overline{CE}$ to High Z	–	5	–	5	–	11	ns
t_{PU}	$\overline{CE}$ to Power-up	0	–	0	–	0	–	ns
t_{PD}	$\overline{CE}$ to Power-down	–	12	–	15	–	20	ns
t_{WC}	Write Cycle Time	12	–	15	–	25	–	ns
t_{SCE}	$\overline{CE}$ to Write End	9	–	9	–	20	–	ns
t_{AW}	Address Set-up to Write End	9	–	10	–	20	–	ns
t_{HA}	Address Hold from Write End	0	–	0	–	0	–	ns
t_{SA}	Address Set-up to Write Start	0	–	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ Pulse Width	8	–	9	–	20	–	ns
t_{SD}	Data Set-Up to Write End	8	–	9	–	15	–	ns
t_{HD}	Data Hold from Write End	0	–	0	–	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z	–	7	–	7	–	11	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	2	–	2	–	3	–	ns

Timing Waveforms

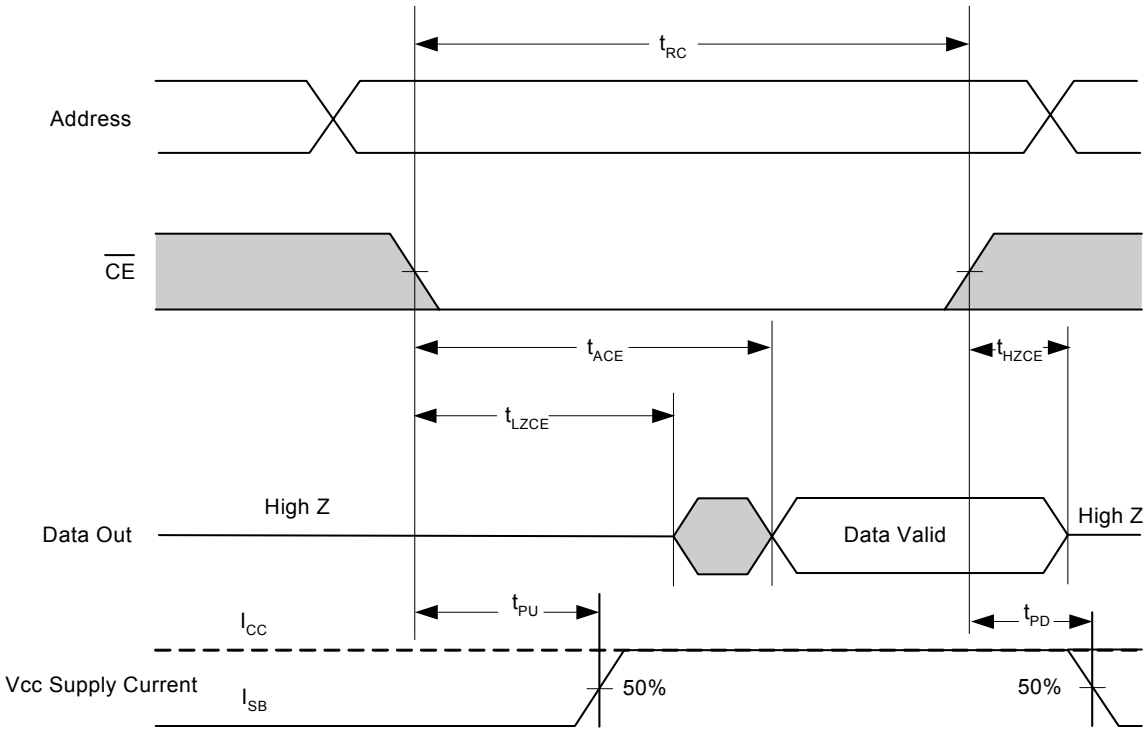
Read Cycle No. 1[9, 10]



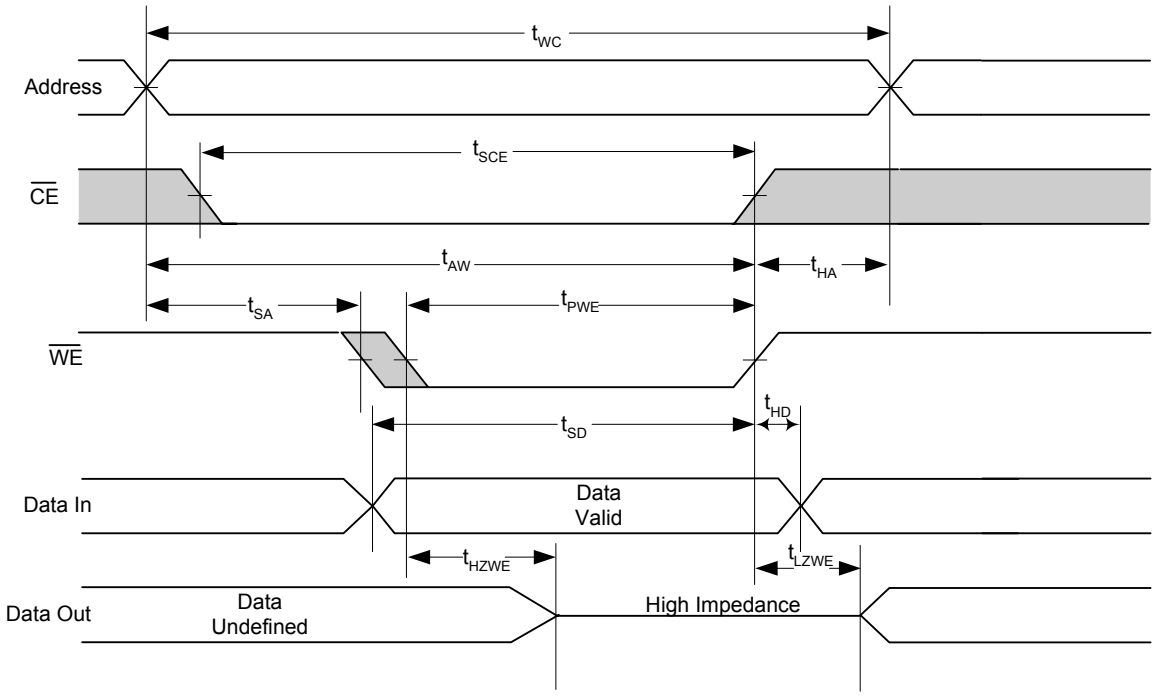
Notes
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, and t_{HZWE} is less than t_{LZWE} for any given device.
7. The internal Write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the Write. The input data setup and hold timing should be referenced to the leading edge of the signal that terminates the write.
8. t_{HZCE}, t_{HZWE} are specified as in part (b) of the "AC Test Loads[5]" on page 4. Transitions are measured ±200 mV from steady state voltage.
9. Device is continuously selected. $\overline{CE}$ = V_{IL}.
10. $\overline{WE}$ is HIGH for Read Cycle.

Timing Waveforms (continued)

Read Cycle No. 2[4, 11, 12]



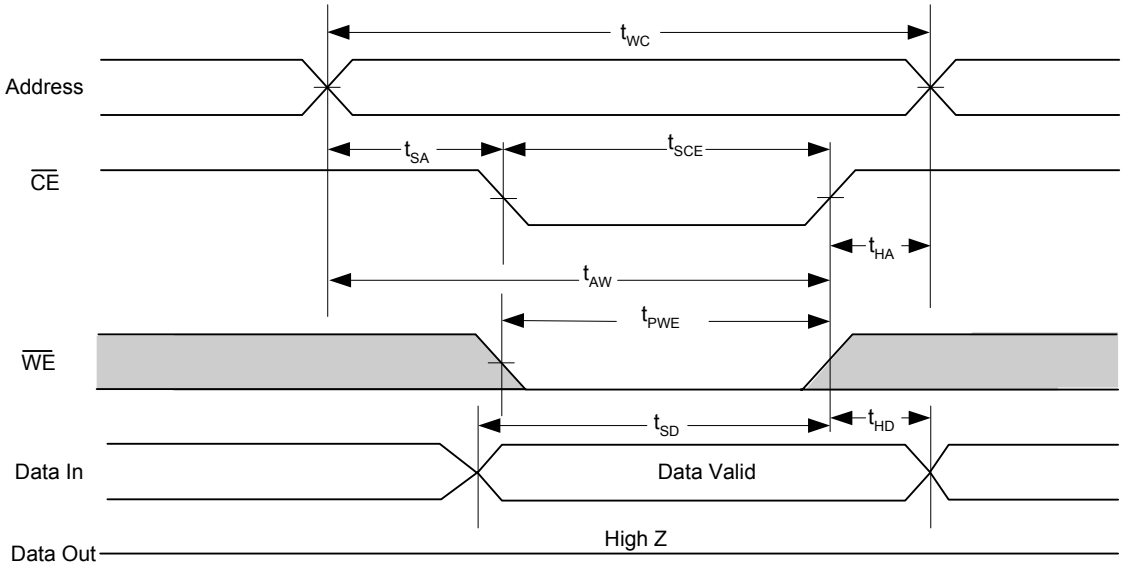
Write Cycle No. 1 ($\overline{WE}$ Controlled)[4, 13]



Notes
11. $\overline{WE}$ is HIGH in read cycle.
12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
13. The minimum write cycle time is the sum of t_{HZWE} and t_{SD}.

Timing Waveforms (continued)

Write Cycle No. 2 ($\overline{CE}$ Controlled)[14, 15]



Truth Table

$\overline{CE}$	$\overline{WE}$	I/Ox	Mode	Power
H	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	Data Out	Read	Active (I_{CC})
L	L	Data In	Write	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
12	CY7C197BN-12VC	51-85030	24-lead SOJ (8 x 15 x 3.5 mm)	Commercial
15	CY7C197BN-15VC	51-85030	24-lead SOJ (8 x 15 x 3.5 mm)	Commercial
25	CY7C197BN-25PC	51-85013	24-lead DIP (6.6 x 31.8 x 3.5 mm)	Commercial

Please contact local sales representative regarding availability of these parts.

Notes
14. This cycle is $\overline{CE}$ controlled.
15. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high impedance state.

Package Diagrams

Figure 1. 24-lead (300-mil) SOJ (51-85030)

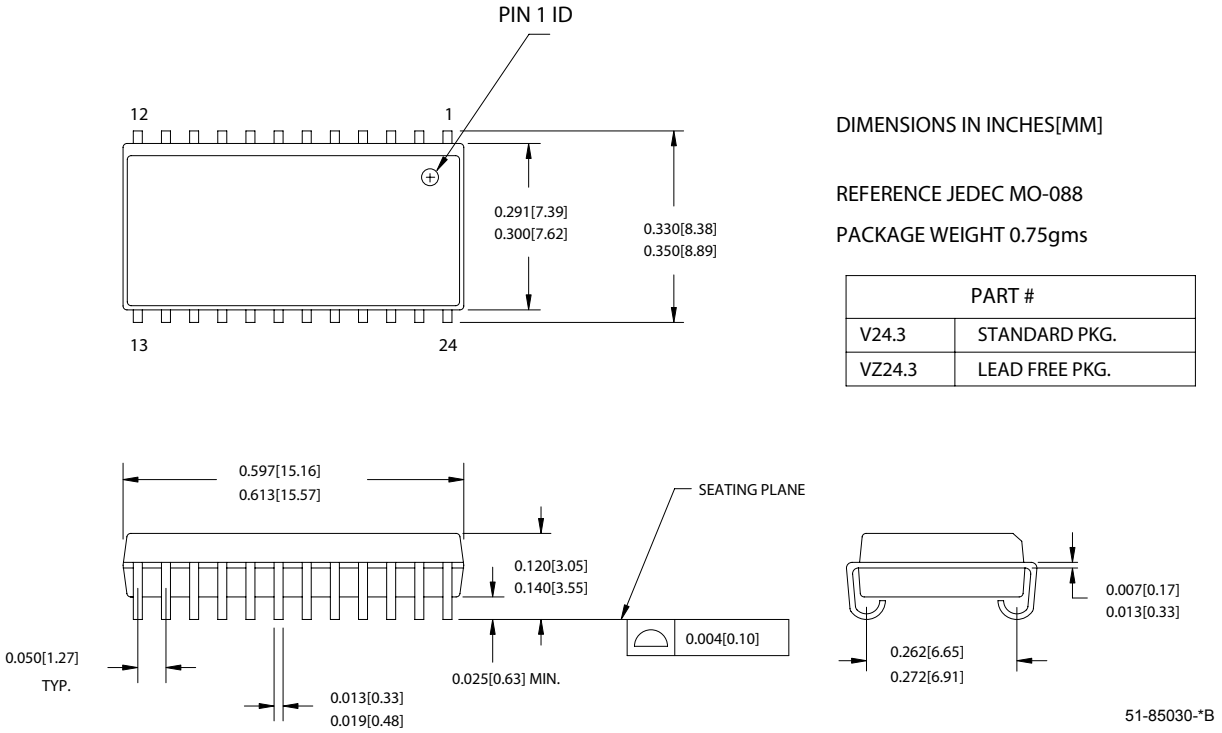
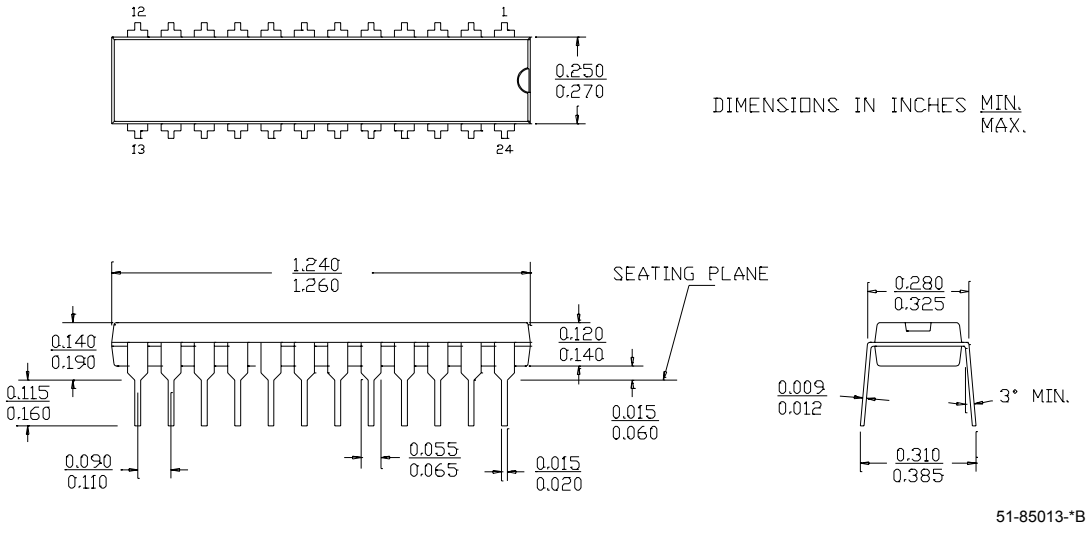


Figure 2. 24-lead DIP (6.6 x 31.8 x 3.5 mm) (51-85013)



Document History Page

Document Title: CY7C197BN 256 Kb (256K x 1) Static RAM Document Number: 001-06447				
REV.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	901742	See ECN	NXR	New Data Sheet