PRELIMINARY

CY7C197D

256K (256K x 1) Static RAM

Features

- **Pin- and function-compatible with CY7C197B**
- **High speed**
  - **— t_{AA} = 10 ns**
- **CMOS for optimum speed/power**
- **Low active power**
  - **— I_{CC} = 60 mA @ 10 ns**
- **Low CMOS standby power**
  - **— I_{SB2} = 3 mA**
- **TTL-compatible inputs and outputs**
- **Data retention at 2.0V**
- **Automatic power-down when deselected**
- **Available in Pb-Free Packages**

Functional Description[1]

The CY7C197D is a high-performance CMOS static RAM organized as 256K words by 1 bit. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}$) and three-state drivers. The CY7C197D has an automatic power-down feature, reducing the power consumption when deselected.

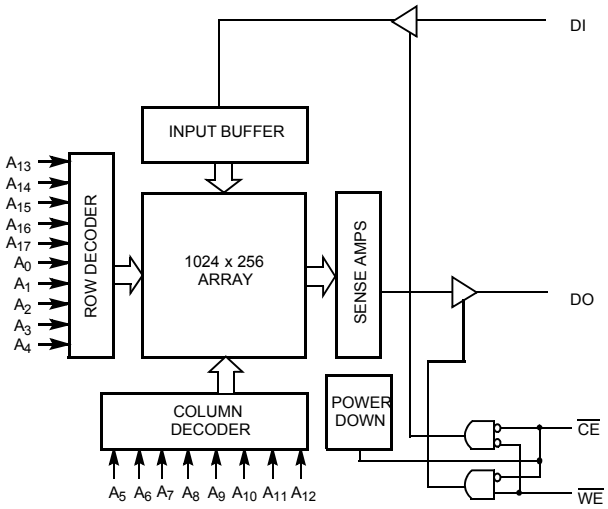
Writing to the device is accomplished when the Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs are both LOW. Data on the input pin (D_{IN}) is written into the memory location specified on the address pins (A_0 through A_{17}).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) LOW while Write Enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data output (D_{OUT}) pin.

The output pin stays in a high-impedance state when Chip Enable ($\overline{CE}$) is HIGH or Write Enable ($\overline{WE}$) is LOW.

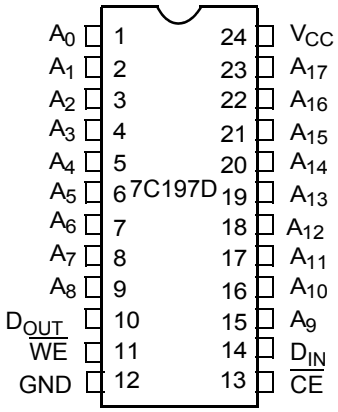
The CY7C197D is available in standard 24-Lead DIP and SOJ Pb-Free Packages.

Logic Block Diagram



Pin Configurations

DIP/SOJ
Top View



Selection Guide

	CY7C197D-10	CY7C197D-12	CY7C197D-15
Maximum Access Time (ns)	10	12	15
Maximum Operating Current (mA)	60	50	40
Maximum Standby Current (mA)	3	3	3

Note:
1. For guidelines on SRAM system design, please refer to the “System Design Guidelines” Cypress application note, available on the internet at www.cypress.com.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12)..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High-Z State[2] ..... –0.5V to V_{CC} + 0.5V

DC Input Voltage[2]..... –0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch-up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	–40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	7C197D-10		7C197D-12		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA	2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC} + 0.3V	2.0	V_{CC} +0.3V	V
V_{IL}	Input LOW Voltage[2]		–0.5	0.8	–0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	–1	+1	–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	–1	+1	–1	+1	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND		–300		–300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$		60		50	mA
I_{SB1}	Automatic $\overline{CE}$ Power-down Current—TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}		10		10	mA
I_{SB2}	Automatic $\overline{CE}$ Power-down Current—CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V or V_{IN} < 0.3V		3		3	mA

Parameter	Description	Test Conditions	7C197D-15		Unit
			Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC} + 0.3V	V
V_{IL}	Input LOW Voltage[2]		–0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	–1	+1	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND		–300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$		40	mA
I_{SB1}	Automatic $\overline{CE}$ Power Down Current—TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}		10	mA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current—CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V or V_{IN} < 0.3V		3	mA

Capacitance[4]

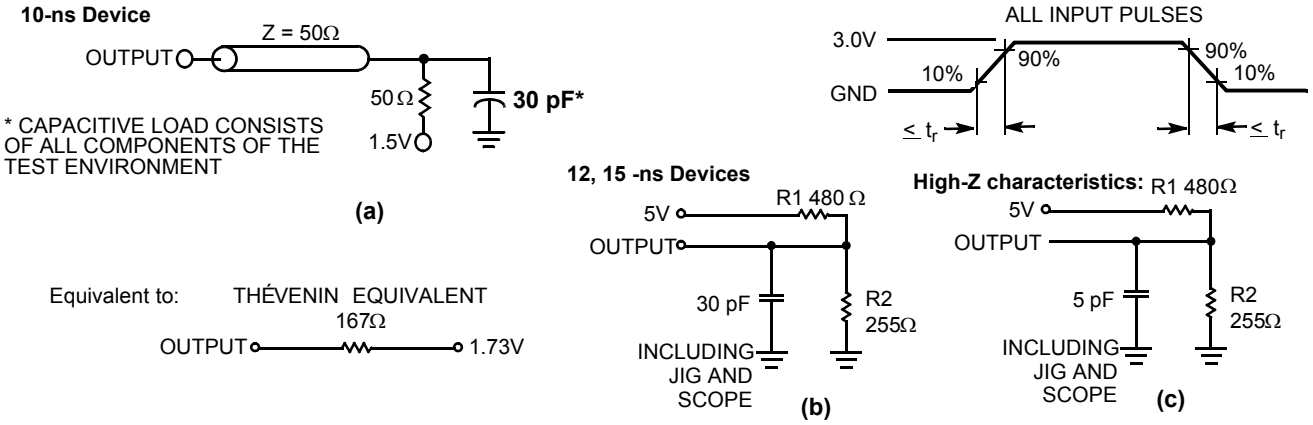
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		10	pF

Notes:
2. V_{IL} (min.) = –2.0V and V_{IH}(max) = V_{CC} + 2V for pulse durations of less than 20 ns.
3. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.

Thermal Resistance[4]

Parameter	Description	Test Conditions	All-Packages	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)[4]	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	TBD	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)[4]		TBD	°C/W

AC Test Loads and Waveforms[5]



Switching Characteristics Over the Operating Range[6]

Parameter	Description	7C197D-10		7C197D-12		7C197D-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{power}[7]	V_{CC}(typical) to the first access	100		100		100		µs
t_{RC}	Read Cycle Time	10		12		15		ns
t_{AA}	Address to Data Valid		10		12		15	ns
t_{OHA}	Output Hold from Address Change	3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		10		12		15	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8]	3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[8, 9]		5		5		7	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		10		12		15	ns
t_{SCE}	$\overline{CE}$ LOW to Write End	8		9		10		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
Write Cycle[10]								
t_{WC}	Write Cycle Time	10		12		15		ns
t_{AW}	Address Set-Up to Write End	7		9		10		ns

Notes:
5. t_r = ≤ 3 ns for all speeds.
6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access can be performed.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE} for any given device.
9. t_{HZCE} and t_{HZWE} are specified with C_L = 5 pF as in part (b) in AC Test Loads and Waveforms. Transition is measured ±200 mV from steady-state voltage.
10. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

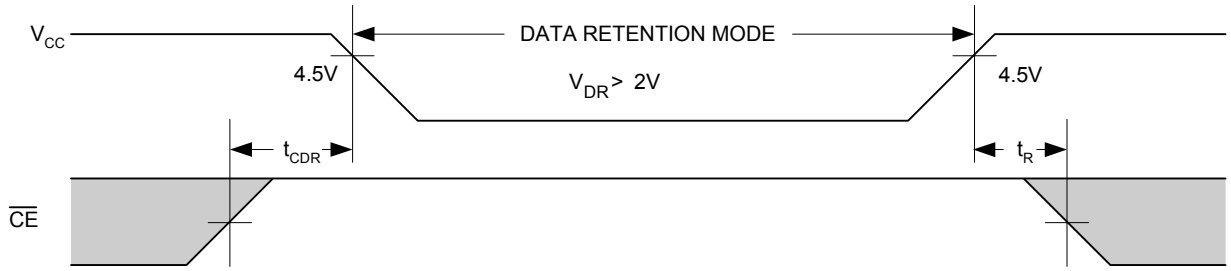
Switching Characteristics Over the Operating Range[6]

Parameter	Description	7C197D-10		7C197D-12		7C197D-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PWE}	$\overline{WE}$ Pulse Width	7		8		9		ns
t_{SD}	Data Set-Up to Write End	6		8		9		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[8]	3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[8,9]		6		7		7	ns

Data Retention Characteristics Over the Operating Range

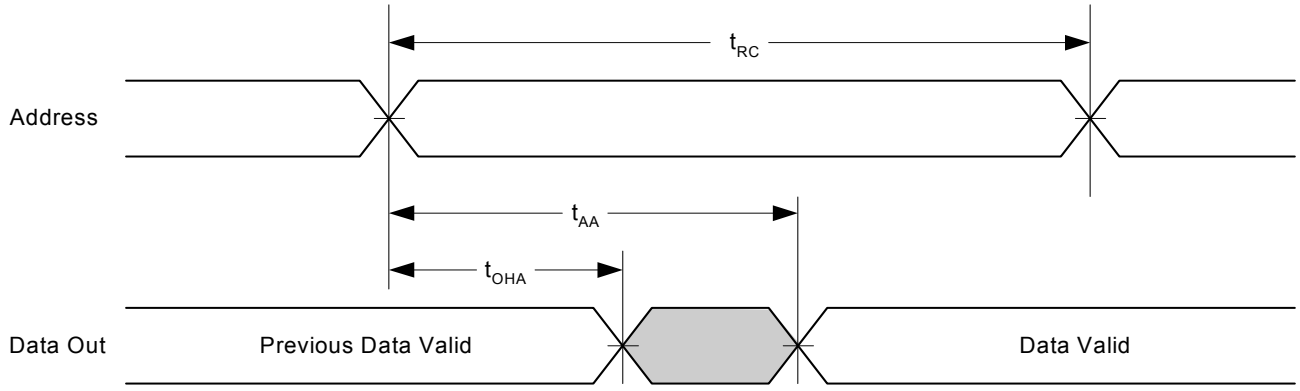
Parameter	Description		Conditions	Min.	Max.	Unit
V_{DR}	V_{CC} for Data Retention			2.0		V
I_{CCDR}	Data Retention Current	Non-L, Com'l / Ind'l	$\underline{V_{CC}} = V_{DR} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		3	mA
		L-Version Only			1.2	mA
t_{CDR}[4]	Chip Deselect to Data Retention Time			0		ns
t_R[11]	Operation Recovery Time			t_{RC}		ns

Data Retention Waveform



Switching Waveforms

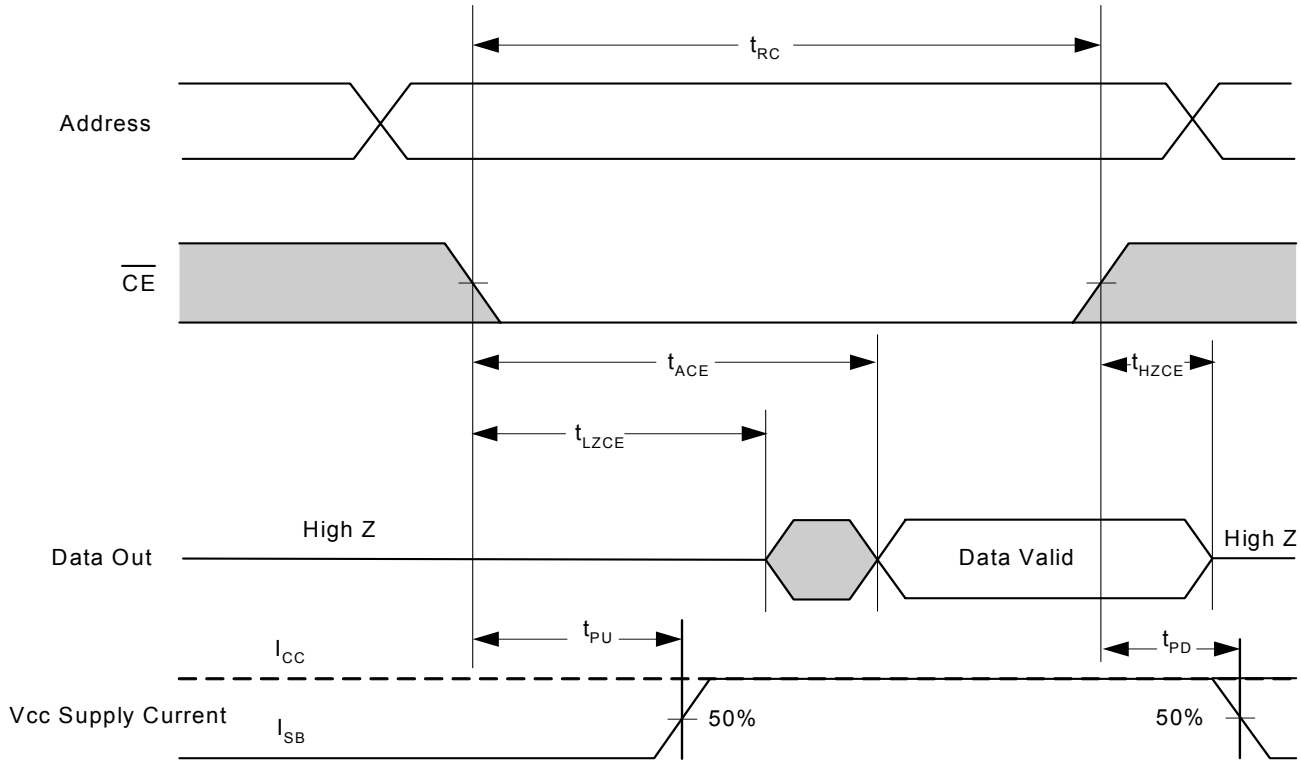
Read Cycle No. 1[12, 13]



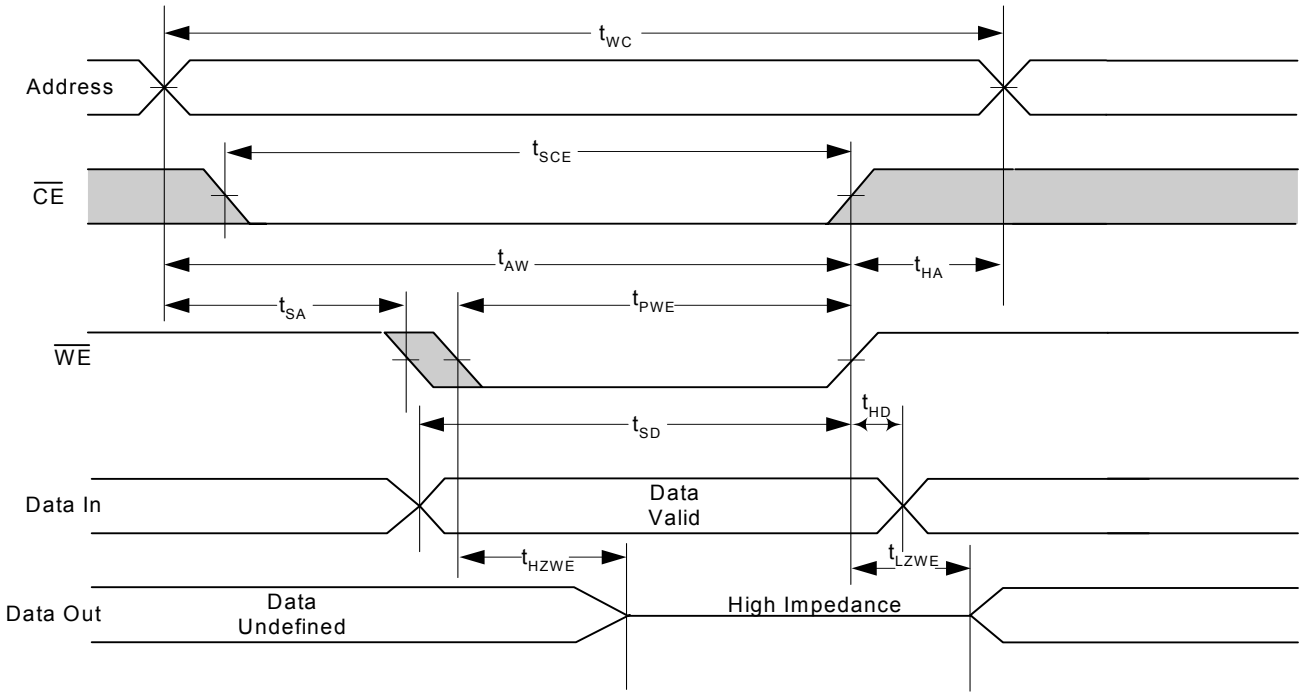
Notes:
11. $\underline{Full}$ device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 50$ µs or stable at $V_{CC(min.)} \geq 50$ µs.
12. $\overline{WE}$ is HIGH for read cycle.
13. Device is continuously selected, $\overline{CE} = V_{IL}$.

Switching Waveforms (continued)

Read Cycle No. 2[12]

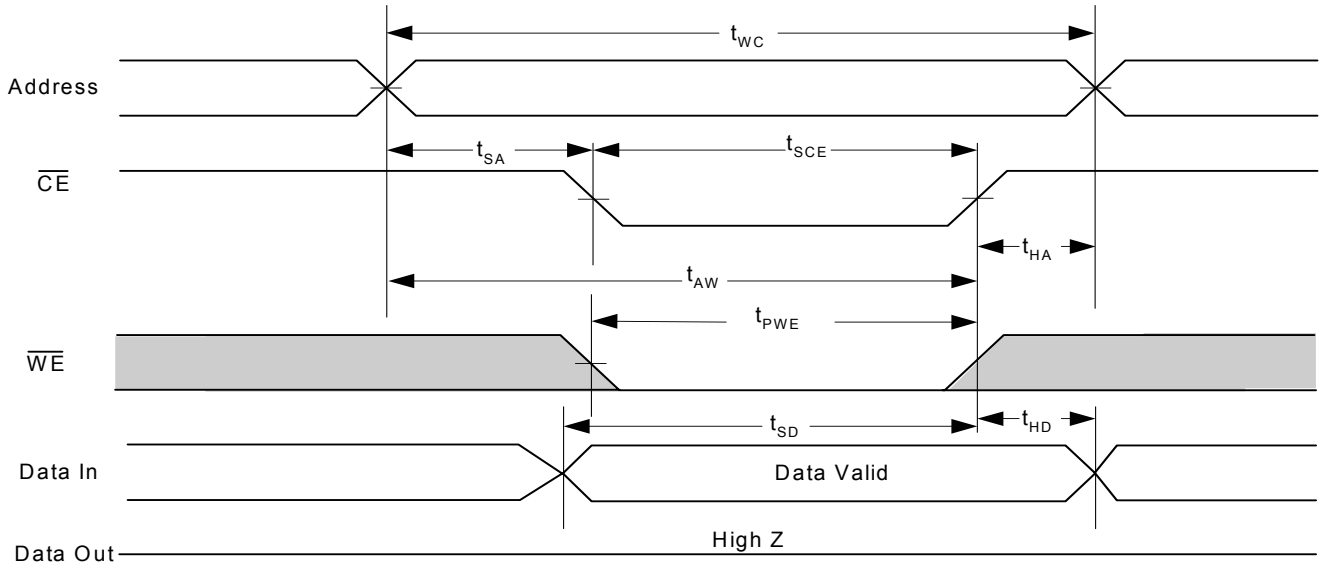


Write Cycle No. 1 ($\overline{WE}$ Controlled)[10]



Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CE}$ Controlled)[10,14]



Truth Table

$\overline{CE}$	$\overline{WE}$	Input/Output	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

Ordering Information

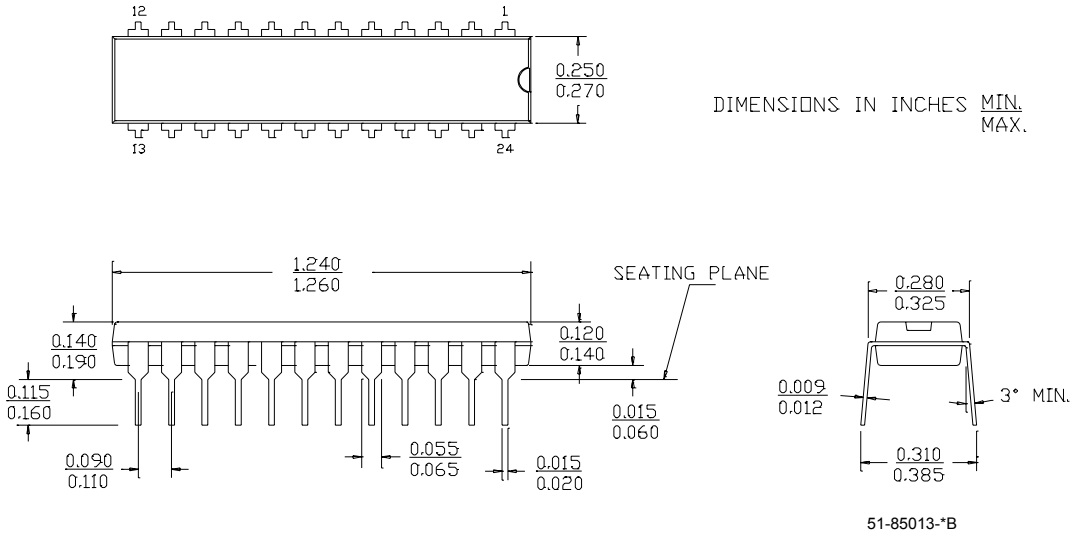
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C197D-10PXC	P13	24-Lead (300-Mil) Molded DIP (Pb-Free)	Commercial
	CY7C197D-10VXC	V13	24-Lead Molded SOJ (Pb-Free)	
	CY7C197D-10PXI	P13	24-Lead (300-Mil) Molded DIP (Pb-Free)	Industrial
	CY7C197D-10VXI	V13	24-Lead Molded SOJ (Pb-Free)	
12	CY7C197D-12PXC	P13	24-Lead (300-Mil) Molded DIP (Pb-Free)	Commercial
	CY7C197D-12VXC	V13	24-Lead Molded SOJ (Pb-Free)	
	CY7C197D-12PXI	P13	24-Lead (300-Mil) Molded DIP (Pb-Free)	Industrial
	CY7C197D-12VXI	V13	24-Lead Molded SOJ (Pb-Free)	
15	CY7C197D-15PXC	P13	24-Lead (300-Mil) Molded DIP (Pb-Free)	Commercial
	CY7C197D-15VXC	V13	24-Lead Molded SOJ (Pb-Free)	
	CY7C197D-15PXI	P13	24-Lead (300-Mil) Molded DIP (Pb-Free)	Industrial
	CY7C197D-15VXI	V13	24-Lead Molded SOJ (Pb-Free)	

Shaded areas contain advance information. Please contact your local Cypress sales representative for availability of these parts.

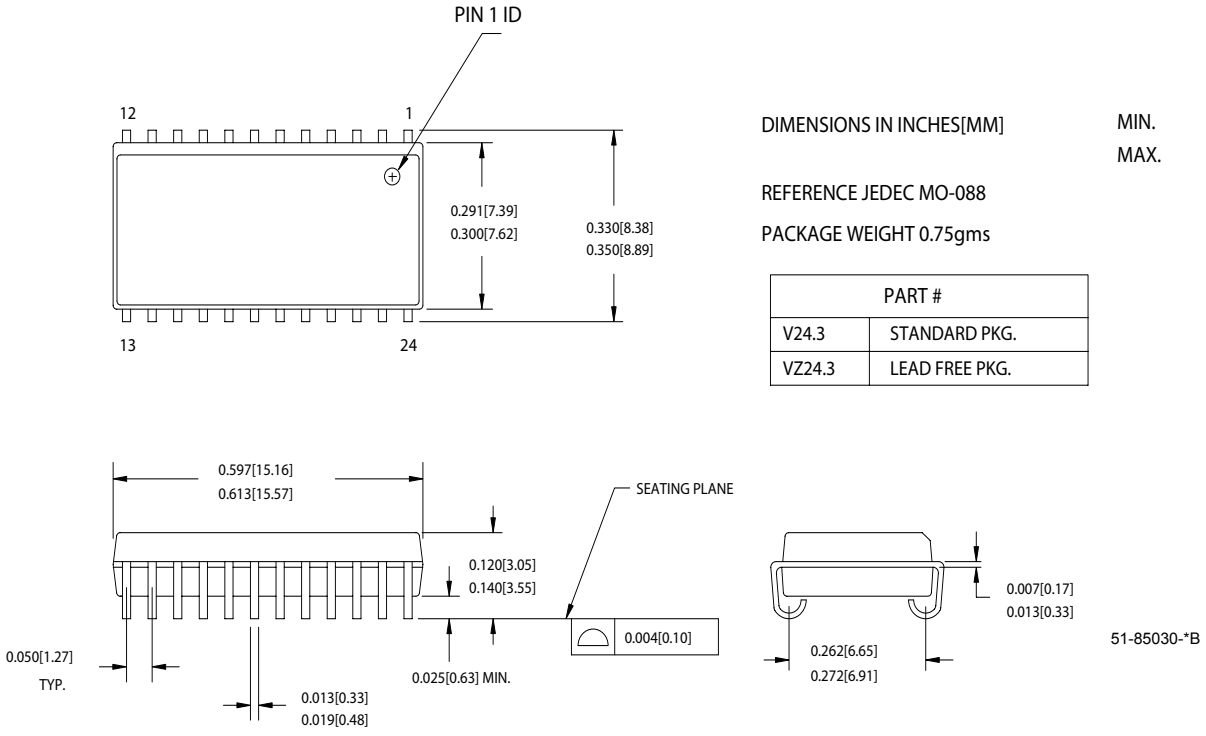
Note:
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Package Diagram

24-Lead (300-Mil) PDIP P13



24-lead (300-mil) SOJ V13



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Document History Page

Document Title: CY7C197D 256K (256K x 1) Static RAM (Preliminary) Document Number: 38-05458				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	201560	See ECN	SWI	Advance Datasheet for C9 IPP
*A	233693	See ECN	RKF	DC parameters modified as per EROS (Spec # 01-02165) Pb-free Offering in Ordering Information
*B	263769	See ECN	RKF	Removed 28-LCC Pinout and Package Diagrams Added Data Retention Characteristics table Added T_{power} Spec in Switching Characteristics table Shaded Ordering Information
*C	307593	See ECN	RKF	1) Reduced Speed bins to -10, -12 and -15 ns 2) Added 'Industrial' grade parts to the Ordering Info on Page #6