CYM74B550
CYM74P550A
CYM74S550, CYM74S551

PRELIMINARY

OPTi Viper Chip Set Level II Cache Module Family

Features

- **Pin-compatible secondary cache module family**
- **Asynchronous (CYM74B550), synchronous pipelined (CYM74P550A), or synchronous burst (CYM74S550, CYM74S551) modules**
- **Ideal for Intel P54C/P55C systems with the OPTi Viper chipset**
- **Operates at 50, 60, and 66 MHz**
- **Uses cost-effective CMOS asynchronous SRAMs or high-performance synchronous SRAMs**
- **160-position Burndy DIMM CELP2X80SC3Z48 connector**
- **3.3V inputs/ data outputs**

Functional Description

This family of secondary cache modules is designed for Intel P54C/P55C systems with the OPTi Viper chip set.

CYM74B550 is a low cost asynchronous cache module that provides 256-Kbytes of cache with industry standard 32Kx8 5 volt SRAMs and 3.3 volt level translators. These modules offer 3-2-2-2 performance at CPU bus speeds up to 66 MHz.

The synchronous modules are available with low cost synchronous pipelined RAMs or high performance synchronous burst RAMs.

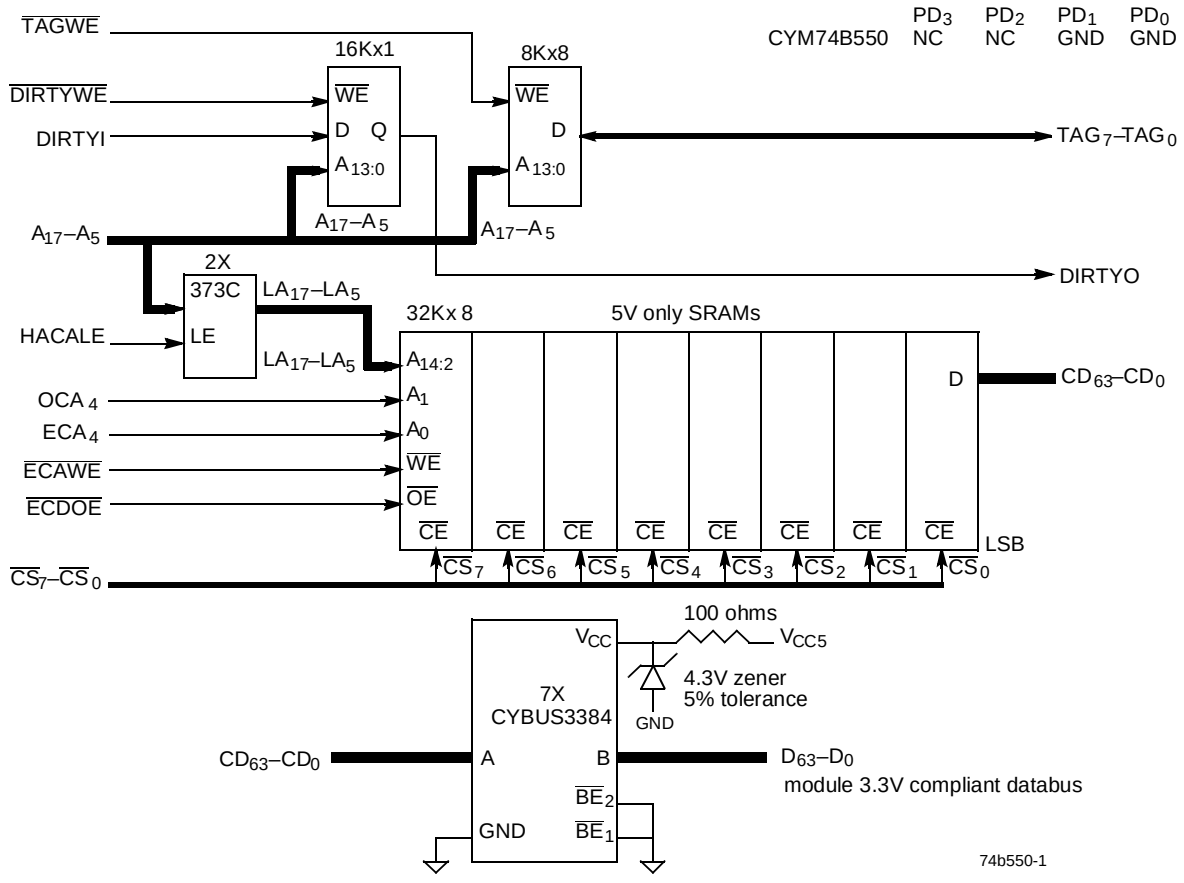
The CYM74P550A is a high performance synchronous pipelined burst 256 KB module and is based on industry standard 32Kx32 pipelined BSRAM. The CYM74P550A has series damping resistors on the data lines.

The CYM74S550 and CYM74S551 are high performance synchronous burst cache modules that provide 256-Kbytes and 512-Kbytes of cache respectively. These modules support 3-1-1-1 performance at 66 MHz.

All of these modules include storage for 8-bits of tag and one dirty bit. Multiple ground pins and on-board decoupling capacitors ensure high performance with maximum noise immunity.

All components on the cache modules are surface mounted on a multi-layer epoxy laminate (FR-4) substrate. The contact pins are plated with 100 micro-inches of nickel covered by 10 micro-inches of gold flash.

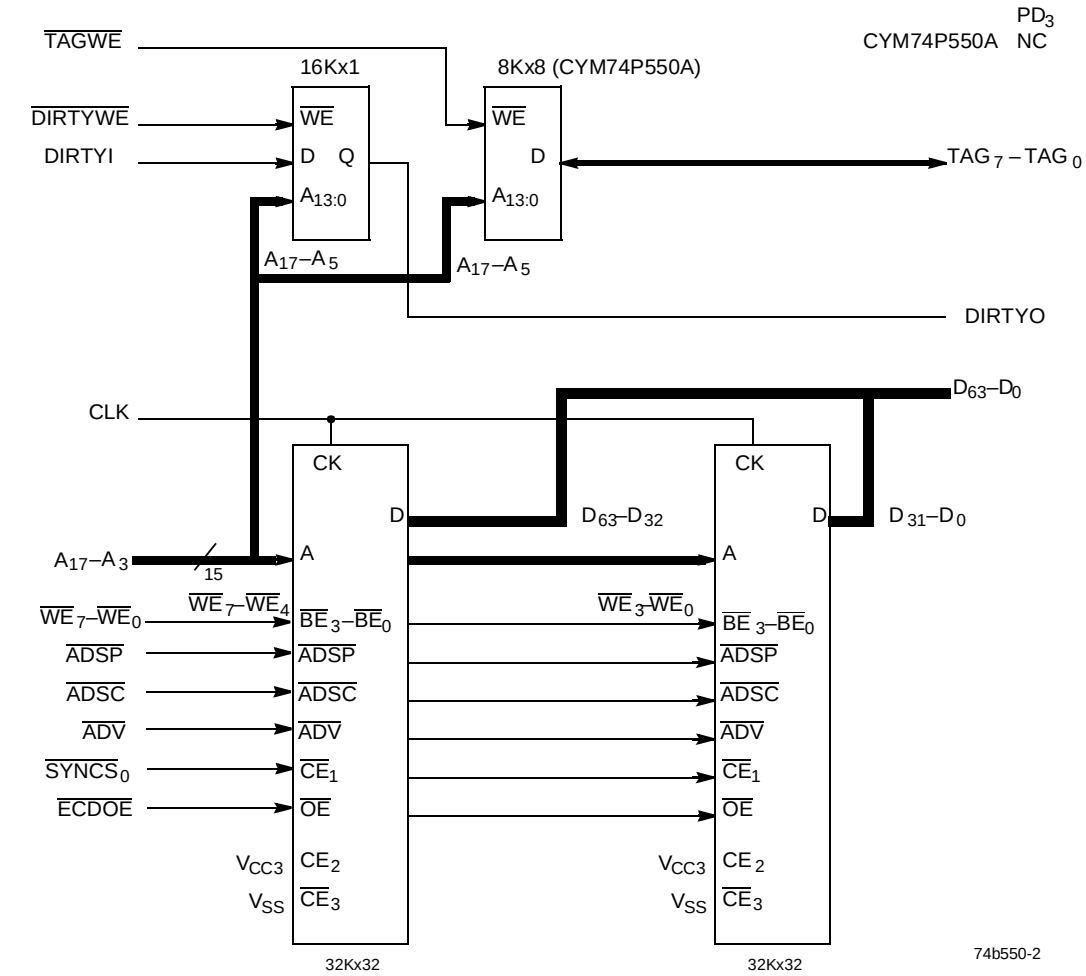
Logic Block Diagram - CYM74B550



Intel is a trademark of Intel Corporation.

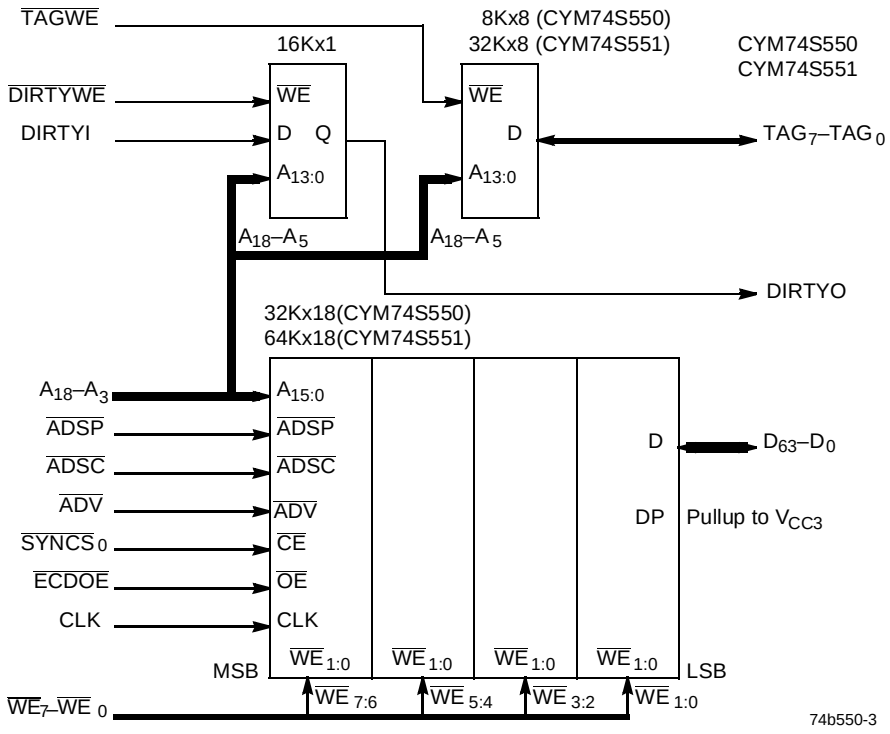
OPTi is a trademark of OPTi, Inc.

Logic Block Diagram – CYM74P550A



Logic Block Diagram - CYM74S550, CYM74S551

Note: A_{18} is not used by CYM74S550



Selection Guide

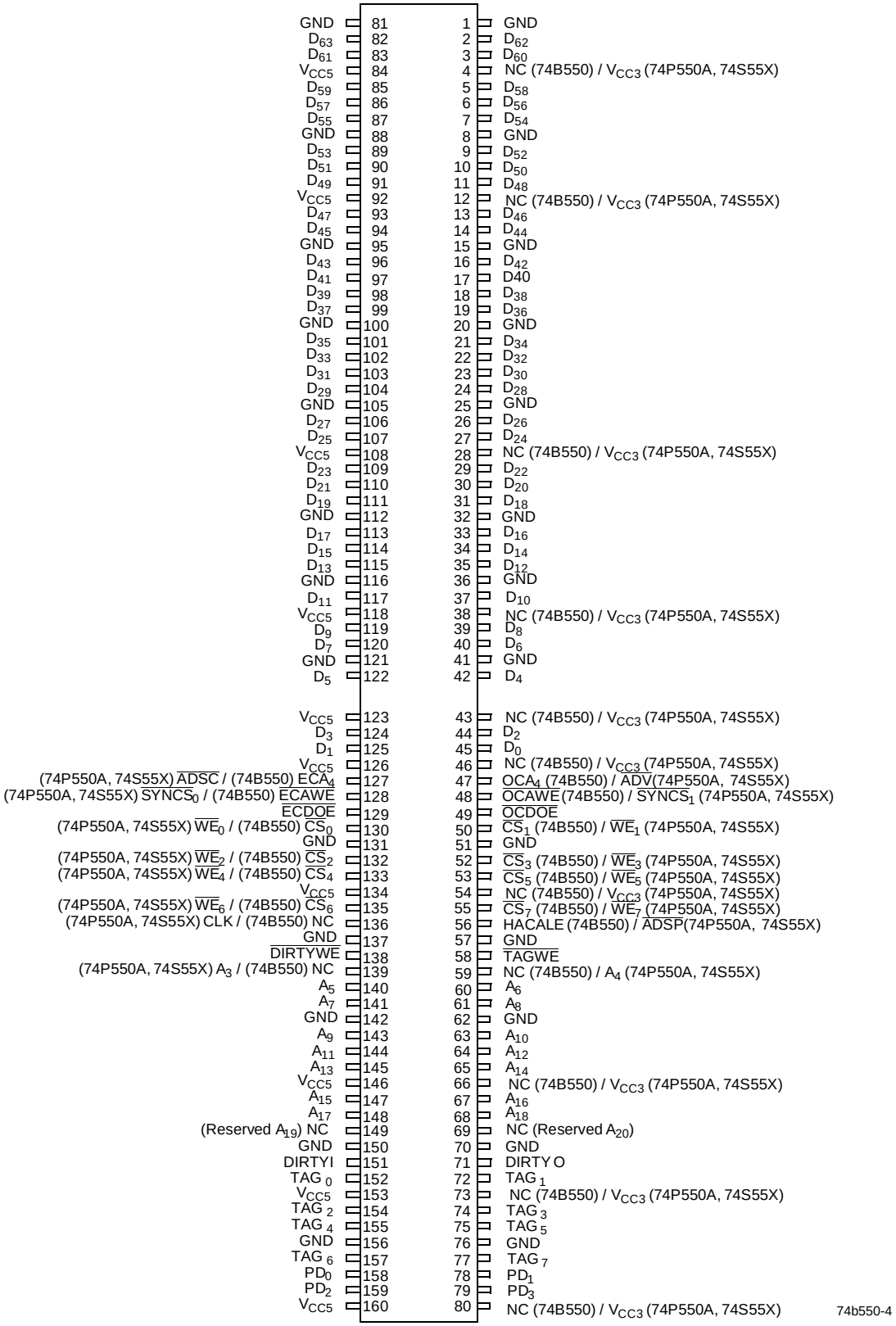
	Asynchronous Cache Modules		
Part Number	**74B550-50**	**74B550-60**	**74B550-66**
Cache Size	256 KB		
System Clock	50 MHz	60 MHz	66 MHz
Data SRAM t_{AA}	25 ns	15 ns	15 ns
Tag SRAM t_{AA}	20 ns	15 ns	12 ns

	Synchronous Pipelined Cache Modules		
Part Number	**74P550A-50**	**74P550A-60**	**74P550A-66**
Cache Size	256 KB		
System Clock	50 MHz	60 MHz	66 MHz
Data SRAM t_{CO}	12 ns	9 ns	9 ns
Tag SRAM t_{AA}	20 ns	15 ns	12 ns

	Synchronous Burst Cache Modules					
Part Number	**74S550-50**	**74S550-60**	**74S550-66**	**74S551-50**	**74S551-60**	**74S551-66**
Cache Size	256 KB			512 KB		
System Clock	50 MHz	60 MHz	66 MHz	50 MHz	60 MHz	66 MHz
Data SRAM t_{CO}	12 ns	9 ns	9 ns	12 ns	9 ns	9 ns
Tag SRAM t_{AA}	20 ns	15 ns	12 ns	20 ns	15 ns	12 ns

Pin Configuration

Dual Read-Out SIMM (DIMM)
Top View



74b550-4

Pin Definitions

Common Signals	Description
V_{CC5}	5V Supply
V_{CC3}	3.3V Supply are CYM74P550A and CYM74S55X only
GND	Ground
A_{18}–A_5	Addresses from processor
D_{63}–D_0	64-bit Data bus from processor
$\overline{ECDOE}$	Even bank output enable input
TAG_7–TAG_0	8-bit Tag RAM bidirectional bus
$\overline{TAGWE}$	Tag RAM write enable input
DIRTYI	1-bit Dirty RAM input
DIRTYO	1-bit Dirty RAM output
$\overline{DIRTYWE}$	Dirty RAM write enable input
PD_3–PD_0	Presence Detect pins
NC	Signal not connected on module.
CYM74B550 Only Signals	**Description**
HACALE	Address Latch Enable input to transparent address latches
OCA_4	Address bit A_3 in async cache module (CYM74B550)
ECA_4	Address bit A_4 in async cache module (CYM74B550)
$\overline{CS}_7$–$\overline{CS}_0$	Data RAM Chip Select inputs
$\overline{ECAWE}$	Even bank write enable input
CYM74P550A,CYM74S55X Signals	**Description**
CLK	Clock input
A_4–A_3	Lower order address bits from processor
$\overline{ADSC}$	Cache Controller Address Strobe input
$\overline{ADSP}$	Processor Address Strobe input
$\overline{ADV}$	Burst Address Advance input
$\overline{SYNCS}_0$	Even bank synchronous burst RAM chip select input
$\overline{SYNCS}_1$	Odd bank synchronous burst RAM chip select input (not used)
$\overline{WE}_7$–$\overline{WE}_0$	Write enable inputs to Data RAMs

Presence Detect Pins

	PD_3	PD_2	PD_1	PD_0
Asynchronous - CYM74B550	NC	NC	GND	GND
Sync Pipelined - CYM74P550A	NC	NC	GND	NC
Synch Burst - CYM74S550	NC	NC	NC	GND
Synch Burst - CYM74S551	NC	GND	NC	GND

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –55°C to +125°C

Ambient Temperature
with Power Applied ..... –0°C to +70°C

3.3V Supply Voltage to Ground Potential..... –0.5V to +4.6V

5V Supply Voltage to Ground Potential..... –0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State ..... –0.5V to +4.6V

DC Input Voltage .....–0.5V to +4.6V

Output Current into Outputs (LOW)..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC5}	V_{CC3}
Commercial (CYM74B550)	0°C to +70°C	5V ± 5%	N/A
Commercial (CYM74P550A, CYM74S55X)	0°C to +70°C	5V ± 5%	3.3V +10%– 5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Condition	Min.	Max.	Unit
V_{IH}	Input HIGH Voltage		2.2		V
V_{IL}	Input LOW Voltage	CYM74B550	–0.5	0.8	V
V_{IL}	Input LOW Voltage	CYM74P550A, CYM74S55X	–0.3	0.8	V
V_{OH}	Output HIGH Voltage	V_{CC3}=Min. I_{OH} = -4 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC3}=Min. I_{OL} = 8 mA		0.4	V
I_{CC} (74B550)	Operating Supply Current	V_{CC5}=Max., I_{OUT}=0 mA, f=f_{MAX}		1650	mA
I_{CC} (74P550A)	Operating Supply Current	V_{CC5}=Max.,V_{CC3}=Max., I_{OUT}=0 mA, f=f_{MAX}		900	mA
I_{CC} (74S550)	Operating Supply Current	V_{CC5}=Max., V_{CC3}=Max., I_{OUT}=0 mA, f=f_{MAX}		1500	mA
I_{CC} (74S551)	Operating Supply Current	V_{CC5}=Max., V_{CC3}=Max., I_{OUT}=0 mA, f=f_{MAX}		1500	mA

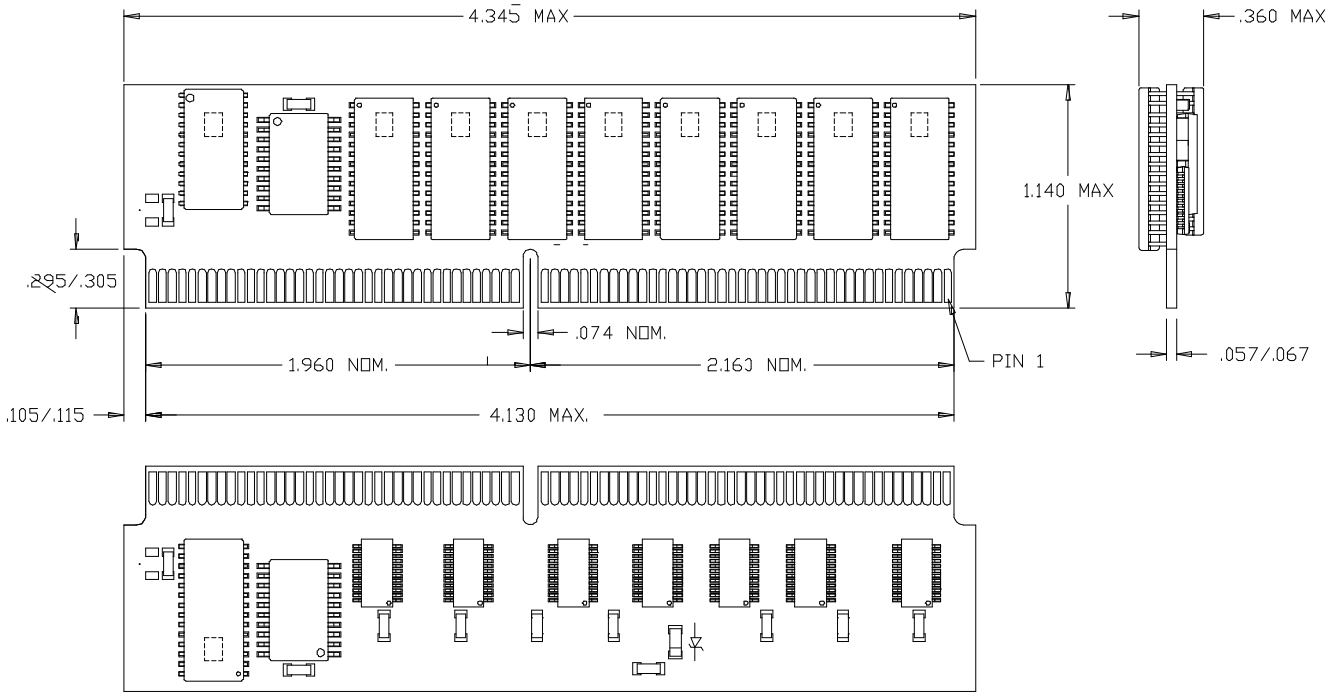
Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Description	Operating Range
50	CYM74B550PM-50C	PM35	160-Pin Dual-Readout SIMM	Async 256 KB	Commercial
	CYM74P550APM-50C	PM42		Sync Pipelined 256 KB	
	CYM74S550PM-50C	PM33		Sync Burst 256 KB	
	CYM74S551PM-50C			Sync Burst 512 KB	
60	CYM74B550PM-60C	PM35	160-Pin Dual-Readout SIMM	Async 256 KB	Commercial
	CYM74P550APM-60C	PM42		Sync Pipelined 256 KB	
	CYM74S550PM-60C	PM33		Sync Burst 256 KB	
	CYM74S551PM-60C			Sync Burst 512 KB	
66	CYM74B550PM-66C	PM35	160-Pin Dual-Readout SIMM	Async 256 KB	Commercial
	CYM74P550APM-66C	PM42		Sync Pipelined 256 KB	
	CYM74S550PM-66C	PM33		Sync Burst 256 KB	
	CYM74S551PM-66C	PM33		Sync Burst 512 KB	

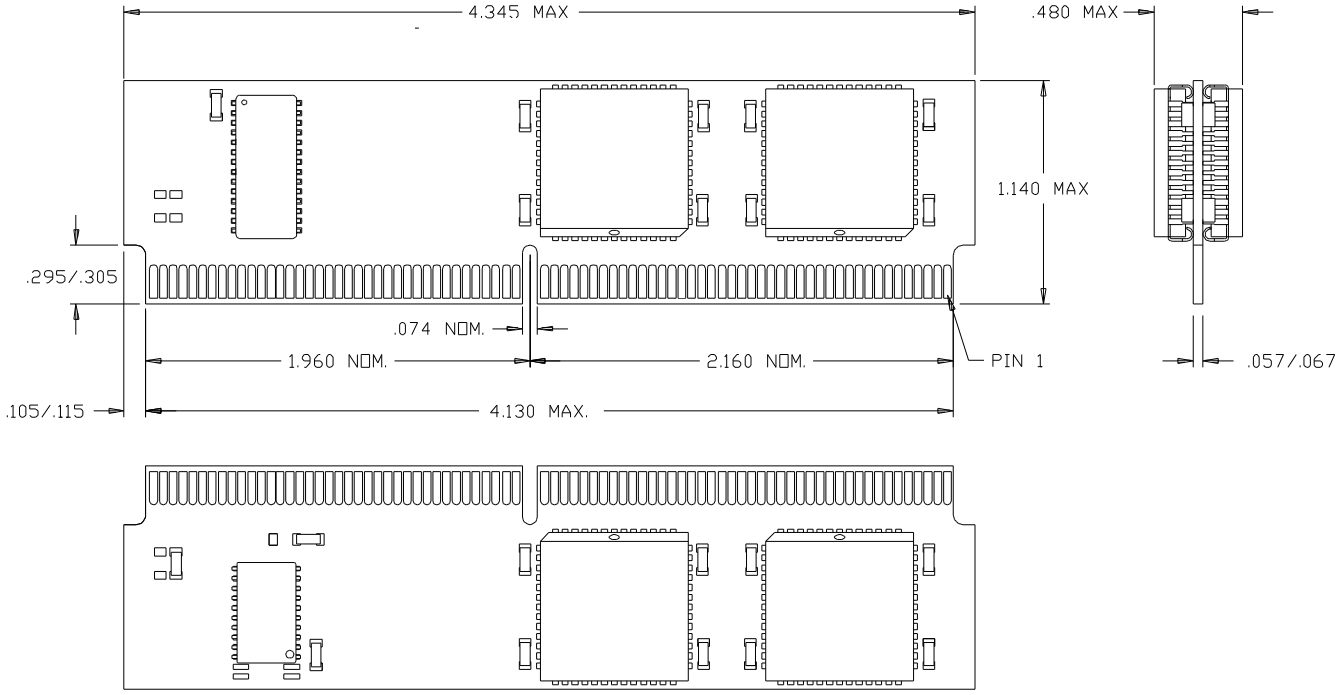
Document #: 38-M-00076-A

Package Diagrams

160-Pin Dual Readout SIMM (PM35)



160-Pin Dual Readout SIMM (PM33)



Package Diagrams (continued)

160-Pin Dual Readout SIMM (PM42)