



AOD3N50
3A, 500V N-Channel MOSFET

General Description

The AOD3N50 has been fabricated using an advanced high voltage MOSFET process that is designed to deliver high levels of performance and robustness in popular AC-DC applications. By providing low $R_{DS(on)}$, C_{iss} and C_{rss} along with guaranteed avalanche capability these parts can be adopted quickly into new and existing offline power supply designs.

Features

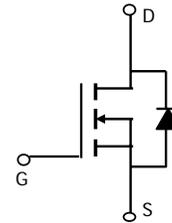
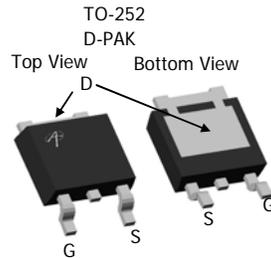
V_{DS} (V) = 600V @ 150°C

I_D = 2.8A

$R_{DS(ON)} < 3\Omega$ ($V_{GS} = 10V$)

100% UIS Tested!

100% R_g Tested!



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	500	V
Gate-Source Voltage	V_{GS}	± 30	V
Continuous Drain Current ^B	I_D	$T_C=25^\circ\text{C}$	A
		$T_C=100^\circ\text{C}$	
Pulsed Drain Current ^C	I_{DM}	9.0	
Avalanche Current ^C	I_{AR}	2.0	A
Repetitive avalanche energy ^C	E_{AR}	60	mJ
Single pulsed avalanche energy ^H	E_{AS}	120	mJ
Peak diode recovery dv/dt	dv/dt	5	V/ns
Power Dissipation ^B	P_D	$T_C=25^\circ\text{C}$	W
		Derate above 25°C	W/°C
Junction and Storage Temperature Range	T_J, T_{STG}	-50 to 150	°C
Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds	T_L	300	°C

Thermal Characteristics

Parameter	Symbol	Typical	Maximum	Units
Maximum Junction-to-Ambient ^{A,G}	$R_{\theta JA}$	45	55	°C/W
Maximum Case-to-Sink ^A	$R_{\theta CS}$	-	0.5	°C/W
Maximum Junction-to-Case ^{D,F}	$R_{\theta JC}$	1.8	2.2	°C/W

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}, V_{GS}=0\text{V}, T_J=25^\circ\text{C}$	500			V
		$I_D=250\mu\text{A}, V_{GS}=0\text{V}, T_J=125^\circ\text{C}$		600		V
$BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D=250\mu\text{A}, V_{GS}=0\text{V}$		0.54		V/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=500\text{V}, V_{GS}=0\text{V}$			1	μA
		$V_{DS}=400\text{V}, T_J=125^\circ\text{C}$			10	
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}, V_{GS}=\pm 30\text{V}$			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=5\text{V}, I_D=250\mu\text{A}$	3.5	4.1	4.7	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}, I_D=1.5\text{A}$		2.3	3	Ω
g_{FS}	Forward Transconductance	$V_{DS}=40\text{V}, I_D=1.5\text{A}$		2.8		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}, V_{GS}=0\text{V}$		0.78	1	V
I_S	Maximum Body-Diode Continuous Current				3	A
I_{SM}	Maximum Body-Diode Pulsed Current				9	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=25\text{V}, f=1\text{MHz}$	221	276	331	pF
C_{oss}	Output Capacitance		25	31.4	38	pF
C_{rss}	Reverse Transfer Capacitance		2.1	2.6	3.0	pF
R_g	Gate resistance	$V_{GS}=0\text{V}, V_{DS}=0\text{V}, f=1\text{MHz}$	1.9	3.9	5.9	Ω
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	$V_{GS}=10\text{V}, V_{DS}=400\text{V}, I_D=3\text{A}$		6.7	8.0	nC
Q_{gs}	Gate Source Charge		1.7	2.0	nC	
Q_{gd}	Gate Drain Charge		2.7	3.2	nC	
$t_{D(on)}$	Turn-On Delay Time	$V_{GS}=10\text{V}, V_{DS}=250\text{V}, I_D=3\text{A}, R_G=25\Omega$		11	13.2	ns
t_r	Turn-On Rise Time		19	23.0	ns	
$t_{D(off)}$	Turn-Off Delay Time		20.5	24.6	ns	
t_f	Turn-Off Fall Time		15	18.0	ns	
t_{rr}	Body Diode Reverse Recovery Time	$I_F=3\text{A}, dI/dt=100\text{A}/\mu\text{s}, V_{DS}=100\text{V}$		134	161	ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=3\text{A}, dI/dt=100\text{A}/\mu\text{s}, V_{DS}=100\text{V}$		0.89	1.1	μC

A: The value of $R_{\theta JA}$ is measured with the device in a still air environment with $T_A=25^\circ\text{C}$.

B: The power dissipation P_D is based on $T_{J(MAX)}=150^\circ\text{C}$ in a TO252 package, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=150^\circ\text{C}$.

D: The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using $<300\mu\text{s}$ pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}=150^\circ\text{C}$.

G: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$.

H: $L=60\text{mH}, I_{AS}=2\text{A}, V_{DD}=50\text{V}, R_G=10\Omega$, Starting $T_J=25^\circ\text{C}$

Rev1: Dec. 2008

THIS PRODUCT HAS BEEN DESIGNED AND QUALIFIED FOR THE CONSUMER MARKI -50 to 175

COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

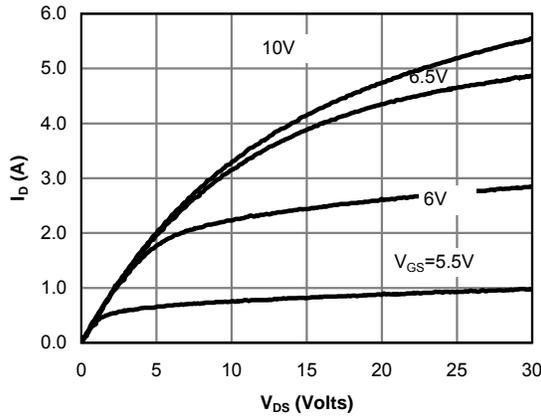


Fig 1: On-Region Characteristics

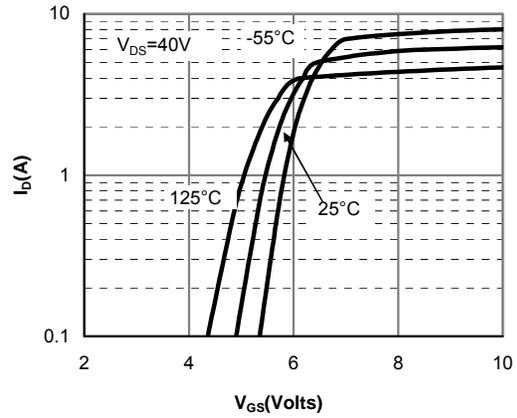


Figure 2: Transfer Characteristics

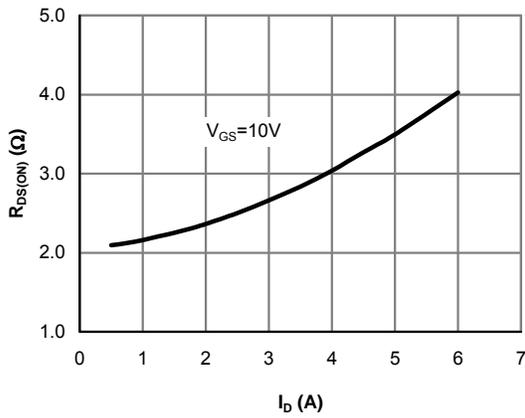


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

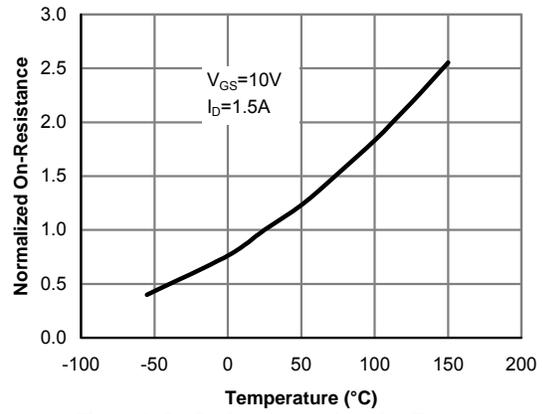


Figure 4: On-Resistance vs. Junction Temperature

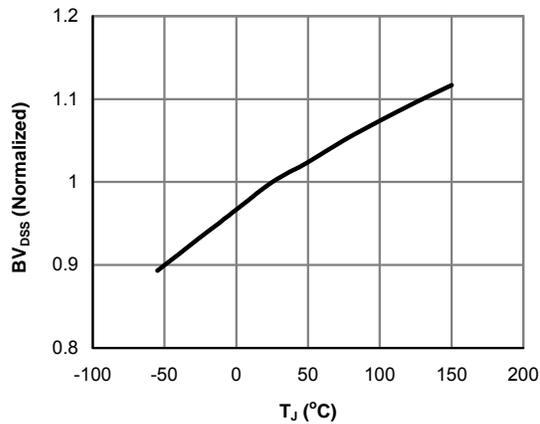


Figure 5: Break Down vs. Junction Temperature

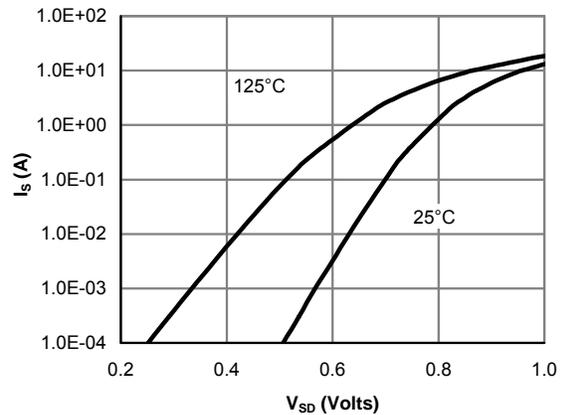


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

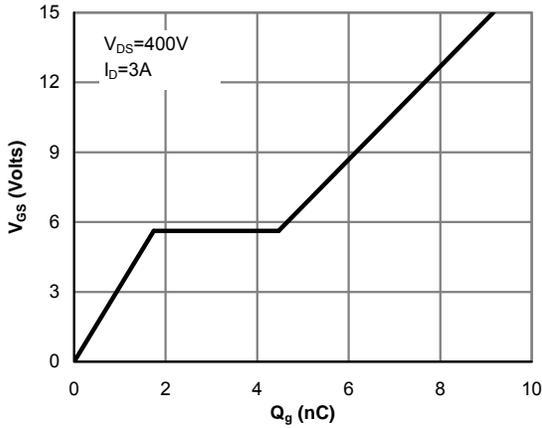


Figure 7: Gate-Charge Characteristics

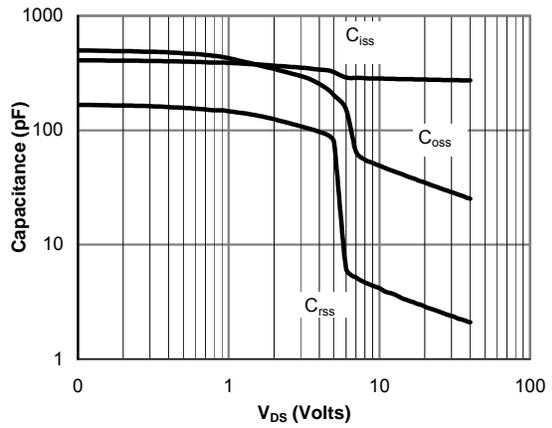


Figure 8: Capacitance Characteristics

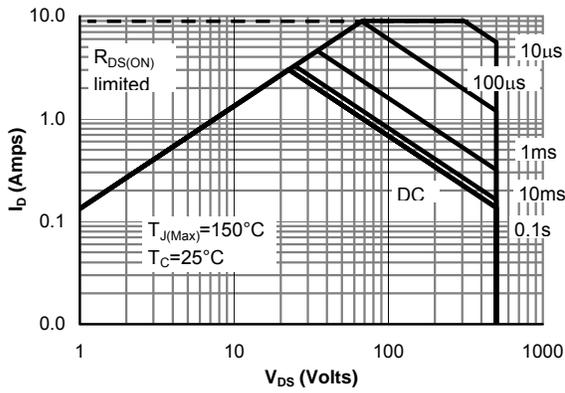


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

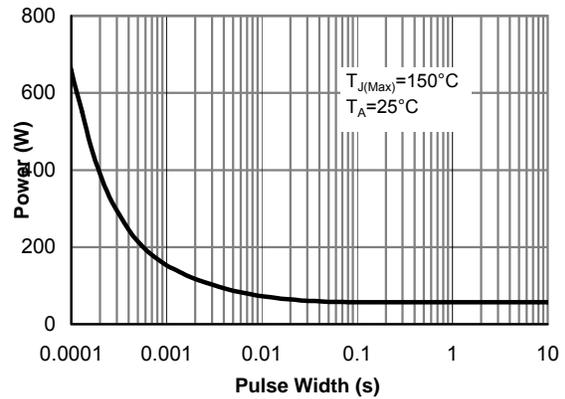


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

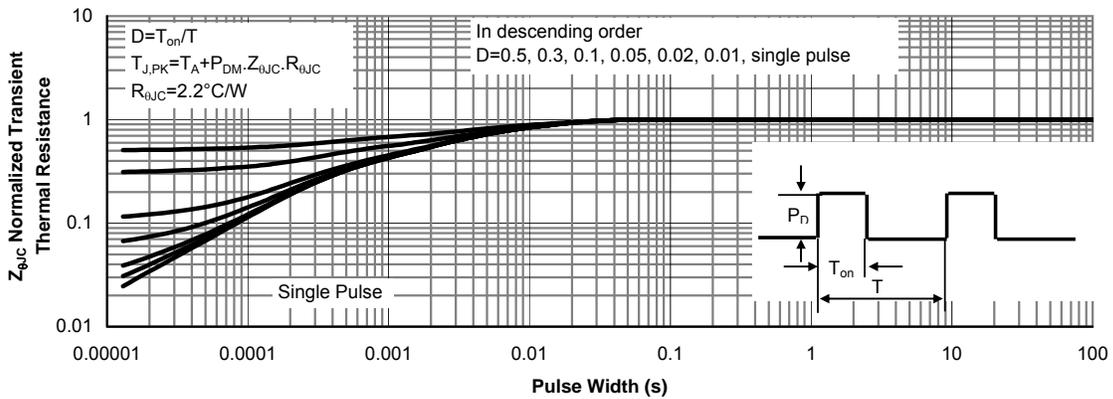


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

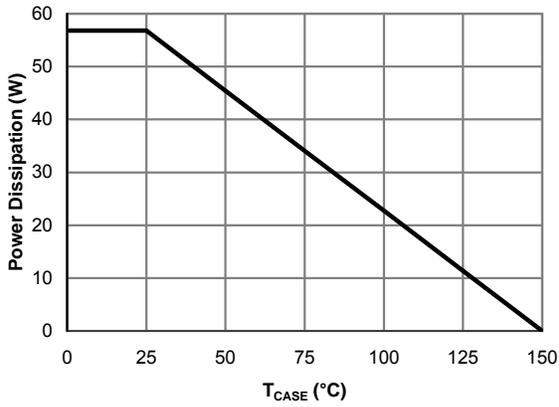


Figure 12: Power De-rating (Note B)

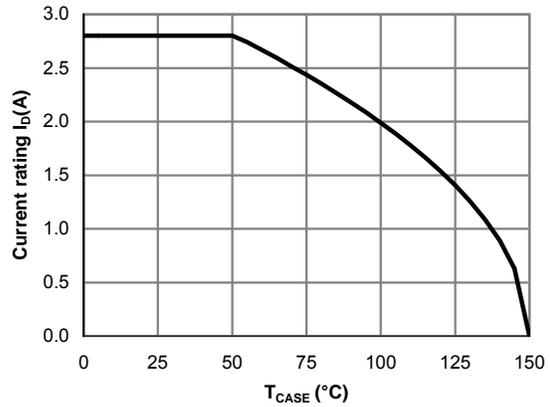


Figure 13: Current De-rating (Note B)

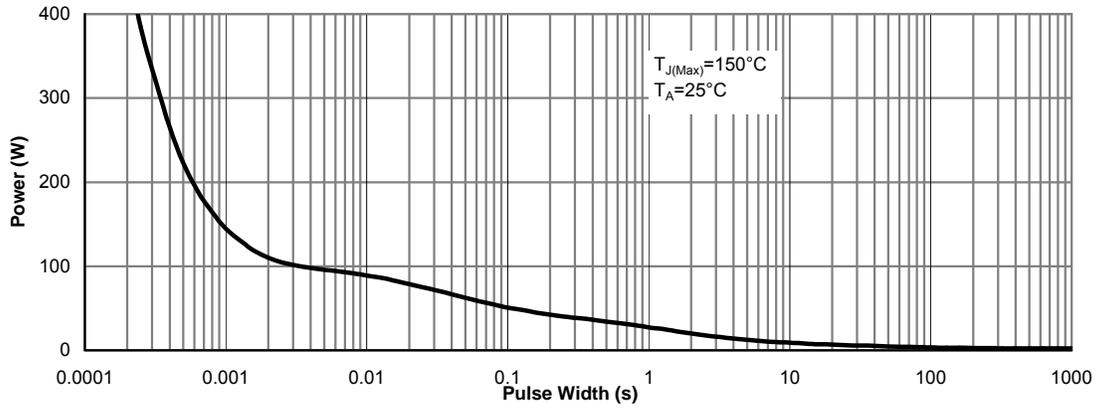


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note G)

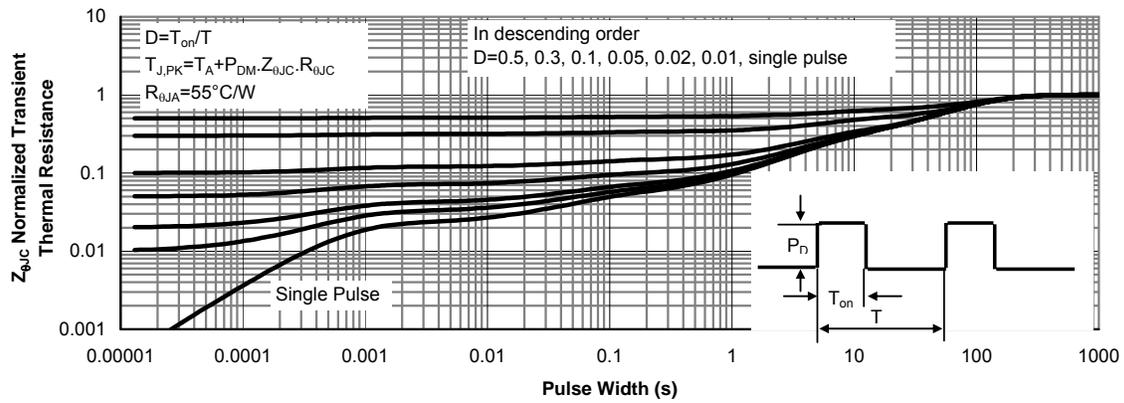
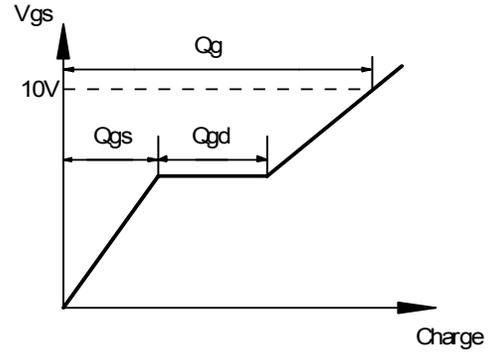
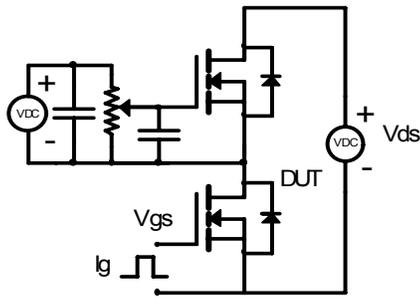
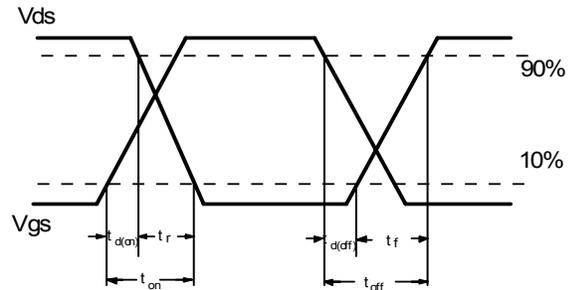
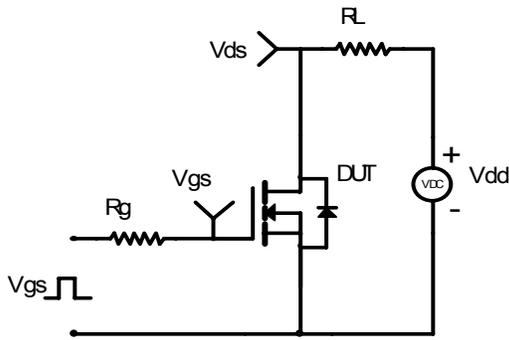


Figure 15: Normalized Maximum Transient Thermal Impedance (Note G)

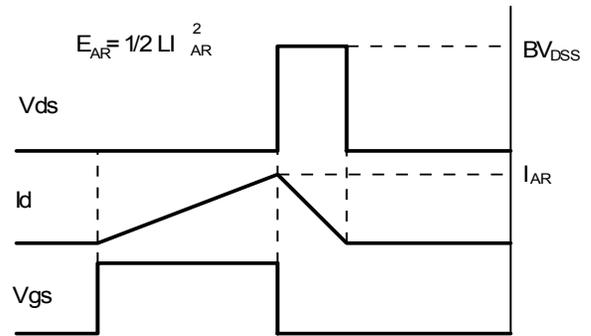
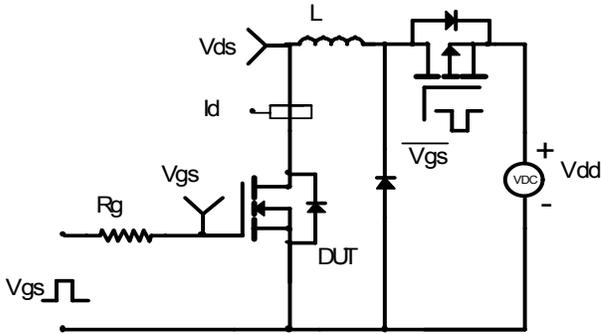
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

