D8255

Programmable Peripheral Interface

ver 1.00

OVERVIEW

The D8255 is a programmable I/O device which is designed for use with all Intel and most other microprocessors.
It provides 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation:

- Mode 0 - Basic Input/Output. This functional configuration provides simple input and output operations for each of the three ports. No „handshaking" is required, data is simply written to or read from a specified port. Mode 0 Basic Functional Definitions:
  - *Two 8-bit ports and two 4-bit ports.*
  - *Any port can be input or output.*
  - *16 different Input/Output configurations are possible in this Mode*
- MODE 1 - Strobed Input/Output. This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or „handshaking" signals. In mode 1, Port A and Port B use the lines on Port C to generate or accept these „handshaking" signals. Mode 1 Basic functional Definitions:
  - *Two Groups (Group A and Group B).*
  - *Each group contains one 8-bit data port and one 4-bit control/data port.*
  - *The 8-bit data port can be either input or output Both inputs and outputs are latched.*
  - *The 4-bit port is used for control and status of the 8-bit data port.*
- MODE 2 - Strobed Bidirectional Bus I/O. This functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus I/O). „Handshaking" signals are provided to maintain proper bus flow discipline in a similar manner to MODE 1. Interrupt generation and enable/disable functions are also available. MODE 2 Basic Functional Definitions:
  - *Used in Group A only.*
  - *One 8-bit, bi-directional bus port (Port A) and a 5-bit control port (Port C).*
  - *The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A)*

The functional configuration of the D8255 is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures.
The control word register can be both written and read as shown in the address decode table in the pin descriptions.

http://www.DigitalCoreDesign.com
http://www.dcd.pl

KEY FEATURES

- Compatible with industry standard 8255
- 24 I/O lines individually programmed in 2 groups of 12:
  - *Group A - Port A and upper half of Port C*
  - *Group B – Port B and lower half of Port C*
- 3 major modes of operation
  - *Mode 0 – Basic input/output*
  - *Mode 1 – Strobed Input/output*
  - *Mode 2 – Bi-directional Bus*
- Control Word Read-Back Capability
- Direct Bit Set/Reset Capability
- Interrupt control functions
- No internal three states busses
- Fully synthesizable technology independent source code.

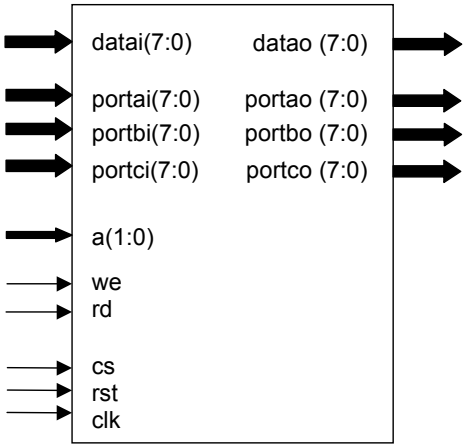
DESIGN FEATURES

- ONE GLOBAL SYSTEM CLOCK
- SYNCHRONOUS RESET
- ALL ASYNCHRONOUS INPUT SIGNALS ARE SYNCHRONIZED BEFORE INTERNAL USE
- ALL LATCHES IMPLEMENTED IN ORIGINAL 8255 DEVICES ARE REPLACED BY EQUIVALENT FLIP-FLOP REGISTERS, WITH THE SAME FUNCTIONALITY

APPLICATIONS

- Embedded microprocessor boards
- Interface to the printer
- I/O component to interface peripheral
- equipment to the microcomputer system bus

SYMBOL



PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
clk	input	Global clock
reset	input	Global reset
cs	input	Chip select
rd	input	Processor read strobe
we	input	Processor write strobe
a[1:0]	input	Processor address lines
portai[7:0]	input	Port A input
portbi[7:0]	input	Port B input
portci[7:0]	input	Port C input
datai[7:0]	input	Data bus (input)
datao[7:0]	output	Data bus (output)
portao[7:0]	output	Port A output
portbo[7:0]	output	Port B output
portco[7:0]	output	Port C output

BLOCK DIAGRAM

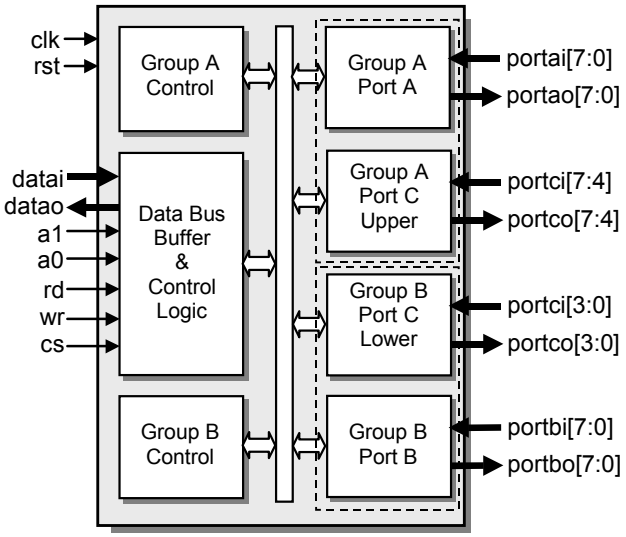
Data Bus Buffer– The Data Bus Buffer is used to interface the D8255 to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic - The control logic block manages all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups A and B.

Group A and Group B Controls - The functional configuration of each port is programmed by the systems software. In essence, the CPU “outputs”' a control word to the D8255. The control word contains information such as “mode”', “bit set”, “bit reset”, etc., that initializes the functional configuration of the D8255. Each of the Control blocks (Group A and Group B) accepts “commands” from the Read/Write Control Logic, receives “control words” from the internal data bus and issues the proper commands to its associated ports.

Group A - Port A and upper half of Port C
Group B - Port B and lower half of Port C

The control word register can be both written and read. Figure below shows the control word format for both Read and Write operations. When the control word is read, bit D7 will always be a logic “1”, as this implies control word mode information.



Ports A, B, and C - The D8255 contains three 8-bit ports. All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or “personality” to further enhance the power and flexibility of the D8255.

Port A - One 8-bit data output latch/buffer and one 8-bit input latch buffer. Both „pull-up" and “pulldown” bus hold devices are present on Port A.

Port B - One 8-bit data input/output latch/buffer. Only „pull-up" bus hold devices are present on Port B.

Port C - One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B. Only „pull-up" bus hold devices are present on Port C.

DELIVERABLES

- Source code:
  - VHDL Source Code or/and
  - VERILOG Source Code or/and
  - ALTERA’s Megafunction or/and
  - EDIF netlist
- VHDL & VERILOG test bench environment
  - Active-HDL automatic simulation macros
  - ModelSim automatic simulation macros
  - Tests with reference responses
- Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet
- Synthesis scripts
- Example application
- Technical support
  - IP Core implementation support
  - 3 months maintenance
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