



ASD™
IPAD™ Computer

DDR110-xxT7RL

DOUBLE DATA RATE TERMINATION NETWORK WITH DISABLE SWITCH

MAIN APPLICATION

DDR (double data rate) Termination Network used on.

- Motherboard
- Workstation
- Server
- Notebooks

DESCRIPTION

The DDR110 provides 10 bits resistor Network to be used for SDR/DDR (double data rate) SDRAM bus Termination.

This device has a series resistors (R_s) to reduce signal reflection noise. This eliminates the need for external terminating resistors.

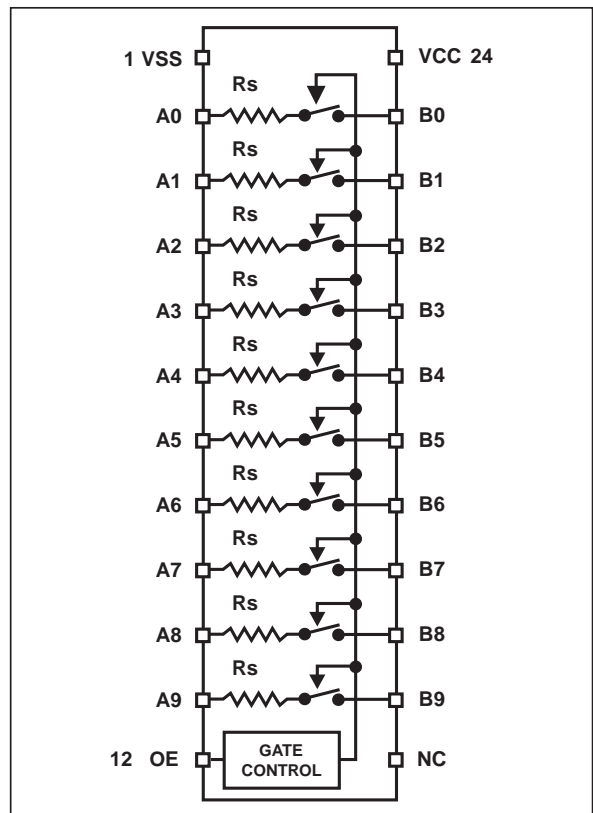
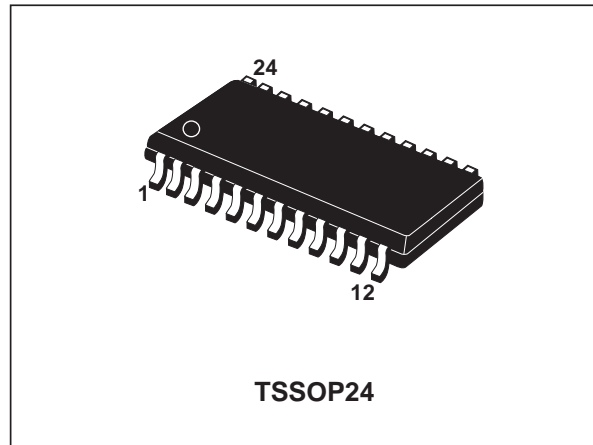
The DDR Termination Network is enabled with the output Enable pin (OE). When OE is HIGH Inputs are connected to Outputs (A connected to B). When OE is LOW every inputs are in High impedance state ($H_i - Z$).

The DDR Termination Network is a bidirectional device when the internal switch is ON. When the switch is OFF, the device will block current in both directions.

This device is made using ST IPAD™ (Integrated Passive & Active devices) technology.

FEATURES AND BENEFITS

- 10 bits Termination Network.
- Integrated Termination resistor (R_s)
- Enable input TTL level compatible
- Impedance matching $\pm 2\%$ (A0-B0 / An-Bn)
- Optimized Low Crosstalk for parallel Termination to V_{tt} .
- Optimized Low propagation delay



DDR110-xxT7RL

FUNCTION TABLE

OE	B0 - B9	Function
High	A0 - A9	Connect Termination
Low	Hi - Z	Disconnect Termination

ABSOLUTE MAXIMUM RATINGS (Tamb = 25°C)

Symbol	Parameter	Test Conditions	Value			Unit
			Tambient = 25°C			
			Min.	Typ.	Max.	
V _{CC}	Supply voltage range		- 0.5	5	7	V
V _{IN}	Input voltage range DQ0/7, DM0, DQS0		- 0.5		7	V
V _{TT}	Termination voltage		- 0.5		7	V
V _{OE}	Termination Enable Voltage range		- 0.5		7	V
I _{IN}	Continuous input current				30	mA
V _{ESD}	ESD ratings (input / output YOE)	HBM MIL STD 883C			2	kV
T _{STG}	Storage temperature		- 65		150	°C

RECOMMENDED OPERATING CONDITIONS (Tamb = 25°C)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V _{IN}	Input voltage DQ0/7, DM0, DQS0	OE LOW OE HIGH	0 0		+ 3.3 + 2.5	V
V _{IH}	Output Enable (OE) HIGH voltage	Guaranteed logic HIGH level	2	5 ⁽¹⁾		V
V _{IL}	Output Enable (OE) LOW voltage	Guaranteed logic LOW level			0.8	V
V _{CC}	Supply voltage		4.5	5	5.5	V
V _{TT}	Termination voltage			1.25		V

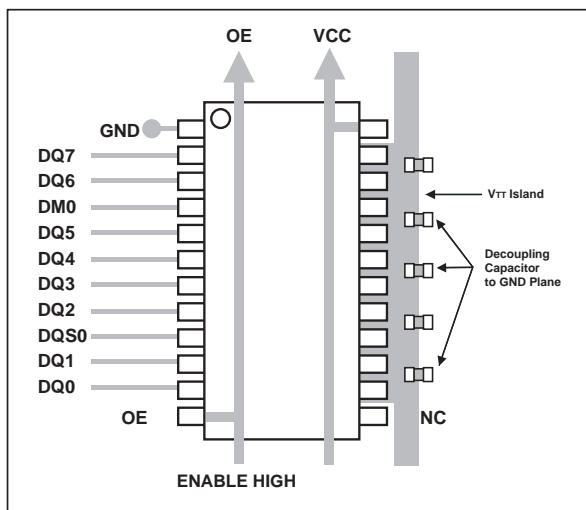
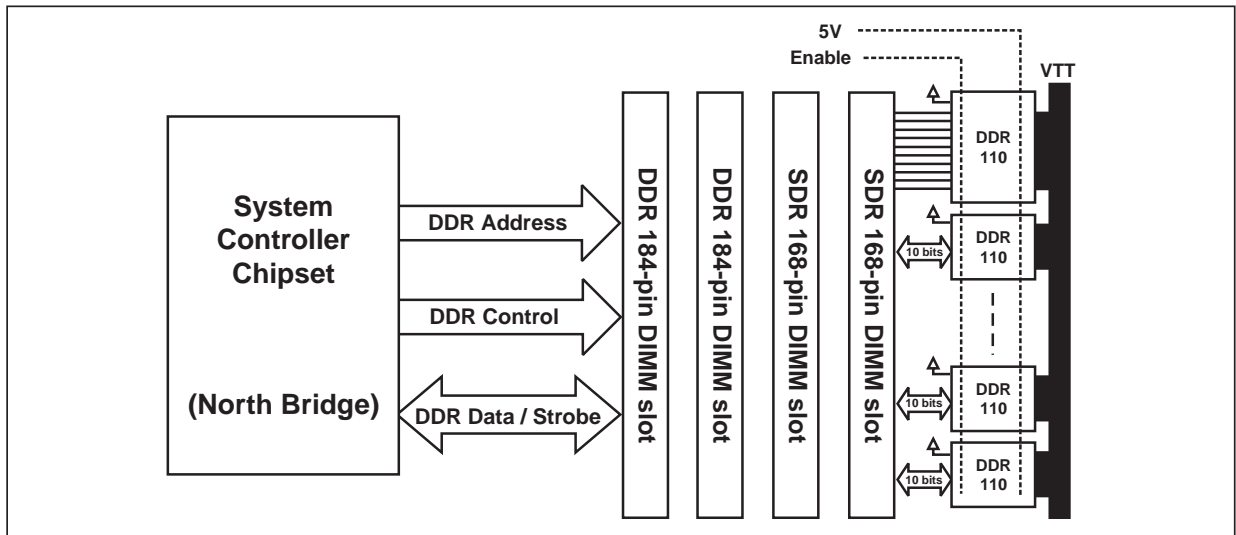
(1) Open collector output with 10k pull-up resistor to 5V is recommended for typical OE signal.

DDR110-xxT7RL

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C - V_{cc} = 5V)

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
R _{ON}	Switch ON Resistance	V _{TT} = 1.25V, V _{IN} = 0V, OE = + 5V DDR110-27 DDR110-56	22 45	27 56	32 67	Ω Ω
I _{OFF}	INPUT Leakage current Switch OFF	INPUT = + 3.3V, OE = 0V			1	μA
C _{OFF}	OFF-state capacitance	V _{IN} = 0V, 1MHz, 30mV _{RMS} , OE = 0V		6		pF

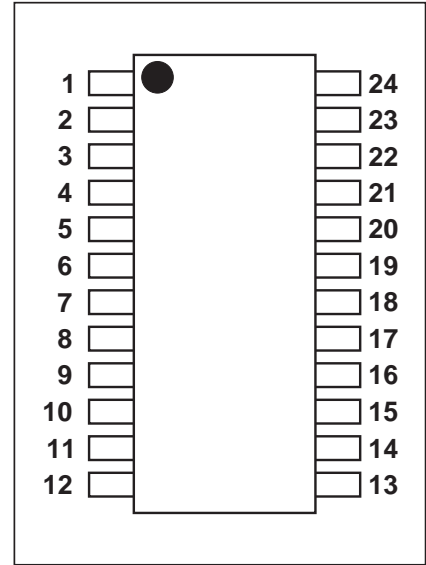
APPLICATION SCHEMATICS



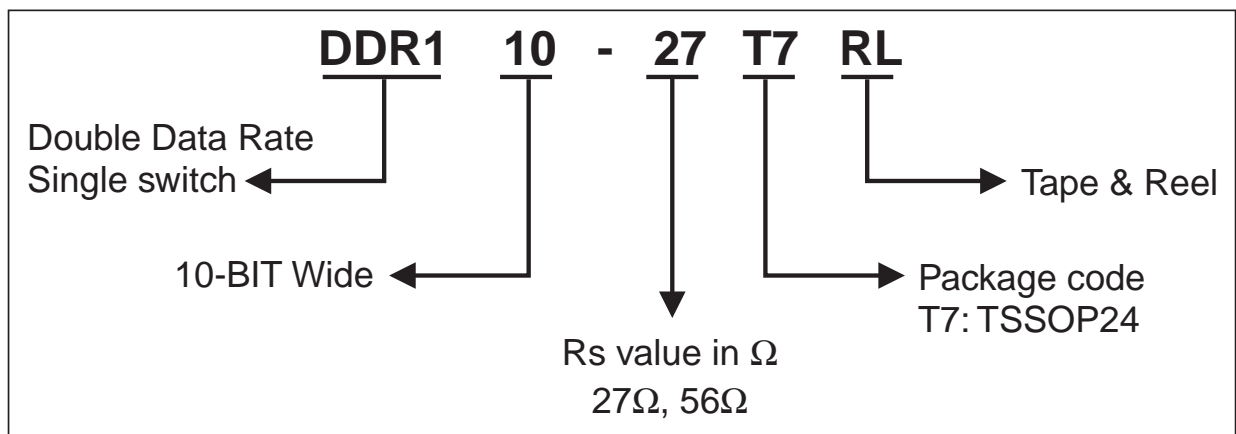
DDR110-xxT7RL

PIN ASSIGNMENT

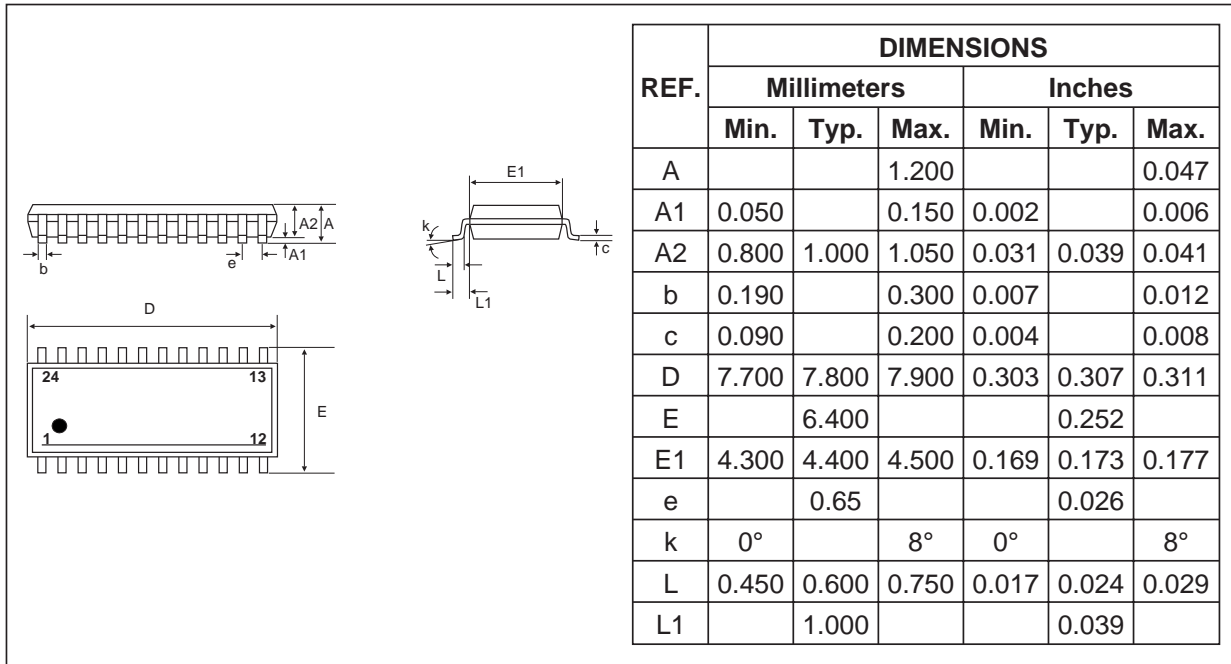
Pin #	Assignment for DDR Termination	Pin #	Assignment for DDR Termination
1	$V_{SS} = GND$	24	V_{CC}
2	A0	23	B0
3	A1	22	B1
4	A2	21	B2
5	A3	20	B3
6	A4	19	B4
7	A5	18	B5
8	A6	17	B6
9	A7	16	B7
10	A8	15	B8
11	A9	14	B9
12	Termination enable HIGH	13	Not Connected



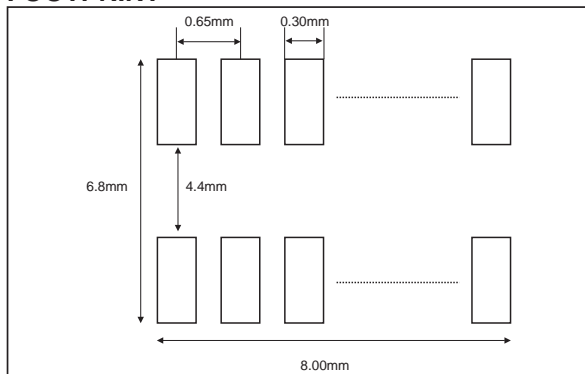
OTHER INFORMATION



PACKAGE MECHANICAL DATA
TSSOP-24



FOOTPRINT



Type	Marking	Package	Weight	Base qty	Delivery mode
DDR110-27T7RL	DDR110-27	TSSOP-24	0.088 g	2500	Tape & Reel
DDR110-56T7RL	DDR110-56	TSSOP-24	0.088 g	2500	Tape & Reel

- Epoxy meets UL94 - V0 standard

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