DDR12 SERIES

Dual output

- **High current dual-output power module for DDR memory**
- **Single compact module provides 25 A @ 2.5 V for V_{ddq} supply and 8 A @ 1.25 V for V_{tt} termination**
- **Tracking dual output voltages (1.25 V @ 8 A, 2.5 V @ 25 A)**
- **Output voltage remote sense**
- **Sink capability for logic terminations**
- **Power good output signal**
- **Overvoltage protection**
- **Overcurrent protection**
- **Remote ON/OFF**
- **Available RoHS compliant**

The dual output DDR12-25D08-AJ is specifically designed to meet the power needs of double data rate memory DIMMS and associated memory control logic. The V_{tt} output tracks the V_{ddq} output, while the V_{tt} output can sink current as required by logic terminations.This converter offers typical efficiencies greater than 84% when operated at 50% load or greater. This model features a wide input range as well as trimmable output voltages.

Remote sense on V_{ddq} and remote ON/OFF facilities are included as standard, and the converter is protected against over-current and over-voltage conditions.

[2 YEAR WARRANTY]

ARTESYN TECHNOLOGIES

File Name: lf_ddr12.pdf Rev: 29 Nov 2005

Stresses in excess of the maximum ratings can cause permanent damage to the device. Operation of the device is not implied at these or any other conditions in excess of those given in the specification. Exposure to absolute maximum ratings can adversely affect device reliability.

Absolute Maximum Ratings

Characteristic	Symbol	Min	Typ	Max	Units	Notes and Conditions
Input voltage - continuous	V_{in} (cont)	-0.3		13.2	Vdc	$V_{in(+)}$ - $V_{in(-)}$
Input voltage - nominal	V_{in} (nom)		12			
Operating temperature	T_{op}	0		80	°C	Refer to derating guidelines and Note 1
Storage temperature	$T_{storage}$	-40		125	°C	
Output current	I_{ddq} (max) I_{tt} (max)			25 8	A A	

All specifications are typical at V_{in}(nom), V_{ddq} = 2.5 V, V_{tt} = 1.25 V and full load. Tests were performed at 25 °C unless otherwise stated.

Input Characteristics

Characteristic	Symbol	Min	Typ	Max	Units	Notes and Conditions
Input voltage - operating	V_{in} (oper)	10.8	12	13.2	Vdc	
Input current - min. load	I_{in}		400		mAdc	V_{in} (min) - V_{in} (max), enabled
Input current - Quiescent	I_{in} (off)		20		mAdc	Converter disabled

Turn On/Off

Characteristic	Symbol	Min	Typ	Max	Units	Notes and Conditions
Input voltage - turn on	V_{in} (on)	10	10.2	10.4	Vdc	
Input voltage - turn off	V_{in} (off)	9.7	9.9	10.1	Vdc	
Turn on delay - enabled, then power applied	T_{delay} (power)		5		ms	With the enable signal asserted, this is the time from when the input voltage reaches the minimum specified operating voltage until the POWER GOOD is asserted high
Turn on delay - power applied, then enabled	T_{delay} (enable)		5		ms	V_{in} = V_{in} (nom), then enabled. This is the time taken until the POWER GOOD is asserted high
Output to POWER GOOD delay	T_{delay}		3		ms	Output voltage in full regulation to POWER GOOD asserted high
Rise time	T_{rise}		2		ms	

Signal Electrical Interface

Characteristic - Signal Name	Symbol	Min	Typ	Max	Units	Notes and Conditions
At remote/control ON/OFF pin Open collector or equivalent compatible						**See Notes 2 and 3** See Application Note 133 for Remote ON/OFF details
High level input voltage	V_{ih}	2.0			V	Converter guaranteed on when OUTEN pin is greater than V_{ih} (max)
Low level input voltage	V_{il}			0.80	V	Converter guaranteed off when OUTEN pin is less than V_{il} (max)
Low level input current	I_{il} (max)		1		mA	V_{il} = 0.0 V

Reliability and Service Life

Characteristic	Symbol	Min	Typ	Max	Units	Notes and Conditions
Mean time between failure	MTBF	TBD			Hours	Telcordia SR-332

Other Specifications

Characteristic	Symbol	Min	Typ	Max	Units	Notes and Conditions
Switching frequency	F_{sw}		300		kHz	Fixed frequency
Weight			34		g	

Referenced ETSI standards:

ETS 300 019: Environmental conditions and environmental tests for telecommunications equipment
ETS 300 019: Part 1-3 (1997) Classification of environmental conditions stationary use at weather protected locations
ETS 300 019: Part 2-3 (1997) Specification of environmental tests stationary use at weather protected locations

EMC
Electromagnetic Compatibility

Phenomenon	Port	Standard	Test level	Criteria	Notes and conditions
Immunity:					
ESD	Enclosure	EN61000-4-2	6 kV contact 8 kV air		As per ETS 300 386-1 table 5

Performance criteria:

NP: Normal Performance: EUT shall withstand applied test and operate within relevant limits as specified without damage.
RP: Reduced Performance: EUT shall withstand applied test. Reduced performance is permitted within specified limits, resumption to normal performance shall occur at the cessation of the test.
LFS: Loss of Function (self recovery): EUT shall withstand applied test without damage, temporary loss of function permitted during test. Unit will self recover to normal performance after test.

Referenced ETSI standards:

ETS 300 386-1 table 5 (1997): Public telecommunication network equipment, EMC requirements
ETS 300 132-2 (1996): Power supply interface at the input to telecommunication equipment: Part 2 operated by direct current (dc)
ETR 283 (1997): Transient voltages at interface A on telecommunication direct current (dc) power distributions

Material Ratings

Characteristic - Signal Name	Notes and Conditions
Flammability rating	UL94V-0
Material type	FR4 PCB

Model Numbers

Model Number	Input Voltage	Output Voltage	Output Current (Max.)	Typical Efficiency	Load Regulation
DDR12-25D08-AJ	10.8-13.2 Vdc	2.32-2.75 Vdc 1.16-1.375 Vdc	25 A 8 A	84%	±1.0% See Tracking Spec.

Input Characteristics

Characteristic	Symbol	Min	Typ	Max	Units	Notes and Conditions
Input current - operating	I_{in}		7.2		Adc	
Reflected ripple current	$I_{in\ (ripple)}$		35 50		mA rms mA pk-pk	measured with external filter. See Application Note 133 for details
Input capacitance - internal filter	C_{input}		420		µF	
Input capacitance - external filter	C_{bypass}		10		µF	Use large value ceramic

Electrical Charact. – V_{ddq} O/P

Characteristic	Symbol	Min	Typ	Max	Units	Notes and Conditions
Nominal set-point voltage	$V_{ddq\ (nom)}$		2.316		Vdc	With no external trim resistor
Output voltage range	V_{ddq}	2.316		2.750	Vdc	For details on trimming the output voltage see Application Note 133
Output set-point accuracy			±1.5	±2.5	%	Using 1% trim resistors measured at minimum load
Load regulation			+0/-1	+1/-2	%	Vary load with line held constant (Voltage typically drops with load)
Line regulation			±0.1	±0.2	%	Vary line with load held constant
Cross regulation			±0.4	±0.6		Vary load on V_{tt} with load on V_{ddq} held constant
Temperature co-efficient				0.2	mV/°C	
Ripple and noise				50	mV pk-pk	With recommended external load capacitance and 5 Hz to 20 MHz bandwidth
Load transient response - peak deviation			3		%	Peak deviation for 75% to 100% step load, di/dt = 0.04 A/µs
Load transient response - recovery			200		µs	Settling time to within 1% of output setpoint voltage for 75% to 100% step load
External load capacitance	C_{ext} (V_{ddq})	1000	1680	3000	µF	Recommended 3 x 560 µF with total ESR of 5 mΩ and additional high-quality ceramic capacitors. Consult factory for other capacitance
Overshoot				2.0	%	Nominal output at turn-on
Undershoot				150	mVdc	
Output current - continuous	I_{ddq}	1.5		25	Adc	
Output current - short circuit	I_{sc-ddq}		0		A rms	Latching short circuit protection power or enable needs to be cycled

Electrical Charact. - V_{tt} O/P

Characteristic	Symbol	Min	Typ	Max	Units	Notes and Conditions
Tracking accuracy			12	25	mV	Measured at converter pins ($=V_{ddq}/2 - V_{tt}$)
Ripple and noise				30	mV pk-pk	With recommended external load capacitance and 5 Hz to 20 MHz bandwidth
Load transient response - peak deviation			3		%	Peak deviation for 75% to 100% step load, di/dt = 8 A/µs
Load transient response - recovery			200		µs	Settling time to within 1% of output setpoint voltage for 75% to 100% step load
External load capacitance	C_{ext} (V_{tt})	1000	1680	3000	µF	Recommended 3 x 560 µF with total ESR of 5 mΩ and additional high-quality ceramic capacitors. Consult factory for other capacitance
Output current - continuous	I_{tt}	0		8	Adc	
Output current - short circuit	I_{sc-tt}		0		A rms	Latching short circuit protection power or enable needs to be cycled

Protection and Control Features

Characteristic	Symbol	Min	Typ	Max	Units	Notes and Conditions
Overcurrent limit inception	I_{ddq} I_{tt}		36 14		Adc Adc	

Efficiency

Characteristic	Symbol	Min	Typ	Max	Units	Notes and Conditions
Efficiency	η		84		%	Full load

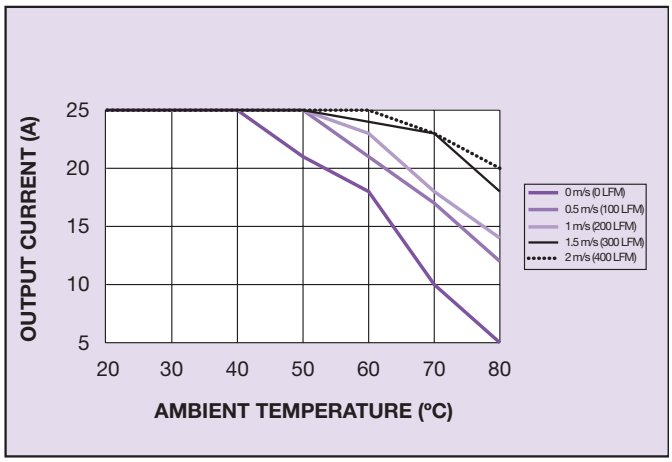


Figure 1: Thermal Derating Curve

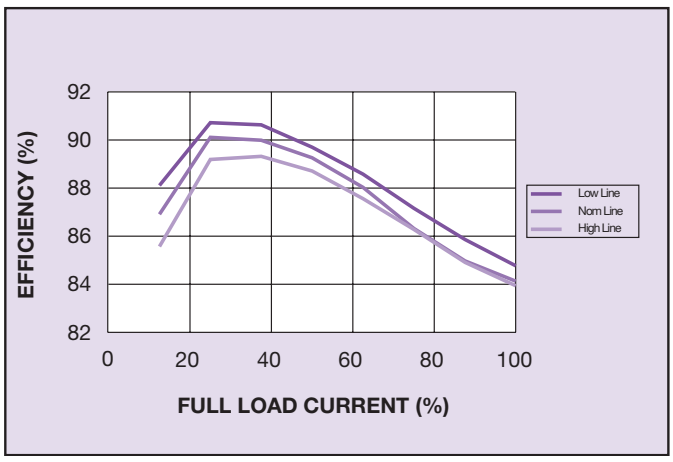


Figure 2: Efficiency vs Load and Line

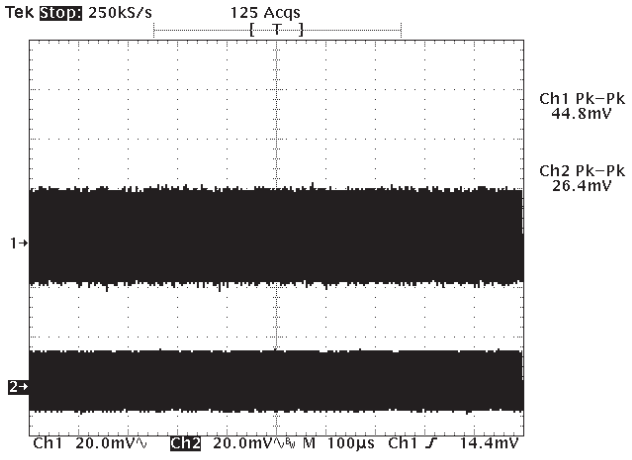


Figure 3: Typical Ripple & Noise
Channel 1: V_{ddq} Output Ripple,
Channel 2: V_{tt} Output Ripple

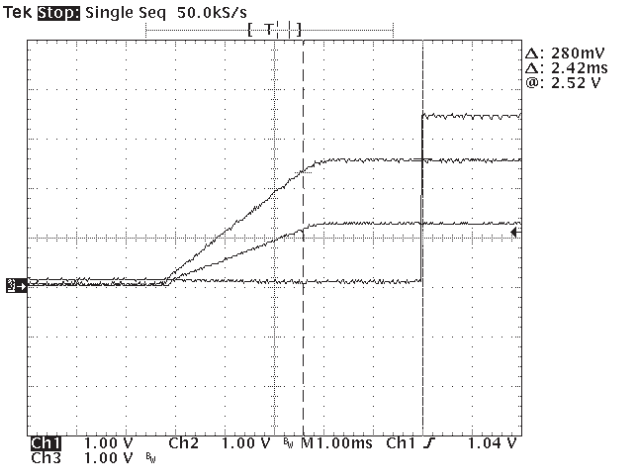


Figure 4: Typical Power-up
Channel 1: V_{ddq} Output Channel 2: V_{tt} Output
Channel 3: Power Good Signal

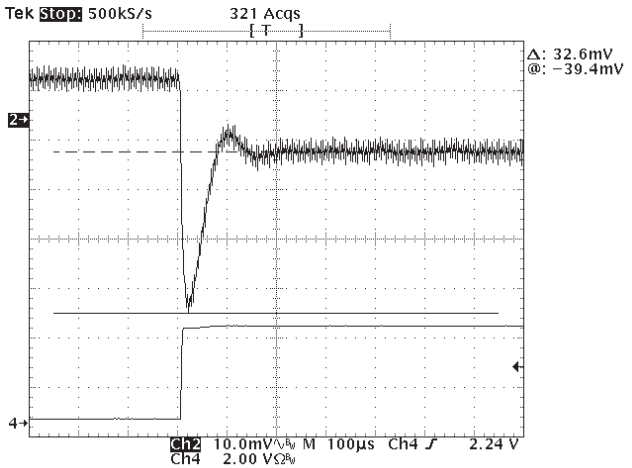


Figure 5: Transient Response 75-100% V_{tt} Source,
Rising Edge (Channel 2: V_{tt} Output Voltage Deviation,
Channel 4: Current load step at 1 A/div)

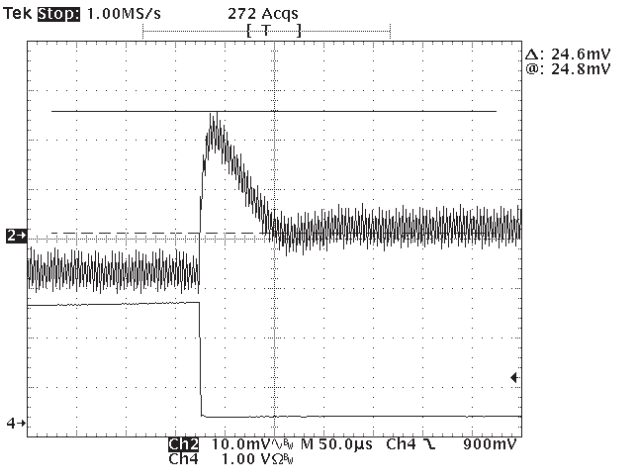


Figure 6: Transient Response 75-100% V_{tt} Source,
Falling Edge (Channel 2: V_{tt} Output Voltage Deviation,
Channel 4: Current load step at 1 A/div)

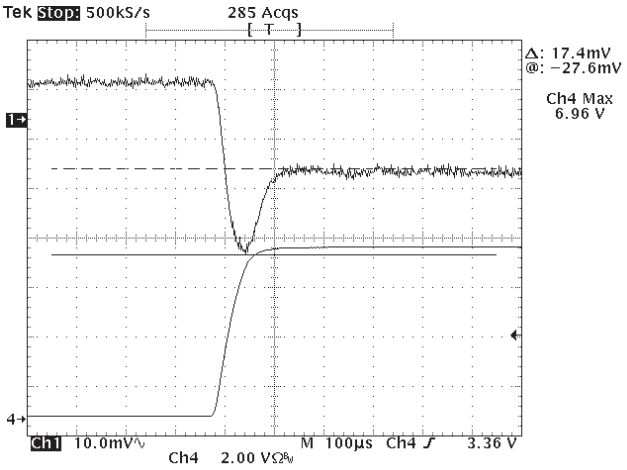


Figure 7: Transient Response 75-100% V_{ddq} Rising Edge, (Channel 1: V_{ddq} Output Voltage Deviation, Channel 4: Current load step at 2 A/div)

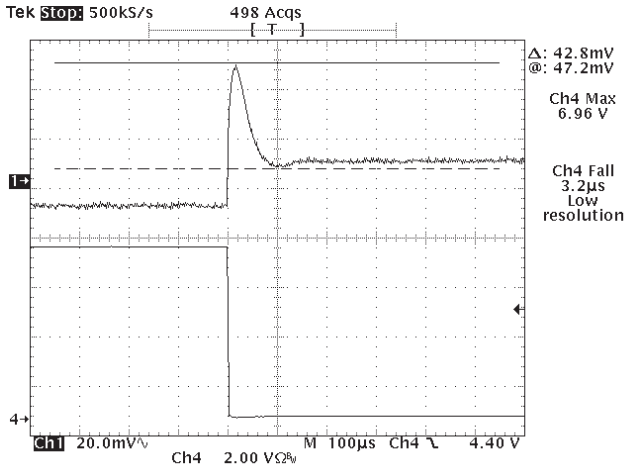


Figure 8: Transient Response 75-100% V_{ddq} Falling Edge, (Channel 1: V_{ddq} Output Voltage Deviation, Channel 4: Current load step at 2 A/div)

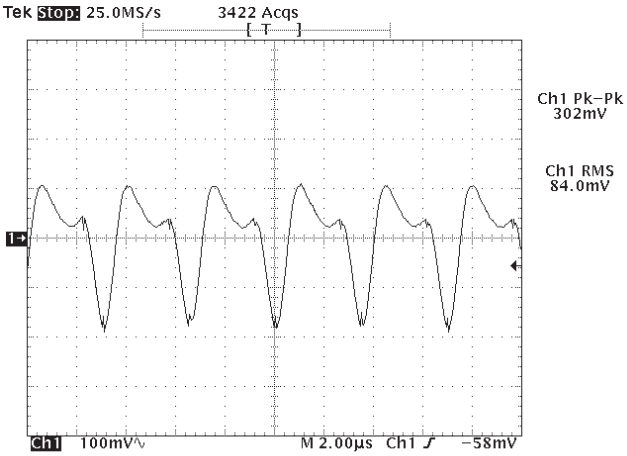
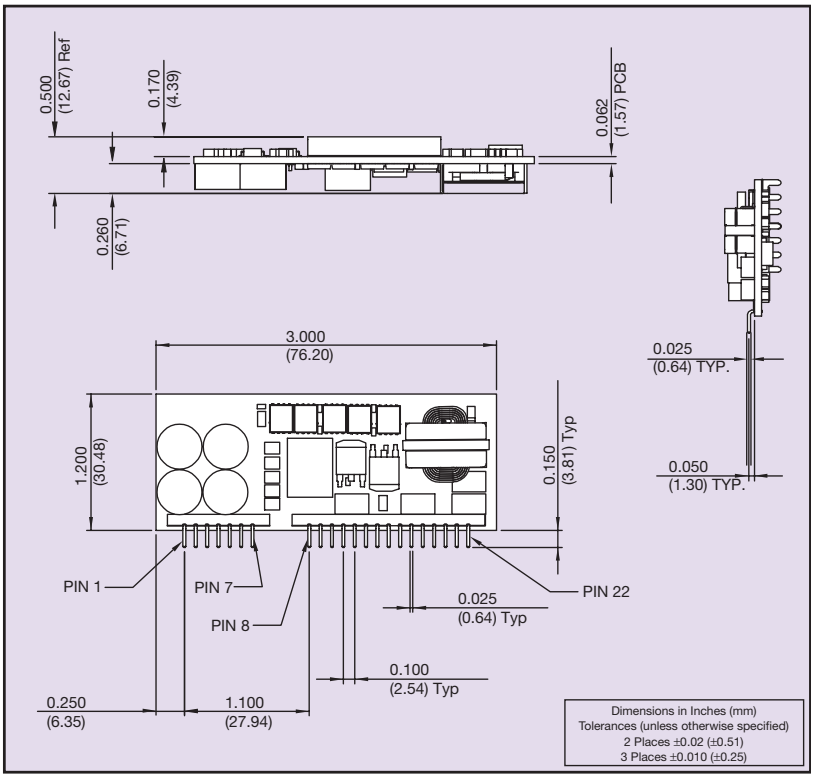


Figure 9: Input Ripple Voltage measurement, Vin = 12 V, V_{ddq} = 25 A, V_{tt} = 8 A (Channel 1: Vin Ripple Voltage)



Pin Connections

Pin No.	Function	Pin No.	Function
J1-1	Power Good	J2-5	Ground
J1-2	Output Enable	J2-6	Ground
J1-3	Ground	J2-7	Ground
J1-4	Ground	J2-8	Ground
J1-5	12V Input	J2-9	V_{ddq} Sense -
J1-6	12V Input	J2-10	V_{ddq} Sense +
J1-7	12V Input	J2-11	V_{ddq}
J2-1	V_{tt} Ref.	J2-12	V_{ddq}
J2-2	V_{tt}	J2-13	V_{ddq}
J2-3	V_{tt}	J2-14	V_{ddq}
J2-4	Ground	J2-15	V_{ddq}

Figure 10: Mechanical Drawing and Pinout Table

Note 1

For maximum reliability temperature at the Thermal Reference Point, shown in Figure 11, should not exceed 100 °C.

Note 2

The control pin is referenced to Vin-

Note 3

The DDR12 is supplied as standard with active High logic.
Control input pulled low: Unit Disabled
Control input left open: Unit Enabled

Note 4

Thermal reference set up: Unit mounted on an edge card test board 215 mm x 115 mm. Test board mounted vertically. For test details and recommended set-up see Application Note 133.

CAUTION: Hazardous internal voltages and high temperatures. Ensure that unit is accessible only to trained personnel. The user must provide the recommended fusing in order to comply with safety approvals.

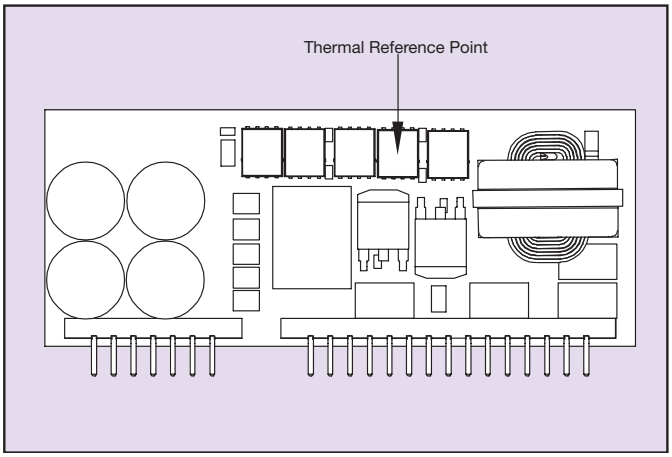


Figure 11: Thermal Reference Points

NORTH AMERICA
e-mail: sales.us@artesyn.com

☎ 800 769 7274
☎+508 628 5600

EUROPEAN LOCATIONS
e-mail: sales.europe@artesyn.com

IRELAND
☎+353 24 93130

AUSTRIA
☎+43 1 80150

FAR EAST LOCATIONS
e-mail: sales.asia@artesyn.com

HONG KONG
☎+852 2699 2868

File Name: lf_ddr12.pdf Rev: 29 Nov 2005