Analog Switches and Multiplexers

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Multiplexers

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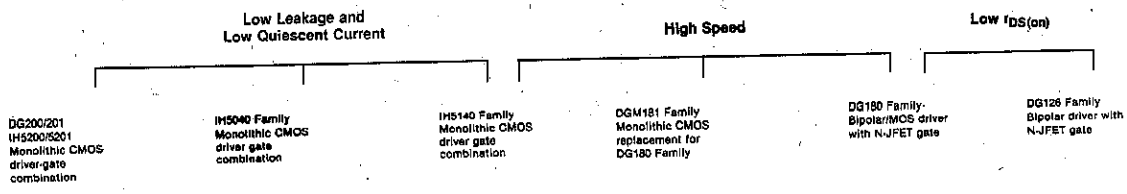
Analog Switch



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Features
1. DG200/201 industry standard
2. IH5200/5201 have far superior specs
3. IH520/DG201 have 4 individually controllable SPST switches
4. IH5200/DG200 have 2 individually controllable SPST switches

Features
1. Very low quiescent current resulting in very low power consumption
2. Low cost
3. Good speed with moderate $r_{DS(on)}$ and leakage
4. Over voltage protection to ±25V
5. Can switch up to ±13V signals with ±15V supplies

Features
1. High speed switching
2. Low quiescent current resulting in low power consumption
3. Low leakage resulting in low error term
4. Lower cost than the comparable speed DG180 family
5. Can switch signals almost to the supply rails

Features
1. Drops into DG180 family sockets. Meets or exceeds all specs
2. Lower cost than DG180
3. Lower leakages and power consumption than DG180

Features
1. Low $r_{DS(on)}$
2. As fast as the IH5140 Family
3. Moderate leakage
4. Draw high quiescent currents

Features
1. Low $r_{DS(on)}$
2. Only switch with true chip enable pin
3. Moderate leakage
4. Draw high-quiescent currents

Notes
1. TTL, DTL, CMOS and PMOS compatible
2. IH5200, DG200 — Dual SPST
   IH5201, DG201 — Quad SPST

Notes
1. TTL, DTL, CMOS, and PMOS compatible
2. 5040 through 5047 have 75Ω $r_{DS(on)}$ max @25°C
3. IH5048 thru IH5051 have 35Ω $r_{DS(on)}$ max @25°C

IH5040	SPST
IH5041/5048	Dual SPST
IH5042/5050	SPDT
IH5043/5051	Dual SPDT
IH5044	DPST
IH5045/5049	Dual DPST
IH5046	DPDT
IH5047	4PST
IH5052/5053	Quad SPST
IH200	Dual SPST
IH201/202	Quad SPST

Notes
1. TTL and CMOS compatible
2. Pin compatible with the more popular members of the DG180 family

IH5140	SPST
IH5141	Dual SPST
IH5142	SPDT
IH5143	Dual SPDT
IH5144	DPST
IH5145	Dual DPST

Notes
1. TTL, DTL, RTL and CMOS compatible
2. DGM181, 184, 187, and 190 have 30Ω max $r_{DS(on)}$
3. DGM182, 185, 188, and 191 have 75Ω max $r_{DS(on)}$

DGM181/2	Dual SPST
DGM184/5	Dual DPST
DGM187/8	SPDT
DGM190/1	Dual SPDT

Notes
1. DTL, TTL, RTL compatible
2. DG180, 183, 185 and 189 have 10Ω max on resistance but have higher leakage than others in the family
3. DG181, 184, 187 and 190 have 30Ω max $r_{DS(on)}$
4. DG182, 185, 188 and 191 have 75Ω max $r_{DS(on)}$

DG180/1/2, Dual SPST
DG183/4/5, Dual DPST
DG186/7/8, SPDT
DG189/90/1, Dual SPDT

Notes

DG133, 134, 141, 151, 152	Dual SPST
DG126, 129, 140, 153, 154	Dual DPST
DG143, 144, 146, 161, 162	Differential Input, SPDT
DG139, 142, 145, 163, 164	Differential Input, DPDT

IH5001/2	SPST
IH5003-7	Dual SPST

Selector Guide

Low Charge Injection	Video/RF Switch	For switches whose outputs go into the inverting input of an Op Amp	For switching positive signals only
IH181 Family CMOS driver and Varafet gate	IH5341 Family series shunt video/RF switch	IH5009 Virtual ground switch	IH5025 Positive signal switch
Features 1. Lowest charge injection 2. Almost as fast as IH5140 and DG180 Families 3. Very low quiescent current resulting in low power consumption 4. Ultra low leakage	**Features** 1. $r_{DS(on)}$ < 75Ω, flat from DC to 100 MHz (< 3dB) 2. "OFF" isolation > 60dB @10 MHz 3. Cross coupling isolation > 60dB @10MHz 4. +/−5V to +/−15V power supply range 5. High speed switching	Output of a switch must go into the virtual ground point of an Op Amp (unless signal is <0.2V) **Features** 1. Very low quiescent current 2. Does not need driver; can be driven directly by CMOS gates 3. Low cost	Can switch positive signals only unless a translator driver is used **Features** 1. Very low quiescent current 2. Does not need driver; can be driven directly by TTL 3. Low cost
Notes 1. TTL, HTL, CMOS and PMOS compatible 2. Pin for pin compatible with DG180 family IH181/182 Dual SPST IH184/185 Dual DPST IH187/188 SPDT IH190/191 Dual SPDT	**Notes** 1. TTL, DTL, RTL and CMOS compatible 2. IH5341 Dual SPST	**Notes** 1. All switches in IH5009 family are SPST 2. Odd numbered devices are driven by 15V logic 3. Even numbered devices are driven by 5V logic IH5009/5010 quad, compensated IH5011/5012 quad uncompensated IH5013/5014 triple compensated IH5015/5016 triple uncompensated IH5017/5018 dual compensated IH5019/5020 dual uncompensated IH5021/5022 single compensated IH5023/5024 single uncompensated	**Notes** 1. All switches in IH5025 family are SPST 2. All devices can be driven by 15V logic. All devices can be driven by 5V logic if input signal is less than 1V IH5025/5026 quad, common drain IH5027/5028 quad IH5029/5030 triple, common drain IH5031/5032 triple IH5033/5034 dual, common drain IH5035/5036 dual IH5037/5038 single

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Analog Switches with Driver

Type	No. of Channels	Intersil Device No.	Switch Technology	$r_{DS(on)}$ Ω max(1)	$I_{D(off)}$ nA max	t_{on} µs max	t_{off} µs max	Logic input: Logic Level	Logic input: Input Type(2)	Power Consumption mW
SPST	1	IH5021	P-JFET	100	0.2	0.5	0.5	TTL High Level	lo	
		IH5022	P-JFET	150	0.2	0.5	0.5	TTL Low Level	lo	
		IH5023	P-JFET	100	0.2	0.5	0.5	TTL High Level	lo	
		IH5024	P-JFET	150	0.2	0.5	0.5	TTL Low Level	lo	
		IH5037	P-JFET	100	0.5	0.2	0.2	TTL High Level	lo	
		IH5038	P-JFET	150	0.5	0.2	0.2	TTL High Level	lo	
		IH5040	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, CMOS, PMOS	hi	.035
		IH5140	CMOS	50	0.1	0.1	0.075	TTL, CMOS	hi	.035
SPST	2	DG180	N-JFET	10	10.0	0.3	0.25	DTL, TTL, RTL	lo	120
		DG181	N-JFET	30	1.0	0.15	0.13	DTL, TTL, RTL	lo	120
		DG182	N-JFET	75	1.0	0.25	0.13	DTL, TTL, RTL	lo	120
		DGM182	CMOS	75	0.1	0.25	0.13	DTL, TTL, RTL	lo	.035
		DG200	CMOS	70	1.0	0.7	0.5	DTL, TTL, RTL, CMOS, TTL High Level	lo	3.0
		IH5017	P-JFET	100	0.2	0.5	0.5	TTL, High Level	lo	
		IH5018	P-JFET	150	0.2	0.5	0.5	TTL, Low Level	lo	
		IH5019	P-JFET	100	0.2	0.5	0.5	TTL, High Level	lo	
		IH5020	P-JFET	150	0.2	0.5	0.5	TTL, Low Level	lo	
		IH5033	P-JFET	100	0.5	0.2	0.2	TTL, High Level	lo	
		IH5034	P-JFET	150	0.5	0.2	0.2	TTL, High Level	lo	
		IH5035	P-JFET	100	0.5	0.2	0.2	TTL, High Level	lo	
		IH5036	P-JFET	150	0.5	0.2	0.2	TTL, High Level	lo	
		IH5041	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, CMOS, PMOS	hi	.035
		IH5048	CMOS	35	1.0	0.25	0.15	DTL, TTL, RTL, CMOS, PMOS	hi	.035
		IH5141	CMOS	50	0.1	0.1	0.075	TTL, CMOS	hi	.035
		IH5341	CMOS	75	0.1	0.3	0.15	TTL, CMOS	hi	.035
SPST	3	IH5013	P-JFET	100	0.2	0.5	0.5	TTL, High Level	lo	
		IH5014	P-JFET	150	0.2	0.5	0.5	TTL, Low Level	lo	
		IH5015	P-JFET	100	0.2	0.5	0.5	TTL, High Level	lo	
		IH5016	P-JFET	150	0.2	0.5	0.5	TTL, Low Level	lo	
		IH5029	P-JFET	100	0.5	0.2	0.2	TTL, High Level	lo	
		IH5030	P-JFET	150	0.5	0.2	0.2	TTL, High Level	lo	
		IH5031	P-JFET	100	0.5	0.2	0.2	TTL, High Level	lo	
		IH5032	P-JFET	150	0.5	0.2	0.2	TTL, High Level	lo	
SPST	4	DG118	P-MOSFET	450	-4.0	0.3	1.0	DTL, TTL, RTL	lo	133
		DG201	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, CMOS	lo	.350
		IH5009	P-JFET	100	0.2	0.5	0.5	TTL, High Level	lo	
		IH5010	P-JFET	150	0.2	0.5	0.5	TTL, Low Level	lo	
		IH5011	P-JFET	100	0.2	0.5	0.5	TTL, High Level	lo	
		IH5011	P-JFET	150	0.2	0.5	0.5	TTL, Low Level	lo	
		IH5025	P-JFET	100	0.5	0.2	0.2	TTL High Level	lo	
		IH5026	P-JFET	150	0.5	0.2	0.2	TTL High Level	lo	
		IH5027	P-JFET	100	0.5	0.2	0.2	TTL High Level	lo	
		IH5028	P-JFET	150	0.5	0.2	0.2	TTL High Level	lo	
		IH5052	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, CMOS, PMOS	lo	.350
		IH5053	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, CMOS, PMOS	hi	.350
SPST	5	DG123	P-MOSFET	450	-4.0	0.3	1.0	DTL, TTL, RTL	hi	133
		DG125	P-MOSFET	450	-4.0	0.3	1.0	DTL, TTL, RTL	lo	133
		DG143A	N-JFET	80	1.0	0.4	0.8	DTL, TTL, RTL	(3)	84
		DG144A	N-JFET	30	1.0	0.4	0.8	DTL, TTL, RTL	(3)	84
		DG146A	N-JFET	10	10.0	0.5	1.25	DTL, TTL, RTL	(3)	84
		DG161A	N-JFET	15	10.0	0.5	1.25	DTL, TTL, RTL	(3)	90
		DG162A	N-JFET	50	2.0	0.4	0.8	DTL, TTL, RTL	(3)	90
		DG186	N-JFET	10	10.0	0.3	0.25	DTL, TTL, RTL	(3)	73
		DG187	N-JFET	30	1.0	0.15	0.13	DTL, TTL, RTL	(3)	73
SPDT	1	DG188	N-JFET	75	1.0	0.25	0.13	DTL, TTL, RTL	(3)	73
		DGM188	CMOS	75	0.1	0.25	0.13	DTL, TTL, RTL	(3)	.035
		IH5042	CMOS	75	1.0	0.05	0.025	DTL, TTL, RTL PMOS, CMOS	(3)	.035
		IH5050	CMOS	35	1.0	0.25	0.15	DTL, TTL, RTL PMOS, CMOS	(3)	.035
		IH5142	CMOS	50	0.1	0.175	0.125	TTL, CMOS	(3)	.035

Analog Switches with Driver continued

Type	No. of Channels	Device No.	Switch Technology	$r_{DS(on)}$ Ω max(1)	$I_{D(off)}$ nA max	t_{on} µs max	t_{off} µs max	Logic Input: Logic Level	Logic Input: Input Type(2)	Power Consumption mW
		DG189	N-JFET	10	10.0	0.3	0.25	DTL, TTL, RTL	(3)	120
		DG190	N-JFET	30	1.0	0.15	0.13	DTL, TTL, RTL	(3)	120
		DG191	N-JFET	75	1.0	0.25	0.13	DTL, TTL, RTL	(3)	120
		DGM191	CMOS	75	0.1	0.25	0.13	DTL, TTL, RTL	(3)	.035
SPDT	2	IH5043	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, PMOS, CMOS	(3)	.035
		IH5051	CMOS	35	1.0	0.25	0.15	DTL, TTL, RTL, PMOS, CMOS	(3)	.035
		IH5143	CMOS	50	0.1	0.175	0.125	TTL, CMOS	(3)	.035
DPST	1	IH5044	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, CMOS, PMOS	hi	.035
		IH5144	CMOS	50	0.1	0.175	0.125	TTL, CMOS	hi	.035
		DG183	N-JFET	10	10.0	0.3	0.25	DTL, TTL, RTL	hi	84
		DG184	N-JFET	30	1.0	0.15	0.13	DTL, TTL, RTL	hi	84
		DG185	N-JFET	75	1.0	0.25	0.13	DTL, TTL, RTL	hi	84
DPST	2	DGM185	CMOS	75	0.1	0.25	0.13	DTL, TTL, RTL	hi	.035
		IH5045	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, PMOS, CMOS	hi	.035
		IH5049	CMOS	35	1.0	0.25	0.15	DTL, TTL, RTL, PMOS, CMOS	hi	.035
		IH5145	CMOS	50	0.1	0.175	0.125	TTL, CMOS	hi	.035
		DG139A	N-JFET	30	1.0	0.4	0.8	DTL, TTL, RTL	(3)	84
		DG142A	N-JFET	80	1.0	0.4	0.8	DTL, TTL, RTL	(3)	84
DPDT	1	DG145A	N-JFET	10	10.0	0.5	1.25	DTL, TTL, RTL	(3)	84
		DG163A	N-JFET	15	10.0	0.5	1.25	DTL, TTL, RTL	(3)	90
		DG164A	N-JFET	50	2.0	0.4	0.8	DTL, TTL, RTL	(3)	90
		IH5046	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL CMOS, PMOS	(3)	.035
4PST	1	IH5047	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL CMOS, PMOS	hi	.035

Multiplexers

Type	No. of Channels	Device No.	Switch Technology	$r_{DS(on)}$ Ω max(1)	$I_{D(off)}$ nA max	t_{on} µs max	t_{off} µs max	Logic Input: Logic Level	Logic Input: Input Type(2)	Power Consumption mW
CMOS	1 of 8	IH6108	CMOS	300	0.1	1.5	1.0	DTL, TTL, RTL, CMOS	hi	4.5
CMOS	1 of 16	IH6116	CMOS	600	0.2	1.5	1.0	DTL, TTL, RTL, CMOS	hi	4.5
CMOS	2 of 8	IH6208	CMOS	300	0.1	1.5	1.0	DTL, TTL, RTL, CMOS	hi	4.5
CMOS	2 of 16	IH6216	CMOS	600	0.2	1.5	1.0	DTL, TTL, RTL, CMOS	hi	4.5
CMOS Fault Protected	1 of 8	IH5108	CMOS	700	0.1	1.5	1.0	DTL, TTL, RTL, CMOS	hi	4.5
	2 of 8	IH5208	CMOS	700	0.1	1.5	1.0	DTL, TTL, RTL, CMOS	hi	4.5

Drivers for FET Switches

Electrical Characteristics @ +25°C—Military Temperature Devices

No. of Channels	Device No.	V_{OUT} Positive Volts	V_{OUT} Negative Volts	t_{on} ns max	t_{off} ns max	I_{INL} µA (max)	I_{INH} mA (max)	Logic Input Level	Power Consumption (mW)
2	IH6201	+14.0	-14.0	200	300	1.0	1.0	TTL	350
4	D129	V_{supply}	-19.3	250	1000	200	0.25µA	TTL/DTL	55
6	D123	V_{supply}	-19.7	250	600	1.0	1.0µA	TTL/DTL	20
	D125	V_{supply}	-19.7	250	600	1.0	1.5µA	TTL	50

RF/VIDEO SWITCH

Type	No. of Channels	Device No.	$r_{DS\ (ON)}$ Ω Max.	Off Isolation	Logic Input	Power Consumption (mW)
CMOS	2	IH5341	75.	>60dB @ 10 MHz	TTL, CMOS	0.030

Notes:
1. Switch Resistance under worst case analog voltage.
2. Positive logic LO ("0") or HI ("1") voltage at driver input necessary to turn switch on.
3. Logic "0" or "1" can be arbitrarily assigned for double-throw switches.
4. Switch resistance under best case analog voltage.

DG118/123/125
4 and 5-Channel Driver-MOS-FET Switch Combinations

FEATURES

- Available With and Without Programmable Constant Current pull-up
- Zener Protection on All Gates
- P-Channel Enhancement-Type MOS-FET Switches
- Each Switch Summed to One Common Point

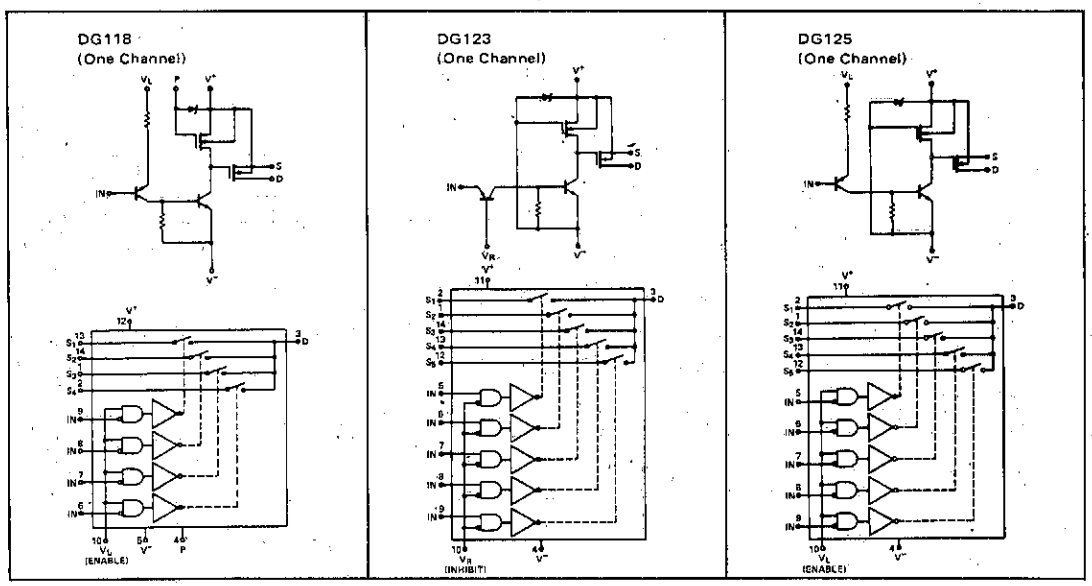
GENERAL DESCRIPTION

This series includes devices with four and five channel switching capability. Each channel is composed of a driver and a MOS-FET switch. Two driver versions are supplied for inverting and noninverting applications. A MOS-FET, used as a current source provides an active pull-up for faster switching.

An external biasing connection is brought out for biasing the current source for optimization of speed and power.

3

SCHEMATIC AND LOGIC DIAGRAMS (Outline Dwgs DD, FD-2, JD)



ORDERING INFORMATION

DG118 A K

- Package
  - K — 14-pin CERDIP
  - L — 14-pin Flat Package
  - P — 14-Pin Ceramic DIP (Special Order Only)
- Temperature Range
  - A — Military (−55°C to +125°C)
  - B — Industrial (−20°C to +85°C)
- Device Chip Type

TRUTH TABLE

DG123		DG118, DG125		Switch Cond.
V_{IN}	V_R	V_{IN}	V_L	
L	L	L	L	OFF
H	L	L	H	ON
L	H	H	L	OFF
H	H	H	H	OFF

L = 0V, H = +V

ABSOLUTE MAXIMUM RATINGS

Collector to Emitter ($V^+ - V^-$) 33V
Collector to Pull-up ($V^+ - V_P$) 33V
Drain to Emitter ($V_D - V^-$) 32V
Source to Emitter ($V_S - V^-$) 32V
Drain to Source ($V_D - V_S$) 28V
Source to Drain ($V_S - V_D$) 28V
Logic to Emitter ($V_L - V^-$) 33V
Reference to Emitter ($V_R - V^-$) 31V
Reference to Input ($V_R - V_{IN}$) 6V
Logic to Input ($V_L - V_{IN}$) . . . . . ±6V

Input to Emitter ($V_{IN} - V^-$) 33V
Current (any terminal) 30mA
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature . . . . . −55°C to +125°C
Dissipation (Note) 750mW
Lead Temperature (soldering, 10 sec.) . . . . . 300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature of 70°C. Derate 10mW/°C for higher ambient temperature.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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ELECTRICAL CHARACTERISTICS

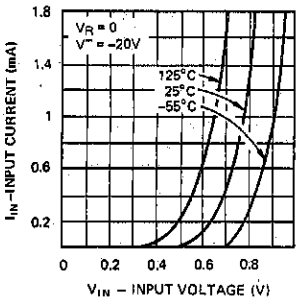
Test conditions unless specified otherwise are as follows: $V_L = 4.5V$, $V_R = 0$, $V^- = -20V$, and $P = -20V$. Input ON and OFF test conditions used for output and power supply specifications.

		PARAMETER (NOTE)	MAX LIMITS				CONDITIONS
			−55°C	+25°C	+125°C	UNITS	
INPUT	DG123	$I_{IN(OFF)}$	1	1	100	μA	$V_{IN} = 0.4V$
		$V_{IN(ON)}$	1.3	1.0	0.8	V	$I_{IN} = 1mA$
	DG118 DG125	$I_{IN(OFF)}$	1	1	20	μA	$V_{IN} = 4.1V$
		$I_{IN(ON)}$	−0.7	−0.7	−0.7	mA	$V_{IN} = 0.5V$
OUTPUT	All circuits	$r_{DS(ON)}$	100	100	125	Ω	$V_D = 10V$, $I_S = -1mA$
			200	200	250	Ω	$V_D = 0$, $I_S = -100\,\mu A$
			450	450	600	Ω	$V_D = -10V$, $I_S = -100\,\mu A$
		$I_{D(ON)}$		4	4000	nA	$V_D = 10V$, $I_{S(all)} = 0$
		$I_{D(OFF)}$		−4	−4000	nA	$V_{S(all)} = 10V$, $V_D = -10V$
		$I_{S(OFF)}$		−1	−1000	nA	$V_D = 10V$, $V_S = -10V$
POWER SUPPLY	All circuits	$I_{CC(ON)}$		3		mA	One Channel (ON)
		$I_{L(ON)}$		3		mA	
		$I_{R(ON)}$		−0.5		mA	
		$I_{EE(ON)}$		−6		mA	
	All circuits	$I_{CC(OFF)}$		10		μA	All Channels (OFF)
		$I_{L(OFF)}$		10		μA	
		$I_{R(OFF)}$		−15		μA	
		$I_{EE(OFF)}$		−20		μA	
SWITCHING TIMES	All circuits	$t_{(ON)}$		0.3		μs	See Switching Times
		$t_{(OFF)}$		1		μs	

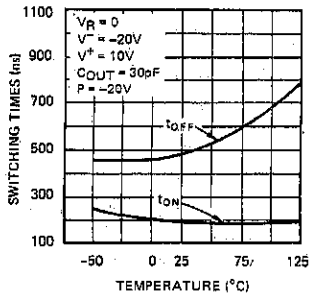
NOTE: (OFF) and (ON) subscript notation refers to the conduction state of the MOS-FET switch for the given test condition.

TYPICAL CHARACTERISTICS

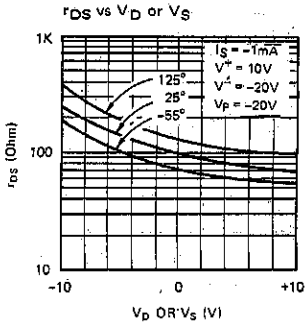
I_{IN} vs V_{IN} DG123



SWITCHING TIMES vs TEMPERATURE



r_{DS} vs V_D or V_S



APPLICATION TIPS

3

The recommended resistor values for interfacing RTL, DTL, and T^2L Logic are shown in Figures 1 and 2.

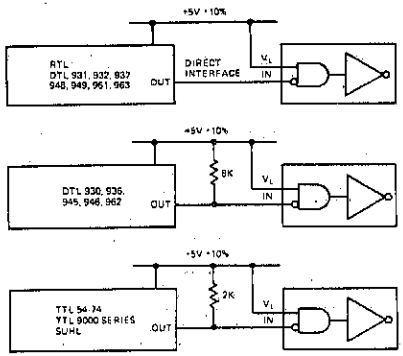


Figure 1. DG118 and DG125 Interface

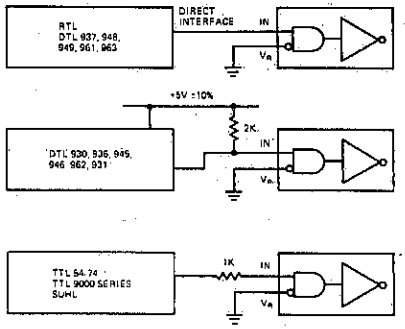
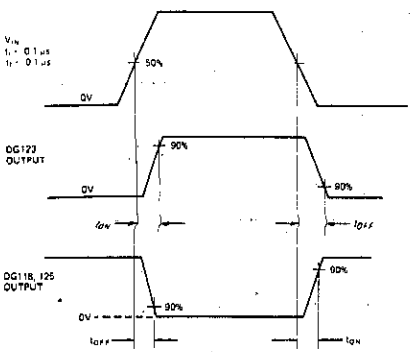


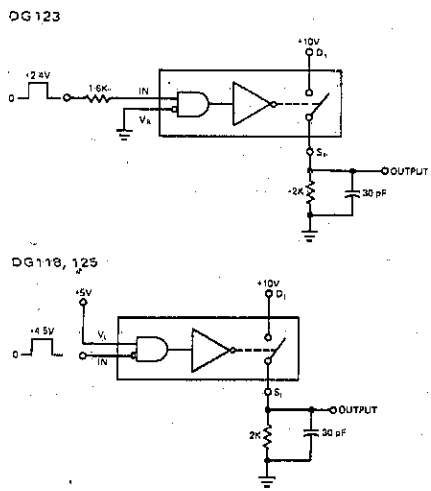
Figure 2. DG123 Interface

Enable Control

The V_R and V_L terminals can be used as either a Strobe or an Enable control. The requirements for sinking current at V_R or sourcing current at V_L are: $I_{L(ON)}$ x No. of channels used, for DG118 and DG125, and $I_{R(ON)}$ x No. of channels used, for the DG123 devices. The voltage at V_L must be greater than the voltage at V_{IN} by at least + 4V.

SWITCHING TIMES





D123/D125
6-Channel FET Switch Drivers

FEATURES

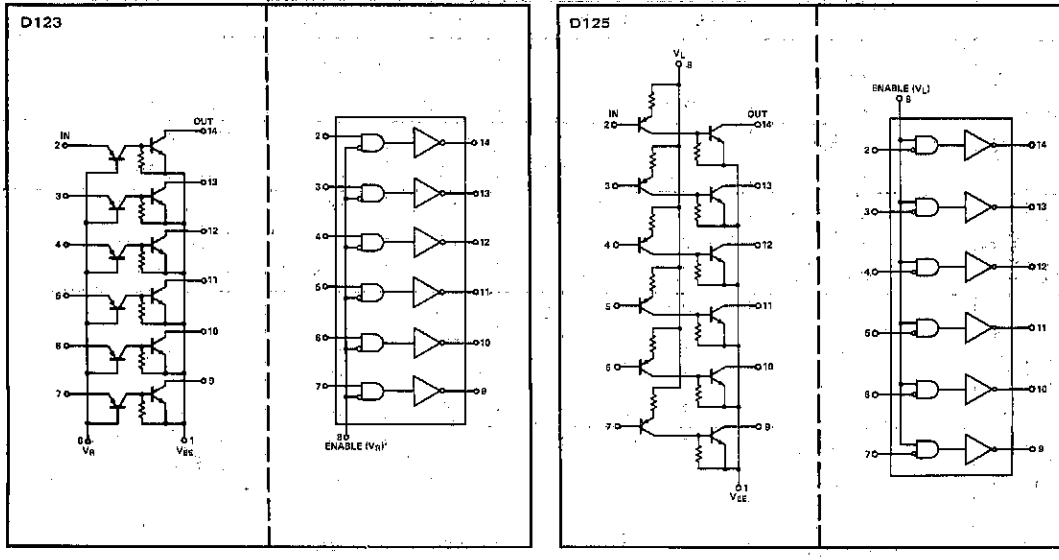
- Provides DC level shifting between low-level Logic and MOS-FET or J-FET switches
- External Collector Pull-ups required
- Direct interface with G116, G117, G119, G115, and G123 MOS-FET switches

GENERAL DESCRIPTION

The D123 and D125 monolithic bi-polar drivers convert low-level positive signals (0 & +5V) to the high level positive and negative voltages necessary to drive FET switches. One lead can be used to provide an enabling capability.

3

SCHEMATIC AND LOGIC DIAGRAMS (Outline Dwgs DD, FD-2, JD)



ORDERING INFORMATION

D123 A K

Package
K — 14-Pin CERDIP
L — 14-Pin Flat Pack
P — 14-Pin Hermetic DIP (Special Order Only)

Temperature Range
A — Military (−55°C to +125°C)
B — Industrial (−20°C to +85°C)

Device Chip Type

ABSOLUTE MAXIMUM RATINGS

Input-to-Emitter Voltage ($V_{IN} - V_{EE}$)	33V
Output-to-Emitter Voltage ($V_O - V_{EE}$)	33V
Logic Supply-to-Emitter Voltage ($V_L - V_{EE}$)	27V
Input-to-Reference Voltage ($V_{IN} - V_R$)	2V
Input-to-Logic Supply Voltage ($V_{IN} - V_L$)	+6V
Reference-to-Emitter Voltage ($V_R - V_{EE}$)	31V
Maximum Dissipation (Note)	750 mW
Current (any pin)	30 mA

Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature of 70°C. Derate 10 mW/°C for higher ambient temperature.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

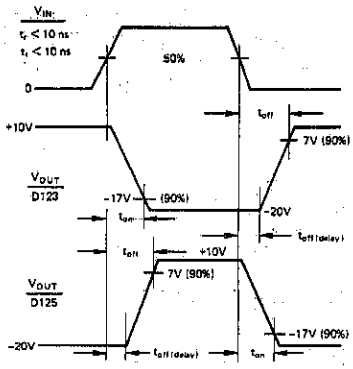
Test conditions unless otherwise specified are as follows: V_{EE} = −20V, V_L = 4.5V, I_{OUT} = 0, V_R = 0. Output and power supply measurements based on specified input conditions.

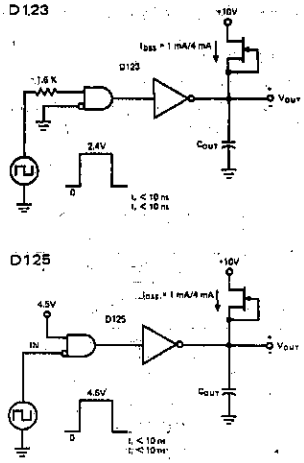
3

		PARAMETER	MAX LIMIT −55°C	MAX LIMIT 25°C	MAX LIMIT 125°C	UNITS	CONDITIONS
INPUT	D123	$I_{IN(OFF)}$	1	1	100	µA	V_{IN} = 0.4V
		$V_{IN(ON)}$	1.3	1	0.8	V	I_{IN} = 1 mA
	D125	$I_{IN(OFF)}$	1	1	20	µA	V_{IN} = 4.1V
		$I_{IN(ON)}$	−0.7	−0.7	−0.7	mA	V_{IN} = 0.5V
OUTPUT	D125 & D123	$I_{OUT(OFF)}$	0.1	0.1	10	µA	V_{OUT} = +10V
		$V_{OUT(ON)}$	−19.7	−19.7	−19.5	V	I_{OUT} = 1 mA
		$V_{OUT(ON)}$	−19.2	−19.2	−19.0	V	I_{OUT} = 4 mA
POWER SUPPLY	D123	$I_{R(ON)}$ (1)	0.5	0.5	0.5	mA	I_{OUT} = 0 for ON measurements. V_{OUT} = +10V for OFF measurements.
		$I_{R(OFF)}$ (2)	1	1	150	µA	
		$I_{EE(ON)}$ (1)	1	1	1	mA	
		$I_{EE(OFF)}$ (2)	2	2	200	µA	
	D125	$I_{L(ON)}$ (1)	2	2	1.9	mA	
		$I_{L(OFF)}$ (2)	1	1	100	µA	
		$I_{EE(ON)}$ (1)	2	2	1.9	mA	
		$I_{EE(OFF)}$ (2)	2	2	200	µA	
SWITCHING TIMES	D125 & D123	$t_{(on)}$		250		ns	I_{OUT} = 1 mA C_{OUT} (3) = 10 pF
		$t_{(off)}$ (4)		800		ns	(See Switching Times)
		$t_{(on)}$		250		ns	I_{OUT} = 4 mA C_{OUT} (3) = 10 pF
		$t_{(off)}$ (5)		600		ns	(See Switching Times)

NOTES: (1) One channel ON, 5 channels OFF.
(2) All channels OFF.
(3) Add 30 ns per pF for 1 mA and add 8 ns per pF for 4 mA for additional capacitive loading.
(4) For Dual-In-Line package add 120 ns to $t_{(off)}$.
(5) For Dual-In-Line package add 30 ns to $t_{(off)}$.

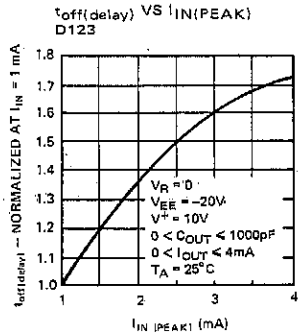
SWITCHING TIMES

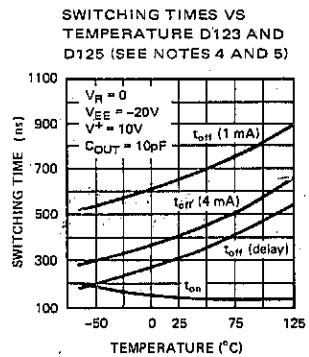


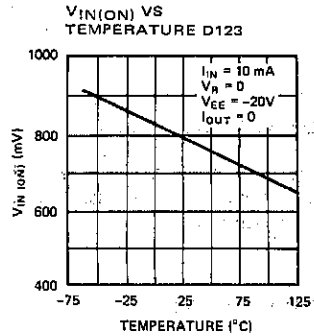


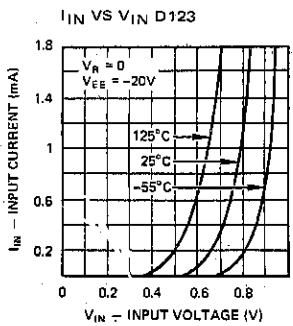
Circuit Diagrams

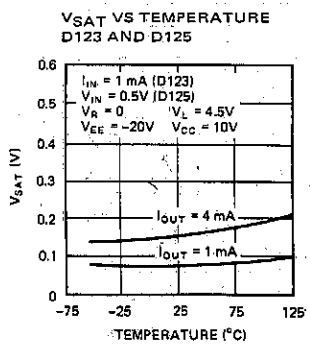
TYPICAL CHARACTERISTICS

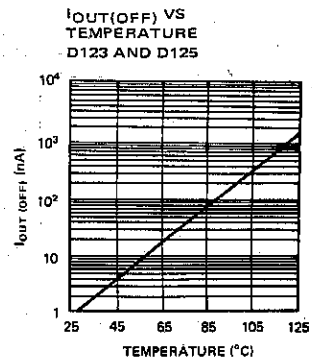










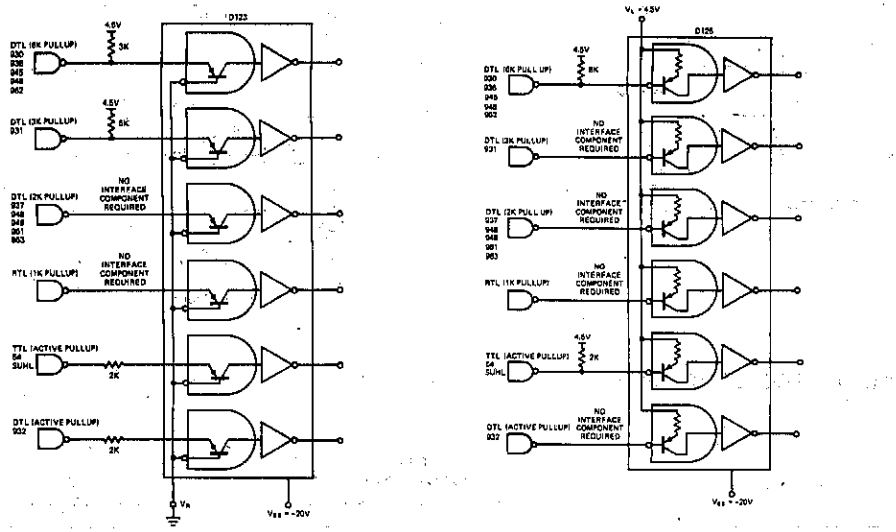


APPLICATION TIPS

Interfacing the D123 and D125

In order to meet all the specifications on this data sheet, certain requirements must be met by the drive circuitry.

The D125 can be turned ON easily, but care must be exercised to insure turn-off. Keeping $V_L - V_{IN} \leq 0.4V$ is a must to insure turn-off. To accomplish this a shunt resistor must be added to supply the leakage current (I_{CES}) for DTL devices. Since I_{CES} = 50 μA, a 0.4V/0.05 mA = 8k or less should be used. For T^2L devices using a 2k resister will insure turn-off with up to 200 μA of leakage current.

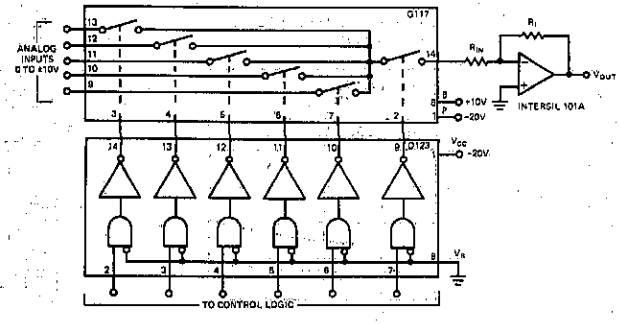


Using the ENABLE Control

Device pins V_R or V_L, can be used to enable the D123 or D125 drivers. For the D123 the enabling driver must sink $I_{R(ON)}$ X no. of channels used. For the D125, $I_{L(ON)}$ X no. of channels used must be sourced with a voltage at least +4V greater than V_{IN}.

APPLICATIONS

Using INTERSIL'S MOS-FET SWITCH G117 with either the D123 or D125 drivers provides a reliable means of providing up to 5 channels with a series block for multiplexing applications.



5-Channel Multiplexer

D129
4-Channel MOS FET Switch Driver with Decode

FEATURES

- Quad Three-Input Gates Decode Binary Counter to Four Lines
- Inputs Compatible with Low Power TTL and DTL, I_F = 200μA Max
- Output Current Sinking Capability 10mA
- External Pull-Up Elements Required
- Compatible with G115 and G123 Series Multichannel MOS FET Switches which include Current-Limiter Pull-Up FETs

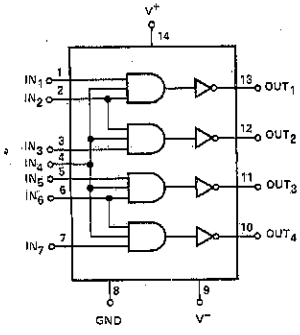
GENERAL DESCRIPTION

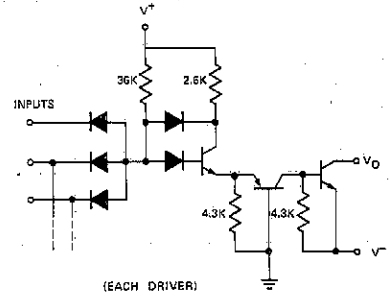
The D129 is a 4-channel driver with binary decode input. It has been designed to provide the DC level-shifting required to interface low-level logic outputs (0.7 to 2.2V) to field-effect transistor inputs (up to 50V peak-to-peak). For a 5V input logic supply, the V^- terminal can be set at any voltage between −5V and −30V. The output transistor is capable of sinking 10mA and will stand-off up to 50V above V^- in the off-state.

The ON state of the driver is controlled by a logic "1" (open) on all three input logic lines, while the OFF state of the driver is achieved by pulling any one of the three inputs to a logic "0" (ground).

The 4-channel driver is internally connected such that each one can be controlled independently or decoded from a binary counter.

SCHEMATIC AND LOGIC DIAGRAMS (Outline Dwgs DD, FD-2, JD)





ORDERING INFORMATION

D129 A K

- K — Package: K — 14-pin CERDIP; L — 14-pin Flat Pak; P — 14-pin Ceramic DIP (Special Order Only)
- A — Temperature Range: A — −55°C to +125°C; B — −20°C to +85°C
- D129 — Device Chip Type

ABSOLUTE MAXIMUM RATINGS

$V_O - V^-$ 50V
GND – V^- 33V
V^+ – GND 8V
V_{IN} – GND . . . . . ±6V
Current (any terminal) 30mA
Storage Temperature . . . . . –65°C to +150°C
Operating Temperature . . . . . –55°C to +125°C
Power Dissipation (note) 750mW
Lead Temperature (Soldering, 10 sec) . . . . . 300°C

Note: Dissipation rating assumes device mounted with all leads welded or soldered to pc board in ambient temperature of 70°C. Derate 10mW/°C for higher ambient termperatures.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

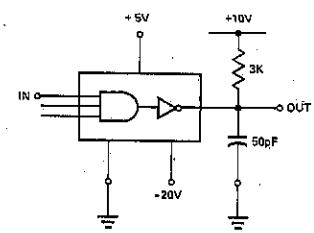
3

ELECTRICAL CHARACTERISTICS Test conditions unless otherwise specified $V^- = -20V$, $V^+ = 5V$

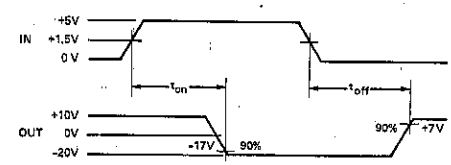
	PARAMETER		CONDITIONS		MAX LIMITS D129M –55°C	D129M 25°C	D129M 125°C	D129I –20°C	D129I 25°C	D129I 85°C	UNIT
OUT	V_{OL}	Output Voltage, Low	I_O = 10mA	V_{IN} = 2.2V, V^+ = 4.5V	-19.3	-19.3	-19	-19.25	-19.25	-19	V
OUT	V_{OL}	Output Voltage, Low	I_O = 1mA	V_{IN} = 2.2V, V^+ = 4.5V	-19.8	-19.8	-19.75				V
OUT	I_{OH}	Output Current, High	V_O = 10V, V_{IN} = 0.7V		0.1	0.1	20	0.2	0.2	10	µA
IN	I_{INH}*	Input Current Input Voltage High	V_{IN} = 5V Input Under Test, V_{IN} = 0 All Other Inputs		0.25	0.25	5	1	1	5	µA
IN	I_{INL}*	Input Current, Input Voltage Low	V_{IN} = 0, V^+ = 5.5V		-250	-200	-160	-250	-225	-200	µA
TIME	t_{on}	Turn-ON Time	See Switching Time Test Circuit			0.25			0.3		µs
TIME	t_{off}	Turn-OFF Time	See Switching Time Test Circuit			1.0			1.5		µs
SUPPLY	I_{EE}	Negative Supply Current	V^- = –20V, V^+ = 5.5V	One Channel "ON"		- 2			- 2.25		mA
SUPPLY	I_L	Logic Supply Current	V^- = –20V, V^+ = 5.5V	One Channel "ON"		3			3.3		mA
SUPPLY	I_{EE}	Negative Supply Current	V^- = –20V, V^+ = 5.5V	All V_{IN} = 0, All Channels "OFF"		-10			-25		µA
SUPPLY	I_L	Logic Supply Current	V^- = –20V, V^+ = 5.5V	All V_{IN} = 0, All Channels "OFF"		0.75			1		mA

*Per gate Input

SWITCHING TIME AND TEST CIRCUIT



t_f = 100ns
t_r = 100ns
t_{pw} = 1µs
f = 100K Hz



INTERSIL DG139, DG142 — DG146, DG161 — DG164

Drivers with Differentially Driven FET Switches

FEATURES

- Each channel complete-interfaces with most integrated logic
- Low OFF power dissipation, 1 mW
- Switches analog signals up to 20 volts peak-to-peak
- Low $r_{DS(ON)}$, 10 ohms max on DG145 and DG146

GENERAL DESCRIPTION

Each package contains a monolithic driver with differential input and 2 or 4 discrete FET switches. The driver may be treated as a special purpose differential amplifier which controls the conduction state of the FET switches. The differential output of the driver sets the switches in opposition, one pair open and the other pair closed. All switches may be opened by applying a positive control signal to the V_R terminal.

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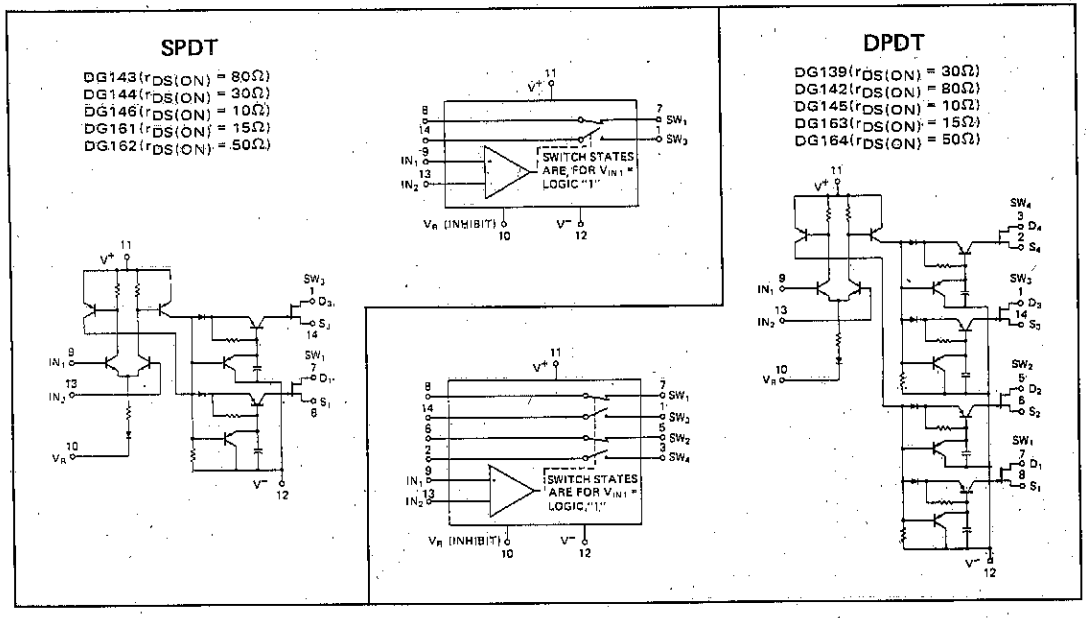
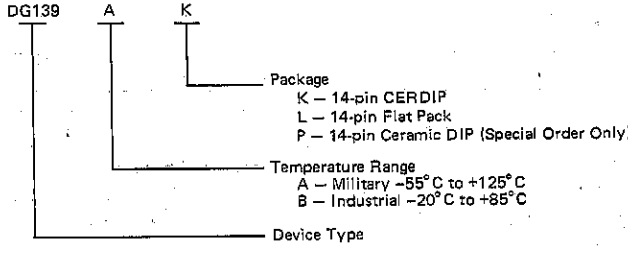
SCHEMATIC AND LOGIC DIAGRAMS (Outline Dwgs DD, FD-2, JD)



ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS

$V^+ - V^-$ 36V
$V_S - V^-$ 30V
$V^+ - V_S$ 30V
$V_S - V_D$ . . . . . ±22V
$V_R - V^-$ 21V
Power Dissipation (Note) . . . . . 750 mW
Current (any terminal) . . . . . 30 mA

$V^+ - V_R$ 17V
$V^+ - V_{IN1}$ or V_{IN2} . 14V
$V_{IN1} - V_{IN2}$ . . . . . ±6V
$V_{IN1} - V_R$ . . . . . ±6V
$V_{IN2} - V_R$ . . . . . ±6V

Storage Temperature . . . . . -65 to +150°C
Operating Temperature . . . . . -55 to +125°C
Lead Temperature (soldering, 10 sec) . . . . . 300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 70°C. For higher temperature, derate at rate of 10 mW/°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3

ELECTRICAL CHARACTERISTICS

Applied voltages for all tests: DG139, DG142, DG143, DG144, DG145, DG146 (V^+ = 12V, V^- = -18V, V_R = 0, V_{IN2} = 2.5V) and DG161, DG162, DG163, DG164 (V^+ = 15V, V^- = -15V, V_R = 0, V_{IN2} = 2.5V). Input test condition that guarantees FET switch ON or OFF as specified is used for output specifications.

	SYMBOL (NOTE)	CHARACTERISTIC	TYPE	ABSOLUTE MAX. LIMIT -55°	25°	125°	UNITS	TEST CONDITIONS
INPUT	$V_{IN(ON)}$	Input Voltage–On	All Circuits	2.9 min	2.5 min	2.0 min	Volts	At Pin 9 and 13 See Figure 1 and 2, Pg. 4
	$V_{IN(OFF)}$	Input Voltage–Off		1.4	1.0	0.6	Volts	At Pin 9 and 13 See Figure 1 and 2, Pg. 4
	$\|V_R - V_{13}\|$	Differential Voltage		0.5 min	0.5 min	0.5 min	Volts	See Note 1, Pg. 4
	$I_{IN1(ON)}$	Input Current		120	60	60	µA	V_{IN1} 3.0V
	$I_{IN2(ON)}$			120	60	60	µA	V_{IN2} 2.0V
	$I_{IN1(OFF)}$	Input Leakage Current		0.1	0.1	2	µA	V_{IN1} 2.0V
	$I_{IN2(OFF)}$			0.1	0.1	2	µA	V_{IN2} 3.0V
SWITCH OUTPUT	$r_{DS(ON)}$	Drain-Source On Resistance	DG142 DG143	80	80	150	Ω	V_D = 10V, I_S = -10mA
			DG139 DG144	30	30	60	Ω	
			DG145 DG146	10	10	20	Ω	V_D = 10V, I_S = -10mA
			DG161 DG163	15	15	30	Ω	V_D = 7.5V, I_S = -10 mA
			DG162 DG164	50	50	100	Ω	
	$I_{D(ON)} + I_{S(ON)}$	Drain Leakage Current	DG139 DG142 DG143 DG144		2	100	nA	$V_D = V_S$ = -10V
	$I_{S(OFF)}$	Source Leakage Current			1	100	nA	V_S = 10V, V_D = -10V
	$I_{D(OFF)}$	Drain Leakage Current			1	100	nA	V_D = 10V, V_S = -10V
	$I_{D(ON)} + I_{S(ON)}$	Drain Leakage Current	DG145 DG146		2	100	nA	$V_D = V_S$ = -10V
	$I_{S(OFF)}$	Source Leakage Current			10	1000	nA	V_S = 10V, V_D = -10V
	$I_{D(OFF)}$	Drain Leakage Current			10	1000	nA	V_D = 10V, V_S = -10V
	$I_{D(ON)} + I_{S(ON)}$	Drain Leakage Current	DG161 DG163		2	500	nA	$V_D = V_S$ = -7.5V
	$I_{S(OFF)}$	Source Leakage Current			10	1000	nA	V_S = 7.5V, V_D = -7.5V
	$I_{D(OFF)}$	Drain Leakage Current			10	1000	nA	V_D = 7.5V, V_S = -7.5V
	$I_{D(ON)} + I_{S(ON)}$	Drain Leakage Current	DG162 DG164		2	500	nA	$V_D = V_S$ = -7.5V
	$I_{S(OFF)}$	Source Leakage Current			2	200	nA	V_S = 7.5V, V_D = -7.5V
	$I_{D(OFF)}$	Drain Leakage Current			2	200	nA	V_D = 7.5V, V_S = -7.5V
POWER SUPPLY	$I_{1(ON)}$	Positive Power Supply Drain Current	All Circuits		4.0		mA	V_{IN1} = 3V or V_{IN1} = 2V
	$I_{2(ON)}$	Negative Power Supply Drain Current			-2.0		mA	
	$I_{R(ON)}$	Reference Power Supply Drain Current			-2.0		mA	
	$I_{1(OFF)}$	Positive Power Supply Leakage Current			25		µA	$V_{IN1} = V_{IN2}$ = 0.8V
	$I_{2(OFF)}$	Negative Power Supply Leakage Current			-25		µA	
	$I_{R(OFF)}$	Reference Power Supply Leakage Current			-25		µA	

NOTE: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.

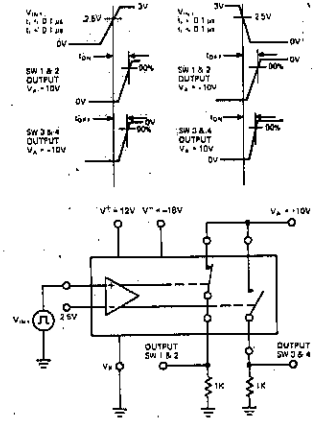
ELECTRICAL CHARACTERISTICS PER CHANNEL (cont.)

	SYMBOL (NOTE)	CHARACTERISTIC	TYPE	ABSOLUTE MAX. LIMIT –55°C	ABSOLUTE MAX. LIMIT 25°	ABSOLUTE MAX. LIMIT 125°	UNITS	TEST CONDITIONS
SWITCHING	t_{ON}	Turn-On Time	DG139, DG142 DG143, DG144 DG162, DG164		0.8		µs	See Below
			DG139, DG142 DG143, DG144 DG162, DG164		0.4	0.7	µs	
	t_{OFF}	Turn-Off Time	DG139, DG142 DG143, DG144 DG162, DG164		1.6		µs	See Below
			DG139, DG142 DG143, DG144 DG162, DG164		0.8	1.2	µs	
	t_{ON}	Turn-On Time	DG145, DG146 DG161, DG163		1.0		µs	See Below
			DG145, DG146 DG161, DG163		0.5	0.8	µs	
	t_{OFF}	Turn-Off Time	DG145, DG146 DG161, DG163		2.5		µs	See Below
			DG145, DG146 DG161, DG163		1.25	1.8	µs	
POWER	P_{ON}	ON Driver Power	All Circuits		175		mW	Both Inputs V_{IN} = 2.5V
	P_{OFF}	OFF Driver Power			1		mW	Both Inputs V_{IN} = 1.0V

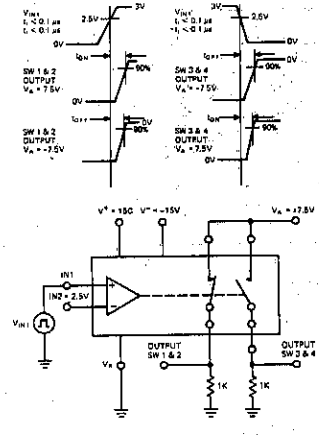
NOTE: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.

SWITCHING TIMES (25°C)

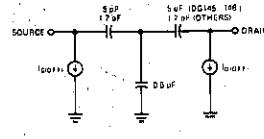
DG139, 142, 143, 144, 145, 146



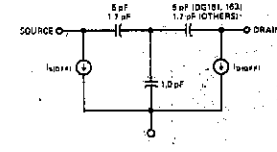
DG161, 162, 163, 164



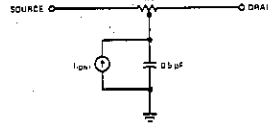
OFF MODEL



OFF MODEL



ON MODEL



ON MODEL

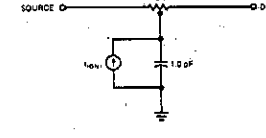


FIGURE 1

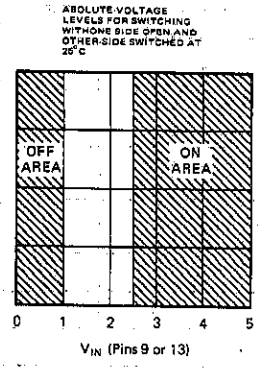
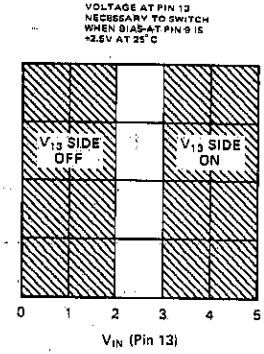


FIGURE 2



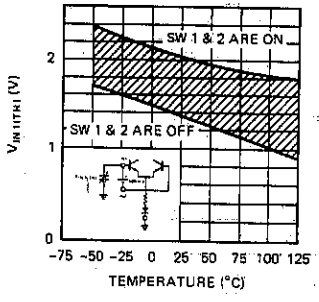
3

NOTE1: An example of Absolute Minimum Differential Voltage, $|V_9 - V_{13}|$, is when V_9 = 3V and V_{13} = 2.5V, the V_9 side of the switch is ON and the V_{13} side of the switch is OFF at 25°C. Conversely, when V_9 = 2V and V_{13} = 2.5V, the V_9 side of the switch is OFF and the V_{13} side of the switch is ON at 25°C.

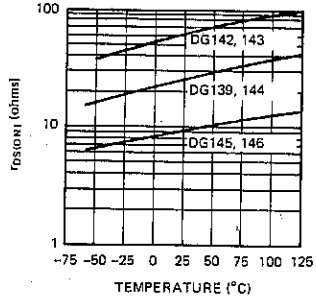
TYPICAL CHARACTERISTICS (per channel)

DG139, 142, 144, 145, 146

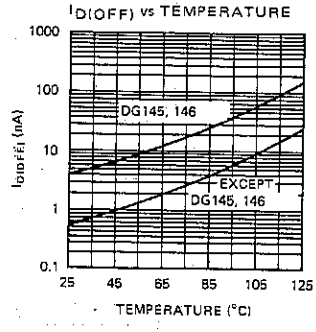
V_{IN1} THRESHOLD vs TEMPERATURE



$r_{DS(ON)}$ vs TEMPERATURE

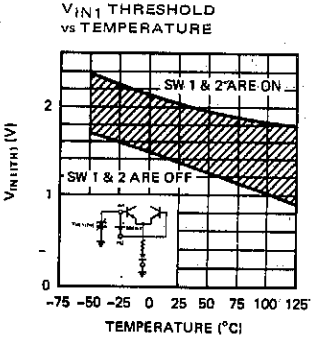


$I_{D(OFF)}$ vs TEMPERATURE

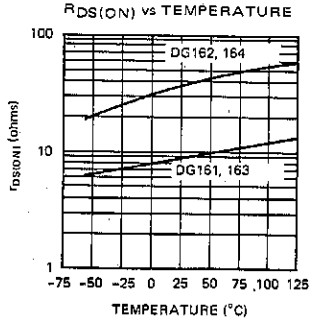


DG161, 162, 163, 164

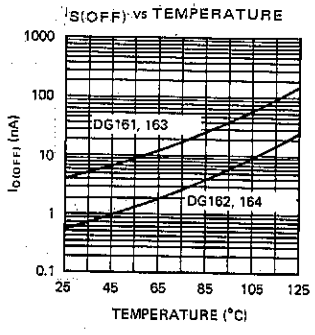
V_{IN1} THRESHOLD vs TEMPERATURE



$R_{DS(ON)}$ vs TEMPERATURE



$I_{S(OFF)}$ vs TEMPERATURE



DG180-191

High-Speed Driver With Junction FET Switches

FEATURES

- **Constant ON-resistance for signals to ±10V (DG182, 185, 188, 191), to ±7.5V (all devices)**
- **±15V power supplies**
- **<2nA leakage from signal channel in both ON and OFF states**
- **TTL, DTL, RTL direct drive compatibility**
- **t_{on}, t_{off} <150ns, break-before-make action**
- **Cross-talk and open switch isolation >50dB at 10MHz (75Ω load)**

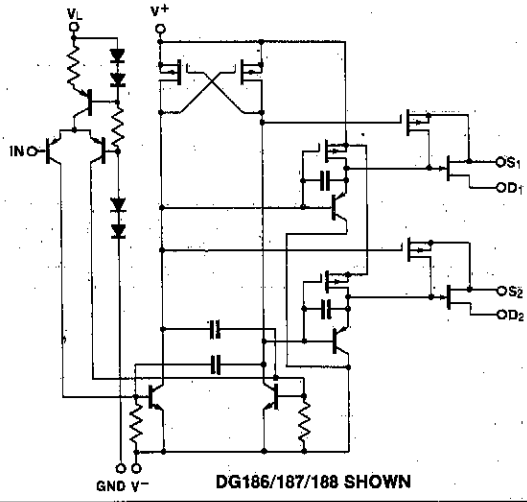
GENERAL DESCRIPTION

The DG180 thru DG191 series of analog gates consists of 2 or 4 N-channel junction-type field-effect transistors (J-FET) designed to function as electronic switches. Level-shifting drivers enable low-level inputs (0.8 to 2V) to control the ON-OFF state of each switch. The driver is designed to provide a turn-off speed which is faster than turn-on speed, so that break-before-make action is achieved when switching from one channel to another. In the ON state, each switch conducts current equally well in both directions. In the OFF condition, the switches will block voltages up to 20V peak-to-peak. Switch-OFF input-output feedthrough is >50dB down at 10MHz, because of the low output impedance of the FET-gate driving circuit.

3

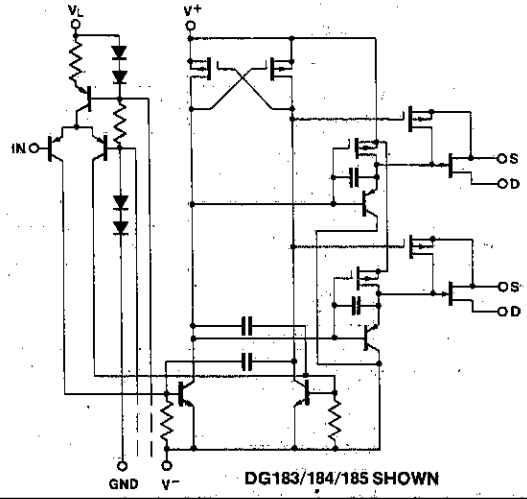
SCHEMATIC DIAGRAM (Typical Channel)

ONE AND TWO CHANNEL SPDT AND SPST CIRCUIT CONFIGURATION



DG186/187/188 SHOWN

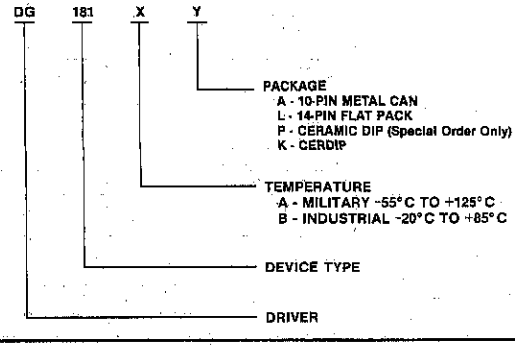
TWO CHANNEL DPST CIRCUIT CONFIGURATION



DG183/184/185 SHOWN

ORDERING INFORMATION

PART NUMBER	TYPE	$r_{DS(on)}$ (MAX)
DG180	Dual SPST	10
DG181	Dual SPST	30
DG182	Dual SPST	75
DG183	Dual DPST	10
DG184	Dual DPST	30
DG185	Dual DPST	75
DG186	SPDT	10
DG187	SPDT	30
DG188	SPDT	75
DG189	Dual SPDT	10
DG190	Dual SPDT	30
DG191	Dual SPDT	75



INTERSIL

MAXIMUM RATINGS

V+-V− 36V
V+-V_D 33V
V_D-V− 33V
V_D-V_S ..... ±22V
V_L-V− 36V
V_L-V_{IN} 8V
V_L-GND 8V
V_{IN}-GND 8V
GND-V− 27V
GND-V_{IN} 20V
Lead Temperature (Soldering, 10 sec) ..... 300°C
Current (S or D) See Note 3 ..... 200mA
Storage Temperature ..... −65°C to +150°C
Operating Temperature ..... −55°C to +125°C
Power Dissipation* ..... 450 (TW), 750 (FLAT), 825 (DIP) mW

*Device mounted with all leads welded or soldered to PC board. Derate 6mW/°C (TW); 10mW/°C (FLAT); 11mW/°C (DIP) above 75°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS ($V^+ = +15V$, $V^- = -15V$, $V_L = 5V$, Unless Noted)

			A SERIES			B SERIES				
	PARAMETER	DEVICE	−55°C	+25°C	+125°C	−20°C	+25°C	+85°C	UNITS	TEST CONDITIONS (Note 1)
SWITCH	$I_{S(off)}$	DG181, 182, 184, 185 187, 188, 190, 191 (DG180, 183, 186, 189)		1 (10)	100 (1000)		5 (15)	100 (300)	nA	V_S = 10V, V_D = −10V, V^+ = 10V V^- = −20V, V_{IN} = "OFF"
		DG181, 184, 187, 190 (DG180, 183, 186, 189)		1 (10)	100 (1000)		5 (15)	100 (300)	nA	V_S = 7.5V, V_D = −7.5V V_{IN} = "OFF"
		DG182, 185, 188, 191		1	100		5	100	nA	V_S = 10V, V_D = −10V V_{IN} = "OFF"
	$I_{D(off)}$	DG181, 182, 184, 185 187, 188, 190, 191 (DG180, 183, 186, 189)		1 (10)	100 (1000)		5 (15)	100 (300)	nA	V_S = 10V, V_D = −10V, V^+ = 10V V^- = −20V, V_{IN} = "OFF"
		DG181, 184, 187, 190 (DG180, 183, 186, 189)		1 (10)	100 (1000)		5 (15)	100 (300)	nA	V_S = 7.5V, V_D = −7.5V V_{IN} = "OFF"
		DG182, 185, 188, 191		1	100		5	100	nA	V_S = 10V, V_D = −10V V_{IN} = "OFF"
	$I_{D(on)} + I_{S(on)}$	DG180, 181, 183, 184 186, 187, 189, 190		−2	−200		−10	−200	nA	$V_D = V_S$ = −7.5V, V_{IN} = "ON"
		DG182, 185, 188, 191		−2	−200		−10	−200	nA	$V_D = V_S$ = −10V, V_{IN} = "ON"
INPUT	I_{INL}	ALL	−250	−250	−250	−250	−250	−250	µA	V_{IN} = 0V
	I_{INH}	ALL		10	20		10	20	µA	V_{IN} = 5V
DYNAMIC	t_{on}	10Ω Switches		300			350		ns	See switching time test circuit
		30Ω Switches		160			180			
		75Ω Switches		250			300			
	t_{off}	10Ω Switches		250			300			
		30Ω and 75Ω Switches		130			150			
	$C_{S(off)}$	DG181, 182, 184, 185, 187, 188, 190, 191 (DG180, 183, 186, 189)	9 typical (21 typical)						pF	V_S = −5V, I_D = 0, f = 1MHz
	$C_{D(off)}$		6 typical (17 typical)							V_D = +5V, I_S = 0, f = 1MHz
	$C_{D(on)} + C_{S(on)}$		14 typical (17 typical)							$V_D = V_S$ = 0, f = 1MHz
	OFF Isolation		Typically >50dB at 10MHz (See Note 2)							R_L = 75Ω, C_L = 3pF
SUPPLY	I^+	DG180, 181, 182, 189 190, 191		1.5			1.5		mA	V_{IN} = 5V
		DG183, 184, 185		0.1			0.1			
		DG186, 187, 188		0.8			0.8			
	I^-	DG180, 181, 182, 189, 190, 191		−5.0			−5.0			
		DG183, 184, 185		−4.0			−4.0			
		DG186, 187, 188		−3.0			−3.0			
	I_L	DG180, 181, 182, 183, 184, 185, 189, 190, 191		4.5			4.5			
		DG186, 187, 188		3.2			3.2			
	I_{GND}	ALL		−2.0			−2.0			
	I^+	DG180, 181, 182, 189, 190, 191		1.5			1.5			V_{IN} = 0V
		DG183, 184, 185		3.0			3.0			
		DG186, 187, 188		0.8			0.8			
	I^-	DG180, 181, 182, 189, 190, 191		−5.0			−5.0			
		DG183, 184, 185		−5.5			−5.5			
		DG186, 187, 188		−3.0			−3.0			
	I_L	DG180, 181, 182, 183, 184, 185, 189, 190, 191		4.5			4.5			
		DG186, 187, 188		3.2			3.2			
	I_{GND}	ALL		−2.0			−2.0			

Note 1: See Switching State Diagrams for V_{IN} "ON" and V_{IN} "OFF" Test Conditions.
Note 2: Off Isolation typically >55dB at 1MHz for DG180, 183, 186, 189.
Note 3: Saturation Drain Current for DG180, 183, 186, 189 only, typically 300mA (2msec Pulse Duration). Maximum Current on all other devices (any terminal) 30mA.

ELECTRICAL CHARACTERISTICS (CONT'D)

MAXIMUM RESISTANCES ($r_{DS(ON)}$ MAX)

DEVICE NUMBER	MILITARY TEMPERATURE			INDUSTRIAL TEMPERATURE			UNITS	CONDITIONS (Note 1) $V^+ = 15V$, $V^- = -15V$, $V_L = 5V$	
	-55°C	+25°C	+125°C	-20°C	+25°C	+85°C			
DG180	10	10	20	15	15	25	Ω	$V_D = -7.5V$	
DG181	30	30	60	50	50	75	Ω	$V_D = -7.5V$	
DG182	75	75	100	100	100	150	Ω	$V_D = -10V$	
DG183	10	10	20	15	15	25	Ω	$V_D = -7.5V$	
DG184	30	30	60	50	50	75	Ω	$V_D = -7.5V$	
DG185	75	75	150	100	100	150	Ω	$V_D = -10V$	$I_S = -10mA$
DG186	10	10	20	15	15	25	Ω	$V_D = -7.5V$	
DG187	30	30	60	50	50	75	Ω	$V_D = -7.5V$	V_{IN} = "ON"
DG188	75	75	150	100	100	150	Ω	$V_D = -10V$	
DG189	10	10	20	15	15	25	Ω	$V_D = -7.5V$	
DG190	30	30	60	50	50	50	Ω	$V_D = -7.5V$	
DG191	75	75	150	100	100	150	Ω	$V_D = -10V$	

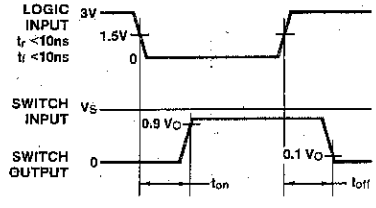
APPLICATION HINT (for design only): Normally the minimum signal handling capability of the DG180 through DG191 family is 20V peak-to-peak for the 75Ω switches and 15V peak-to-peak for the 10Ω and 30Ω switches (refer I_D and I_S tests above). For other Analog Signals, the following guidelines can be used: proper switch turn-off requires that $V^- \leq V_{ANALOG}(peak) - V_p$ where $V_p = 7.5V$ for the 10Ω and 30Ω switches and $V_p = 5.0V$ for 75Ω switches e.g., -10V minimum (-peak) analog signal and a 75Ω switch ($V_p = 5V$), requires that $V^- \leq -10V - 5V = -15V$.

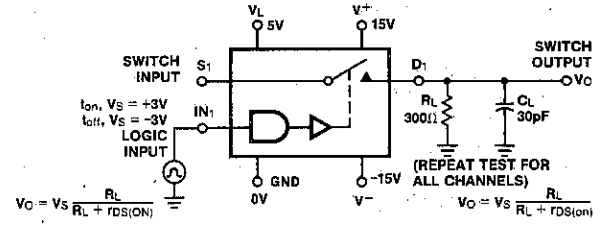
3

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or - as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

LOGIC INPUT FOR "OFF" TO "ON" CONDITION (DG180/181/182 SHOWN)





DUAL SPST
DG180/181/182

TEST CONDITIONS	
DG180/181/182	
V_{IN} "ON" = 0.8V	All Channels
V_{IN} "OFF" = 2.0V	All Channels

SWITCH STATES ARE FOR LOGIC "1" INPUT = 2.0V

DUAL DPST
DG183/184/185

TEST CONDITIONS	
DG183/184/185	
V_{IN} "ON" = 2.0V	All Channels
V_{IN} "OFF" = 0.8V	All Channels

SWITCH STATES ARE FOR LOGIC "1" INPUT = 2.0V

SPDT
DG186/187/188

TEST CONDITIONS	
DG186/187/188	
V_{IN} "ON" = 2.0V	Channel 1
V_{IN} "ON" = 0.8V	Channel 2
V_{IN} "OFF" = 2.0V	Channel 2
V_{IN} "OFF" = 0.8V	Channel 1

SWITCH STATES ARE FOR LOGIC "1" INPUT = 2.0V

DUAL SPDT
DG189/190/191

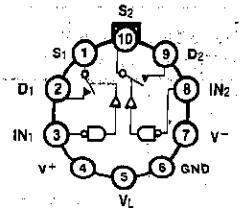
TEST CONDITIONS	
DG189/190/191	
V_{IN} "ON" = 2.0V	Channels 1 & 2
V_{IN} "ON" = 0.8V	Channels 3 & 4
V_{IN} "OFF" = 2.0V	Channels 3 & 4
V_{IN} "OFF" = 0.8V	Channels 1 & 2

SWITCH STATES ARE FOR LOGIC "1" INPUT = 2.0V

PIN CONFIGURATIONS AND SWITCHING STATE DIAGRAM (See previous page for logic input)

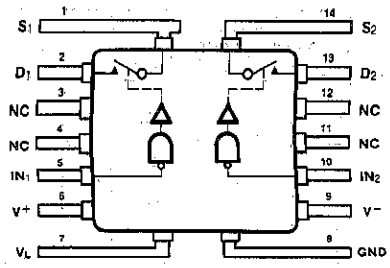
DUAL SPST (DG180, 181, 182)

Metal Can Package



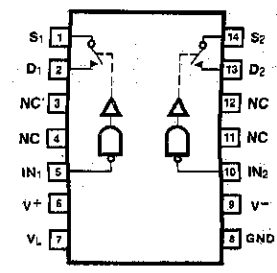
(OUTLINE DWG TO-100)

Flat Package



(OUTLINE DWG FD-2)

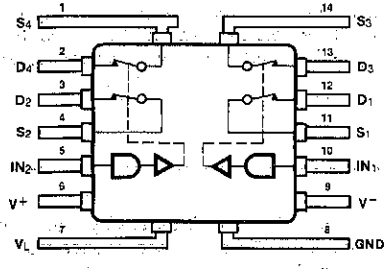
CERDIP*



(OUTLINE DWG JD)

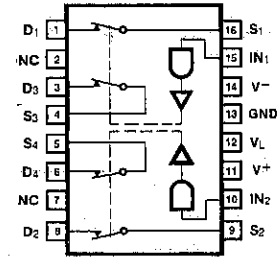
DUAL DPST (DG183, 184, 185)

Flat Package



(OUTLINE DWG FD-2)

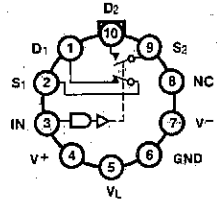
CERDIP*



(OUTLINE DWG JE)

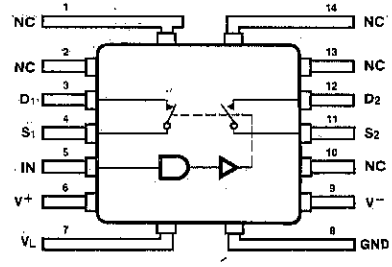
SPDT (DG186, 187, 188)

Metal Can Package



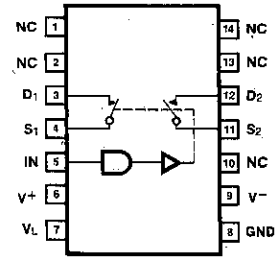
(OUTLINE DWG TO-100)

Flat Package



(OUTLINE DWG FD-2)

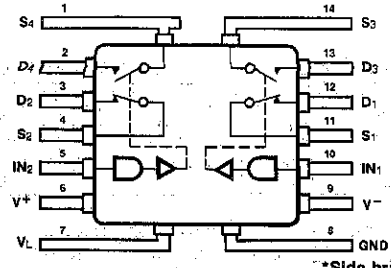
CERDIP*



(OUTLINE DWG JD)

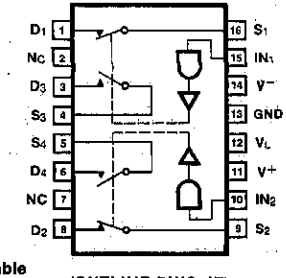
DUAL SPDT (DG189, 190, 191)

Flat Package



(OUTLINE DWG FD-2)

CERDIP*



(OUTLINE DWG JE)

*Side braize ceramic package available as special order only. Consult factory.

DGM181-191
High-Speed CMOS Analog Switches

FEATURES
- **Pin and Function Replacement for DG181 Family**
- **Meets or exceeds all DG181 family specifications with monolithic reliability**
- **Low power consumption**
- **1nA leakage from signal channel in both ON and OFF states**
- **TTL, DTL, RTL direct drive capability**
- **t_{on}, t_{off} <150ns, break-before-make action**
- **Crosstalk and open load switch isolation >50dB at 10MHz (75Ω load)**

GENERAL DESCRIPTION
The DGM181 family of CMOS monolithic switches utilizes Intersil's latch-free junction isolated processing to combine the speed of the hybrid DG181 family with the reliability and low power consumption of a monolithic CMOS construction. These devices, therefore, are an ideal replacement for the DG181 family.

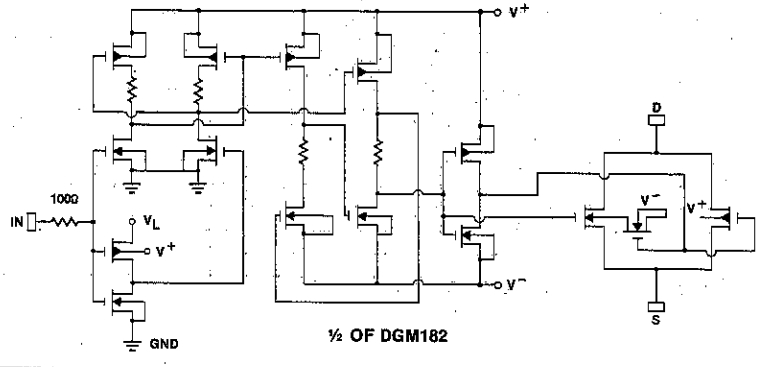
The DGM181 family has a high state threshold of 2.4V; devices which have a threshold of 2.0V (the DG181 specification) can be selected and are available as the DGMS series — see ordering information.

Both series meet or exceed all other specifications of the DG181 family.

No quiescent power is dissipated in either the ON or OFF state of the switch. Maximum power supply current is 10μA from any supply, and typical quiescent currents are in the 10nA range. OFF leakages are guaranteed to be less than 200pA at 25°C.

3

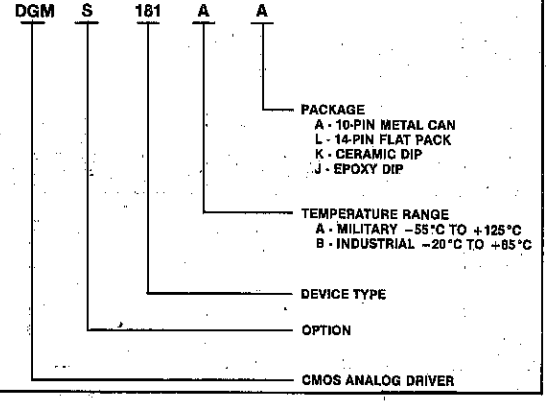
SCHEMATIC DIAGRAM (Typical Channel)



½ OF DGM182

ORDERING INFORMATION

TYPE	STANDARD PART NUMBER	SELECTED PART NUMBER	$r_{DS(on)}$ MAX AT 25°C
Dual SPST	DGM181BX	DGMS181BX	50
	DGM182AX	DGMS182AX	50
	DGM182BX	DGMS182BX	75
Dual DPST	DGM184BX	DGMS184BX	50
	DGM185AX	DGMS185AX	50
	DGM185BX	DGMS185BX	75
SPDT	DGM187BX	DGMS187BX	50
	DGM188AX	DGMS188AX	50
	DGM188BX	DGMS188BX	75
Dual SPDT	DGM190BX	DGMS190BX	50
	DGM191AX	DGMS191AX	50
	DGM191BX	DGMS191BX	75



MAXIMUM RATINGS

$V^+ - V^-$ 36V
$V^+ - V_D$ 33V
$V_D - V^-$ 33V
$V_D - V_S$ ..... ±22V
$V_L - V^-$ 36V
Current (Any Terminal) 30mA
$V_L - V_{IN}$ 30V
$V_L - V_{GND}$ 20V
$V_{IN} - V_{GND}$ 20V
GND − V^- 27V
GND − V_{IN} 20V

Storage Temperature ..... −65°C to +150°C
Operating Temperature ..... −55°C to +125°C
Power Dissipation* ..... 450 (TW), 750 (FLAT), 825 (DIP) mW

*Device mounted with all leads welded or soldered to PC board. Derate 6mW/°C (TW); 10mW/°C (FLAT); 11mW/°C (DIP) above 75°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3

ELECTRICAL CHARACTERISTICS ($V^+ = +15V$, $V^- = -15V$, $V_L = 5V$, unless noted)

	PARAMETER	DEVICE	A SERIES −55°C	A SERIES +25°C	A SERIES +125°C	B SERIES −20°C	B SERIES +25°C	B SERIES +85°C	UNITS	TEST CONDITIONS (Note 1)
SWITCH	$I_{S(off)}$	DGM181, 184, 187, 190					2.0	100	nA	$V_S = 7.5V$, $V_D = -7.5V$ V_{IN} = "OFF"
		DGM182, 185, 188, 191		0.2	50		0.5	50	nA	$V_S = 10V$, $V_D = -10V$ V_{IN} = "OFF"
	$I_{D(off)}$	DGM181, 184, 187, 190					2.0	100	nA	$V_S = 7.5V$, $V_D = -7.5V$ V_{IN} = "OFF"
		DGM182, 185, 188, 191		0.2	50		0.5	50	nA	$V_S = 10V$, $V_D = -10V$ V_{IN} = "OFF"
	$I_{D(on)} + I_{S(on)}$	DGM181, 184, 187, 190					5.0	100	nA	$V_D = V_S = -7.5V$, V_{IN} = "ON"
		DGM182, 185, 188, 191		0.5	50		2.0	50	nA	$V_D = V_S = -10V$, V_{IN} = "ON"
IN	I_{INL}	ALL		1.0	20		10	20	µA	$V_{IN} = 0V$
	I_{INH}	ALL		1.0	20		10	20	µA	$V_{IN} = 5V$
DYNAMIC	t_{on}	DGM181, 184, 187, 190					180		ns	See switching time test circuit
		DGM182, 185, 188, 191		250			300			
	t_{off}	ALL		130			150			
	$C_{S(off)}$	DGM181, 182, 184, 185, 187, 188, 190, 191	5pF typical						pF	$V_S = -5V$, $I_D = 0$, f = 1MHz
	$C_{D(off)}$		6pF typical							$V_D = +5V$, $I_S = 0$, f = 1MHz
	$C_{D(on)} + C_{S(on)}$		11pF typical							$V_D = V_S = 0$, f = 1MHz
	OFF Isolation		Typically >50dB at 10MHz							$R_L = 75\Omega$, $C_L = 3pF$
SUPPLY	I^+	ALL		10	100		100		µA	$V_{IN} = 5V$
	I^-	ALL		10	100		100			
	I_L	ALL		10	100		100			
	I_{GND}	ALL		10	100		100			
	I^+	ALL		10	100		100			$V_{IN} = 0V$
	I^-	ALL		10	100		100			
	I_L	ALL		10	100		100			
	I_{GND}	ALL		10	100		100			

NOTE 1: See Switching State Diagrams for V_{IN} "ON" and V_{IN} "OFF" Test Conditions.

ELECTRICAL CHARACTERISTICS

MAXIMUM RESISTANCES ($r_{DS(ON)}$ MAX)

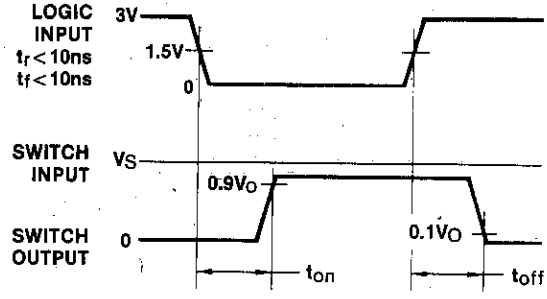
DEVICE NUMBER	MILITARY TEMPERATURE −55°C	MILITARY TEMPERATURE +25°C	MILITARY TEMPERATURE +125°C	INDUSTRIAL TEMPERATURE −20°C	INDUSTRIAL TEMPERATURE +25°C	INDUSTRIAL TEMPERATURE +85°C	UNITS	CONDITIONS (Note 1) $V^+ = 15V$, $V^- = -15V$, $V_L = 5V$	
DGM181				50	50	75	Ω	$V_D = -7.5V$	
DGM182	50	50	75	75	75	100	Ω	$V_D = -10V$	
DGM184				50	50	75	Ω	$V_D = -7.5V$	
DGM185	50	50	75	75	75	100	Ω	$V_D = -10V$	$I_S = -10mA$
DGM187				50	50	75	Ω	$V_D = -7.5V$	V_{IN} = "ON"
DGM188	50	50	75	75	75	100	Ω	$V_D = -10V$	
DGM190				50	50	75	Ω	$V_D = -7.5V$	
DGM191	50	50	75	75	75	100	Ω	$V_D = -10V$	

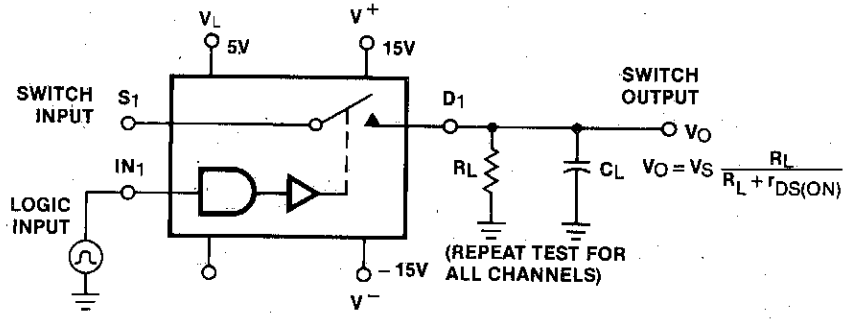
APPLICATION COMMENT: The charge injection in these switches is of opposite polarity to that of the standard DG180 family, but considerably smaller.

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or – as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

LOGIC INPUT FOR "OFF" TO "ON" CONDITION (DG180/181/182 SHOWN)





SWITCH STATES

DUAL SPST
DGM181/182

TEST CONDITIONS	
DGM181/182	
V_{IN} "ON" = 0.8V	All Channels
V_{IN} "OFF" = 2.4V+	All Channels

DUAL DPST
DGM184/185

TEST CONDITIONS	
DGM184/185	
V_{IN} "ON" = 2.4V+	All Channels
V_{IN} "OFF" = 0.8V	All Channels

SPDT
DGM187/188

TEST CONDITIONS	
DGM187/188	
V_{IN} "ON" = 2.4V+	Channel 1
V_{IN} "ON" = 0.8V	Channel 2
V_{IN} "OFF" = 2.4V+	Channel 2
V_{IN} "OFF" = 0.8V	Channel 1

DUAL SPDT
DGM190/191

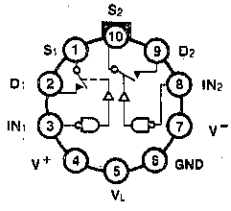
TEST CONDITIONS	
DGM190/191	
V_{IN} "ON" = 2.4V+	Channels 1 & 2
V_{IN} "ON" = 0.8V	Channels 3 & 4
V_{IN} "OFF" = 2.4V+	Channels 3 & 4
V_{IN} "OFF" = 0.8V	Channels 1 & 2

† FOR SELECTED DEVICES, LOGIC "1" INPUT = 2.0V

PIN CONFIGURATIONS & SWITCHING STATE DIAGRAM

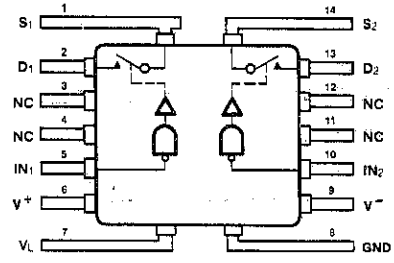
DUAL SPST (DGM181, 182)

Metal Can Package



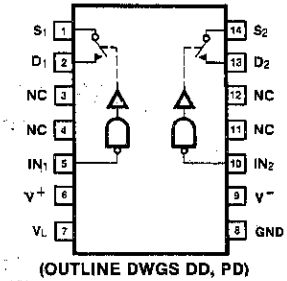
(OUTLINE DWG TO-100)

Flat Package (FD-2)



SWITCH STATES ARE FOR LOGIC "1" INPUT

Dual-In-Line Package

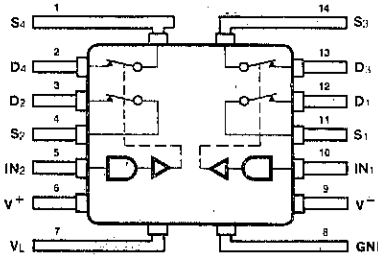


(OUTLINE DWGS DD, PD)

3

DUAL DPST (DGM184, 185)

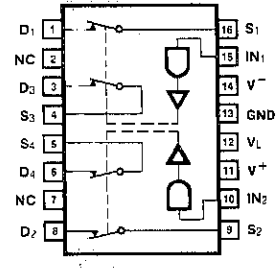
Flat Package



(OUTLINE DWG FD-2)

SWITCH STATES ARE FOR LOGIC "1" INPUT

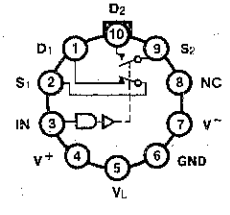
Dual-In-Line Package



(OUTLINE DWGS DE, PE)

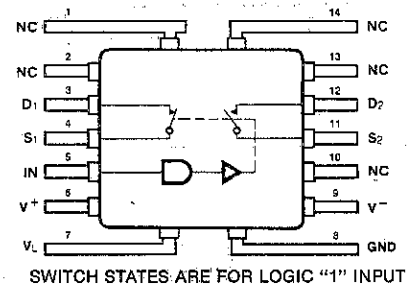
SPDT (DGM187, 188)

Metal Can Package



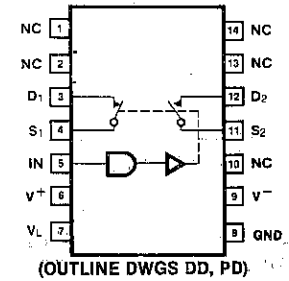
(OUTLINE DWG TO-100)

Flat Package (FD-2)



SWITCH STATES ARE FOR LOGIC "1" INPUT

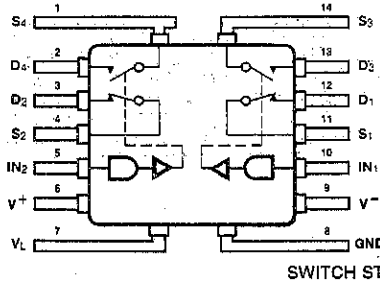
Dual-In-Line Package



(OUTLINE DWGS DD, PD)

DUAL SPDT (DGM190, 191)

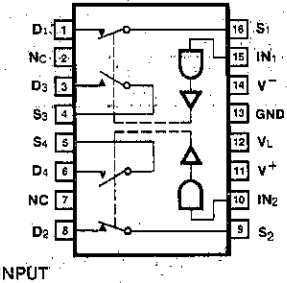
Flat Package



(OUTLINE DWG FD-2)

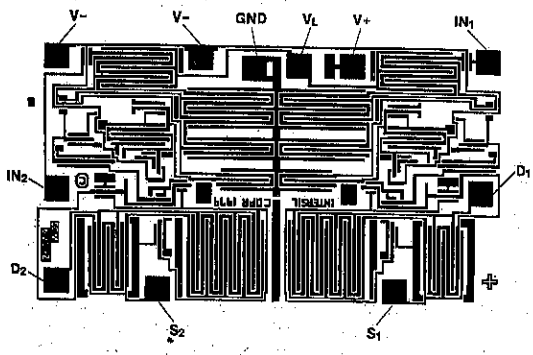
SWITCH STATES ARE FOR LOGIC "1" INPUT

Dual-In-Line Package



(OUTLINE DWGS DE, PE)

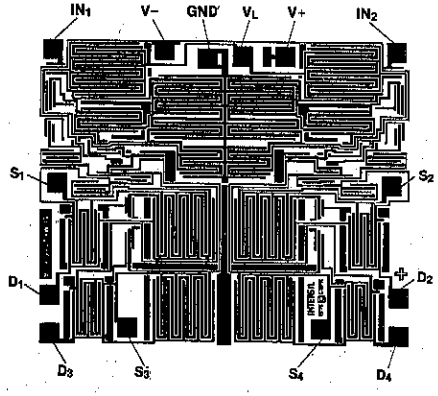
CHIP TOPOGRAPHIES



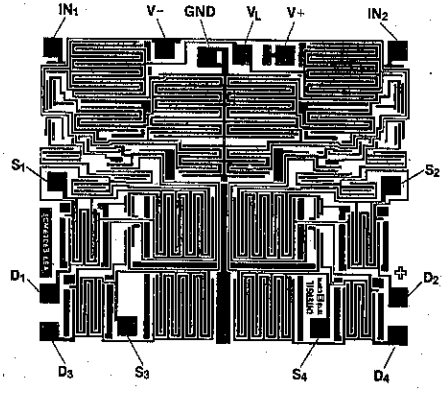
DGM181/182
91x53

CONSULT FACTORY

DGM188



DGM185
91x76



DGM191
91x76

NOTE: BACKSIDE OF CHIP IS COMMON TO V+.

DG200/IH5200
CMOS Dual SPST Analog Switches

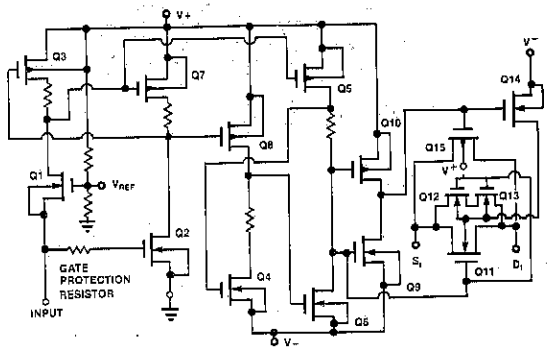
FEATURES
- Switches Greater Than 28Vpp Signals With ± 15V Supplies
- Break-Before-Make Switching t_{off} 250 nsec, t_{on} 700nsec Typical
- T^2L, DTL, CMOS, PMOS Compatible
- Non-Latching With Supply Turn-Off
- Complete Monolithic Construction
- Industry Standard (DG200)
- Improved Performance Version (IH5200)

3

GENERAL DESCRIPTION
The DG200/IH5200 solid state analog gates are designed using an improved, high voltage CMOS monolithic technology. They provide ease-of-use and performance advantages not previously available from solid state switches. Destructive latch-up of solid state analog gates has been eliminated by INTERSIL's CMOS technology.

The DG200 is completely spec and pin-out compatible with the industry standard device, while the IH5200 offers significantly enhanced specifications with respect to ON and OFF leakage currents, switching times, and supply current.

SCHEMATIC DIAGRAM (½ DG200/IH5200)

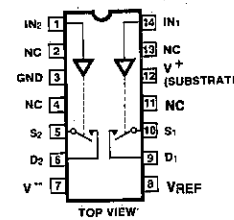


ORDERING INFORMATION

INDUSTRY STANDARD PART	IMPROVED SPEC DEVICE	PACKAGE	TEMPERATURE RANGE
DG200AA	IH5200MTW	10-Pin Metal Can	−55 to +125°C
DG200AK	IH5200MJD	14-Pin CERDIP	−55 to +125°C
DG200AL	IH5200MFD	14-Pin Flat Pak	−55 to +125°C
DG200BA	IH5200ITW	10-Pin Metal Can	−25 to +85°C
DG200BK	IH5200IJD	14-Pin CERDIP	−25 to +85°C
DG200BL	IH5200IFD	14-Pin Flat Pak	−25 to +85°C
DG200CJ	IH5200CPD	14-Pin Epoxy DIP	0 to +70°C

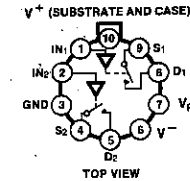
PIN CONFIGURATIONS

CERDIP & EPOXY DUAL-IN-LINE PACKAGE
(outline dwgs JD, PD)



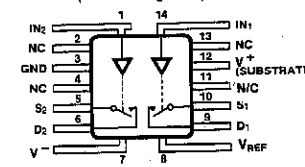
TOP VIEW

METAL CAN PACKAGE
(outline dwg TO-100)



TOP VIEW

FLAT PACKAGE
(outline dwg FD-2)



TOP VIEW

SWITCH STATES ARE FOR LOGIC "1" INPUT (POSITIVE LOGIC)

ABSOLUTE MAXIMUM RATINGS

$V^+ - V^-$ ..... <33V
$V^+ - V_D$ ..... <30V
$V_D - V^-$ ..... <30V
$V_D - V_S$ ..... < ±22V
V_{IN}-GND ..... <20V

Current (Any Terminal) ..... >30mA
Storage Temperature ..... −65°C to +150°C
Operating Temperature ..... −55°C to +125°C
Power Dissipation 450mW
(All Leads Soldered to a P.C. Board.) Derate 6mW/°C Above 75°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3

DG200

ELECTRICAL CHARACTERISTICS (@25°C, $V^+ = +15V$, $V^- = -15V$)

PER CHANNEL		MIN./MAX. LIMITS							
		MILITARY			COMMERCIAL/INDUSTRIAL				TEST
SYMBOL	CHARACTERISTIC	−55°C	+25°C	+125°C	0/−25°C	+25°C	+70°C/+85°C	UNITS	CONDITIONS
$I_{IN(ON)}$	Input Logic Current	1	1	1	1	1	1	μA	$V_{IN} = 0.8V$
$I_{IN(OFF)}$	Input Logic Current	1	1	1	1	1	1	μA	$V_{IN} = 2.4V$
$r_{DS(on)}$	Drain-Source On Resistance	70	70	100	80	80	100	Ω	$I_S = 10mA$ $V_{ANALOG} = \pm 10V$
$r_{DS(on)}$	Channel-to-Channel $r_{DS(on)}$ Match		25 (typ)			30 (typ)		Ω	
V_{ANALOG}	Min. Analog Signal Handling Capability		±15			±15		V	
$I_{D(OFF)}$	Switch OFF Leakage Current	2	2	100	5	5	100	nA	$V_{ANALOG} = -14V$ to +14V
$I_{S(OFF)}$	Switch OFF Leakage Current	2	2	100	5	5	100	nA	$V_{ANALOG} = -14V$ to +14V
$I_{D(ON)} + I_{S(ON)}$	Switch ON Leakage Current	2	2	200	10	10	200	nA	$V_D = V_S = -14V$ to +14V
t_{on}	Switch "ON" Time		1.0			1.0		μs	$R_L = 1k\Omega$, V_{ANALOG} = −10V to +10V See Fig. A
t_{off}	Switch "OFF" Time		0.5			0.5		μs	$R_L = 1k\Omega$, V_{ANALOG} = −10V to +10V See Fig. A
$Q_{(INJ.)}$	Charge Injection		15			20		mV	See Fig. B
OIRR	Min. Off Isolation Rejection Ratio		54			50		dB	f=1MHz, $R_L = 100\Omega$, $C_L \leq 5pF$ See Fig. C, (Note 1)
I_{V1}	+Power Supply Quiescent Current	1000	1000	2000	1000	1000	2000	μA	$V_{IN} = 0V$ or $V_{IN} = 5V$
I_{V2}	−Power Supply Quiescent Current	1000	1000	2000	1000	1000	2000	μA	
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio		54			50		dB	One Channel Off (Note 1)

Note 1: These parameters are not tested in production.

TEST CIRCUITS

Figure A

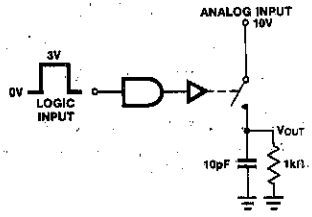


Figure B

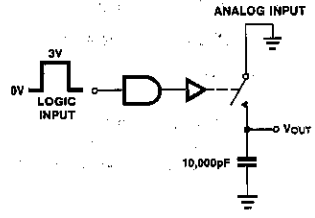
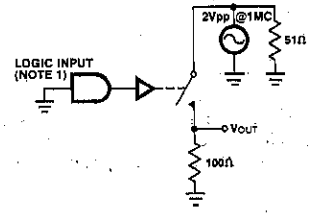


Figure C



3

IH5200

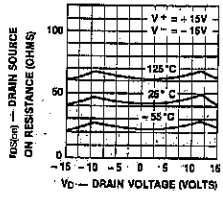
ELECTRICAL CHARACTERISTICS (@25°C, $V^+ = +15V$, $V^- = -15V$, V_{REF} open)

PER CHANNEL		MIN./MAX. LIMITS							
		MILITARY			COMMERCIAL/INDUSTRIAL				TEST
SYMBOL	CHARACTERISTIC	−55°C	+25°C	+125°C	0/−25°C	+25°C	+70°C/+85°C	UNITS	CONDITIONS
$I_{IN(ON)}$	Input Logic Current	1	1	1	1	1	1	µA	$V_{IN} = 0.8V$
$I_{IN(OFF)}$	Input Logic Current	1	1	1	1	1	1	µA	$V_{IN} = 2.4V$
$r_{DS(on)}$	Drain-Source On Resistance	70	70	100	80	80	100	Ω	$I_S = 10mA$ $V_{ANALOG} = \pm 10V$
$r_{DS(on)}$	Channel-to-Channel $r_{DS(on)}$ Match		25 (typ)			30 (typ)		Ω	
V_{ANALOG}	Min. Analog Signal Handling Capability		±15			±15		V	
$I_{D(OFF)}$	Switch OFF Leakage Current	0.2	0.2	50	1	1	50	nA	$V_{ANALOG} = -14V$ to +14V
$I_{S(OFF)}$	Switch OFF Leakage Current	0.2	0.2	50	1	1	50	nA	$V_{ANALOG} = -14V$ to +14V
$I_{D(ON)} + I_{S(ON)}$	Switch ON Leakage Current	0.5	0.5	100	1	1	100	nA	$V_D = V_S = -14V$ to +14V
t_{on}	Switch "ON" Time		0.7			0.8		µs	$R_L = 1k\Omega$, V_{ANALOG} = −10V to +10V See Fig. A
t_{off}	Switch "OFF" Time		0.25			0.4		µs	$R_L = 1k\Omega$, V_{ANALOG} = −10V to +10V See Fig. A
$Q_{(INJ.)}$	Charge Injection		5			10		mV	See Fig. B
OIRR	Min. Off Isolation Rejection Ratio		54			50		dB	f=1MHz, $R_L = 100\Omega$, $C_L \leq 5pF$ See Fig. C, (Note 1)
I_{V1}	+Power Supply Quiescent Current	250	200	150	300	250	200	µA	$V_{IN} = 0V$ or $V_{IN} = 5V$
I_{V2}	−Power Supply Quiescent Current	10	10	100	10	10	100	µA	
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio		54			50		dB	One Channel Off (Note 1)

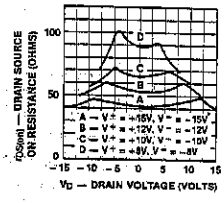
Note 1: These parameters are not tested in production.

TYPICAL CHARACTERISTICS

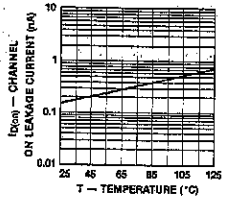
$r_{DS(on)}$ vs V_D and Temperature



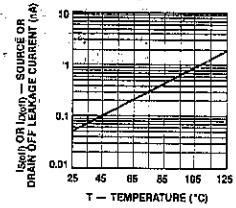
$r_{DS(on)}$ vs V_D and Power Supply Voltage



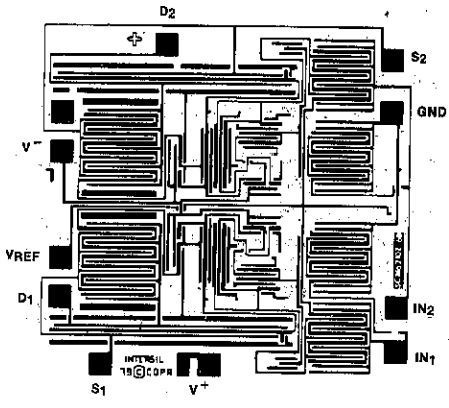
$I_{D(on)}$ vs Temperature*



$I_{S(off)}$ or $I_{D(off)}$ vs Temperature*



CHIP TOPOGRAPHY



NOTE: Backside of chip of common to V+.

3

APPLICATIONS

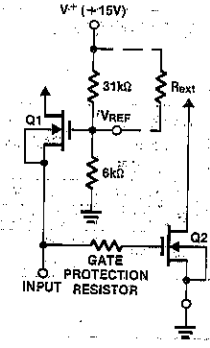
Using the V_{REF} Terminal

The DG200 has an internal voltage divider setting the TTL threshold on the input control lines for +15V on V^+. The schematic is shown here, with nominal resistor values, giving approximately 2.4V on the V_{REF} pin. As the TTL input signal goes from +0.8V to +2.4V, Q1 and Q2 switch states to turn the switch ON and OFF.

If the power supply voltage is less than +15V, then a resistor needs to be added between V^+ and the V_{REF} pin, to restore +2.4V at V_{REF}. The table shows the value of this resistor for various supply voltages, to maintain TTL compatibility. If CMOS logic levels on a +5V supply are being used, the threshold shifts are less critical, but a separate column of suitable values is given in the table. For logic swings of −5V to +5V, no resistor is needed.

In general, the "low" logic level should be <0.8V to prevent Q1 and Q2 from both being ON together (this will cause incorrect switch function). With open collector logic, and a low value of pull-up resistor, the logic "low" level can be above 0.8V. In this case, INTERSIL can supply parts with thresholds >1.5V, allowing the user to define the "low" as <1.5V (consult factory). The V_{REF} point should be set at least 2.6V above this "low" state, or to >4.1V. An external resistor of 27kΩ between V^+ and V_{REF} is required, for a +15V supply.

V^+ Supply (V)	TTL Resistor (kΩ)	CMOS Resistor (kΩ)
+15	—	—
+12	100	—
+10	51	—
+9	(34)	34
+8	(27)	27
+7	18	18



DG201/IH5201
Quad SPST CMOS Analog Switches

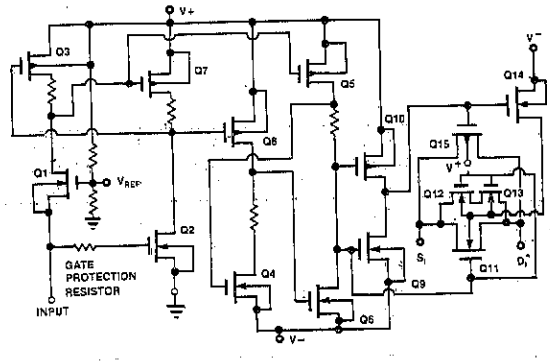
FEATURES
- Switches Greater Than 28V_{p-p} Signals With ±15V Supplies
- Break-Before-Make Switching t_{off} = 250nsec, t_{on} = Typically 500nsec
- TTL, DTL, CMOS, PMOS Compatible
- Non-Latching With Supply Turn-Off
- Complete Monolithic Construction
- Industry Standard (DG201)
- Improved Performance Version IH5201

3

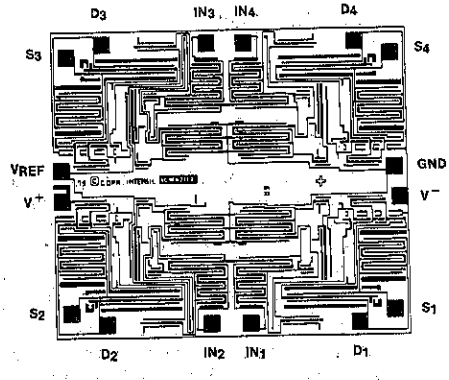
GENERAL DESCRIPTION
The DG201/IH5201 solid-state analog gates are designed using an improved, high-voltage CMOS monolithic technology. They provide ease-of-use and performance advantages not previously available from solid-state switches. Destructive latch-up of solid-state analog gates has been eliminated by INTERSIL's CMOS technology.

The DG201 is completely spec and pin-out compatible with the industry standard device, while the IH5201 offers significantly enhanced specifications with respect to ON and OFF leakage currents, switching times, and supply current.

SCHEMATIC DIAGRAM (¼ DG201/IH5201)



CHIP TOPOGRAPHY



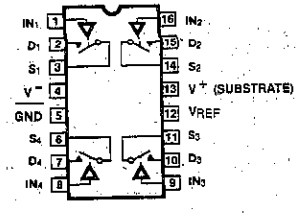
NOTE: Backside of chip common to V+.

ORDERING INFORMATION

INDUSTRY STANDARD PART	IMPROVED SPEC DEVICE	PACKAGE	TEMPERATURE RANGE
DG201AK	IH5201MJE	16-Pin CERDIP	−55°C to +125°C
DG201BK	IH5201IJE	16-Pin CERDIP	−20°C to +85°C
DG201CJ	IH5201CPE	16-Pin Plastic DIP	0°C to +70°C

PIN CONFIGURATION (outline dwgs JE, PE)

DUAL-IN-LINE PACKAGE



SWITCH OPEN FOR LOGIC "1" INPUT

ABSOLUTE MAXIMUM RATINGS

$V^+ - V^-$ ..... <33V
$V^+ - V_D$ ..... <30V
$V_D - V^-$ ..... <30V
$V_D - V_S$ ..... < ±22V
$V_{REF} - V^-$ ..... <33V
$V_{REF} - V_{IN}$ ..... <30V
V_{REF}-GND ..... <20V
V_{IN}-GND ..... <20V

Current (Any Terminal) ..... <30mA
Storage Temperature ..... −65°C to +150°C
Operating Temperature ..... −55°C to +125°C
Power Dissipation 450mW
Derate 6mW/°C Above 70°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3

DG201

ELECTRICAL CHARACTERISTICS (@25°C, $V^+ = +15V$, $V^- = -15V$)

PER CHANNEL		MIN./MAX. LIMITS							
		MILITARY			COMMERCIAL				TEST
SYMBOL	CHARACTERISTIC	−55°C	+25°C	+125°C	0°C	+25°C	+70°C	UNITS	CONDITIONS
$I_{IN(ON)}$	Input Logic Current	1	1	1	1	1	1	μA	$V_{IN} = 0.8V$
$I_{IN(OFF)}$	Input Logic Current	1	1	1	1	1	1	μA	$V_{IN} = 2.4V$
$r_{DS(ON)}$	Drain-Source On Resistance	80	80	125	100	100	125	Ω	$I_S = 10mA$ $V_{ANALOG} = \pm 10V$
$r_{DS(ON)}$	Channel to Channel $r_{DS(ON)}$ Match		25 (typ)			30 (typ)		Ω	
V_{ANALOG}	Analog Signal Handling Capability		±15			±15		V	
$I_{D(OFF)}$	Switch OFF Leakage Current	1	1	100	5	5	100	nA	$V_{ANALOG} = -14V$ to +14V
$I_{S(OFF)}$	Switch OFF Leakage Current	1	1	100	5	5	100	nA	$V_{ANALOG} = -14V$ to +14V
$I_{D(ON)} + I_{S(ON)}$	Switch On Leakage Current	2	2	200	5	5	200	nA	$V_D = V_S = \pm 14V$
t_{on}	Switch "ON" Time		1.0			1.0		μs	$R_L = 1k\Omega$, V_{ANALOG} = −10V to +10V See Fig. A
t_{off}	Switch "OFF" Time		0.5			0.5		μs	$R_L = 1k\Omega$, V_{ANALOG} = −10V to +10V See Fig. A
$Q_{(INJ.)}$	Charge Injection		15			20		mV	See Fig. B
OIRR	Min. Off Isolation Rejection Ratio		54			50		dB	f=1MHz, $R_L = 100\Omega$, $C_L \leq 5pF$ See Fig. C, (Note 1)
I_Q^+	+ Power Supply Quiescent Current	2000	1000	2000	2000	1000	2000	μA	$V_{IN} = 0V$ or 5V
I_Q^-	− Power Supply Quiescent Current	2000	1000	2000	2000	1000	2000	μA	
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio		54			50		dB	One Channel Off (Note 1)

Note 1: These parameters not tested in production.

TEST CIRCUITS

Figure A

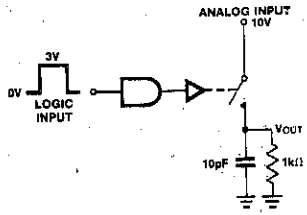


Figure B

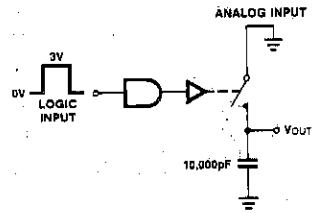
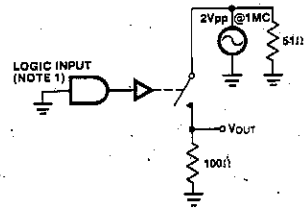


Figure C



3

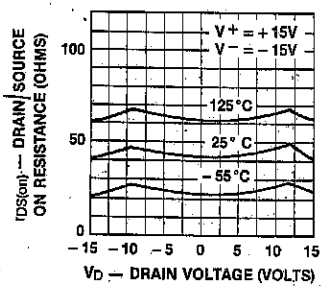
IH5201

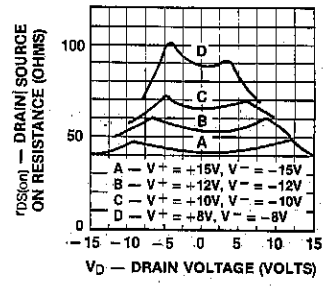
ELECTRICAL CHARACTERISTICS (@25°C, $V^+ = +15V$, $V^- = -15V$)

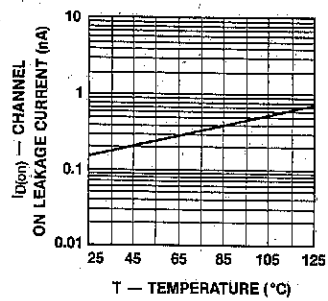
PER CHANNEL		MIN./MAX. LIMITS						UNITS	TEST CONDITIONS
		MILITARY			COMMERCIAL				
SYMBOL	CHARACTERISTIC	−55°C	+25°C	+125°C	0°C	+25°C	+70°C		
$I_{IN(ON)}$	Input Logic Current	1	1	1	1	1	1	μA	$V_{IN} = 0.8V$
$I_{IN(OFF)}$	Input Logic Current	1	1	1	1	1	1	μA	$V_{IN} = 2.4V$
$r_{DS(ON)}$	Drain-Source On Resistance	75	75	100	100	100	125	Ω	$I_S = 10mA$ $V_{ANALOG} = \pm 10V$
$r_{DS(ON)}$	Channel to Channel $r_{DS(ON)}$ Match		25 (typ)			30 (typ)		Ω	
V_{ANALOG}	Analog Signal Handling Capability		±15			±15		V	
$I_{D(OFF)}$/ $I_{S(OFF)}$	Switch OFF Leakage Current	0.2	0.2	50	1	1	50	nA	$V_{ANALOG} = -14V$ to $+14V$
$I_{D(ON)}$ + $I_{S(ON)}$	Switch ON Leakage Current	0.5	0.5	100	1	1	100	nA	$V_D = V_S = \pm 14V$
t_{on}	Switch "ON" Time		0.5			0.75		μs	$R_L = 1k\Omega$, V_{ANALOG} $= -10V$ to $+10V$ See Fig. A
t_{off}	Switch "OFF" Time		0.25			0.3		μs	$R_L = 1k\Omega$, V_{ANALOG} $= -10V$ to $+10V$ See Fig. A
$Q_{(INJ.)}$	Charge Injection		5			10		mV	See Fig. B
OIRR	Min. Off Isolation Rejection Ratio		54			50		dB	$f = 1MHz$, $R_L = 100\Omega$, $C_L \leq 5pF$ See Fig. C, (Note 1)
I_D^+	+Power Supply Quiescent Current	1000	750	600	1500	1000	1000	μA	$V_{IN} = 0V$ to $5V$
I_Q^-	−Power Supply Quiescent Current	10	10	100	20	20	200	μA	
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio		54			50		dB	One Channel Off (Note 1)

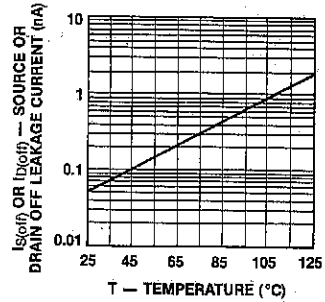
Note 1: These parameters not tested in production.

TYPICAL CHARACTERISTICS









3

APPLICATIONS

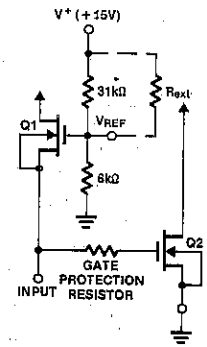
Using the V_{REF} Terminal

The DG201 has an internal voltage divider setting the TTL threshold on the input control lines for +15V on V^+. The schematic is shown here, with nominal resistor values, giving approximately 2.4V on the V_{REF} pin. As the TTL input signal goes from +0.8V to +2.4V, Q1 and Q2 switch states to turn the switch ON and OFF.

If the power supply voltage is less than +15V, then a resistor needs to be added between V^+ and the V_{REF} pin, to restore +2.4V at V_{REF}. The table shows the value of this resistor for various supply voltages, to maintain TTL compatibility. If CMOS logic levels on a +5V supply are being used, the threshold shifts are less critical, but a separate column of suitable values is given in the table. For logic swings of −5V to +5V, no resistor is needed.

In general, the "low" logic level should be < 0.8V to prevent Q1 and Q2 from both being ON together (this will cause incorrect switch function). With open collector logic, and a low value of pull-up resistor, the logic "low" level can be above 0.8V. In this case, INTERSIL can supply parts with thresholds > 1.5V, allowing the user to define the "low" as < 1.5V (consult factory). The V_{REF} point should be set at least 2.6V above this "low" state, or to > 4.1V. An external resistor of 27kΩ between V^+ and V_{REF} is required, for a +15V supply.

V^+ Supply (V)	TTL Resistor (kΩ)	CMOS Resistor (kΩ)
+15	—	—
+12	100	—
+10	51	—
+9	(34)	34
+8	(27)	27
+7	18	18



IH5009 — IH5024
Virtual Ground Analog Switches

FEATURES

- **Switches Analog Signals up to 20 Volts Peak-to-Peak**
- **Each Channel Complete — Interfaces with Most Integrated Logic**
- **Switching Speeds Less than 0.5μs**
- **$I_{D(OFF)}$ Less than 500pA Typical at 70°C**
- **Effective $r_{ds(ON)}$ — 5Ω to 50Ω**
- **Commercial and Military Temperature Range Operation**

3

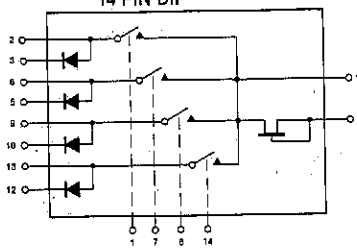
GENERAL DESCRIPTION

The IH5009 series of analog switches were designed to fill the need for an easy-to-use, inexpensive switch for both industrial and military applications. Although low cost is a primary design objective, performance and versatility have not been sacrificed.

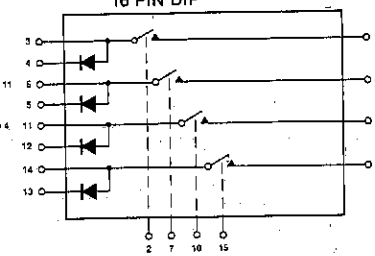
Each package contains up to four channels of analog gating and is designed to eliminate the need for an external driver. The odd numbered devices are designed to be driven directly from T^2L open collector logic (15 volts) while the even numbered devices are driven directly from low level T^2L logic (5 volts). Each channel simulates a SPDT switch. SPST switch action is obtained by leaving the diode cathode unconnected; for SPDT action, the cathode should be grounded (0V). The parts are intended for high performance multiplexing and commutating usage. A logic "0" turns the channel ON and a logic "1" turns the channel OFF.

PIN CONNECTIONS

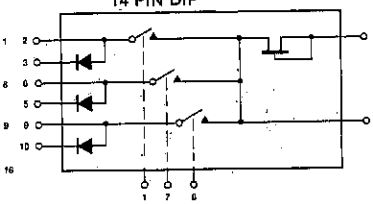
IH5009 ($r_{DS(ON)} \leq 100\Omega$)
IH5010 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP
(OUTLINE DWGS DD, PD, JD)



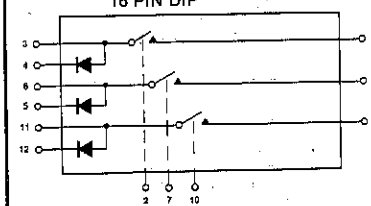
IH5011 ($r_{DS(ON)} \leq 100\Omega$)
IH5012 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN DIP
(OUTLINE DWGS DE, PE, JE)



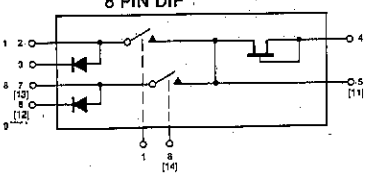
IH5013 ($r_{DS(ON)} \leq 100\Omega$)
IH5014 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP
(OUTLINE DWGS DD, PE, JE)



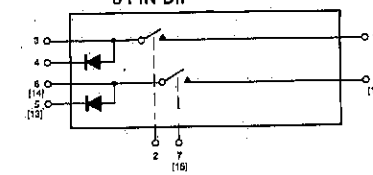
IH5015 ($r_{DS(ON)} \leq 100\Omega$)
IH5016 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN DIP
(OUTLINE DWGS DE, PE, JE)



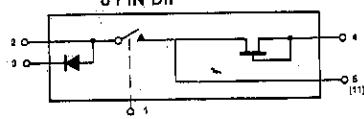
IH5017 ($r_{DS(ON)} \leq 100\Omega$)
IH5018 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP
(OUTLINE DWGS DD, PA, JD)



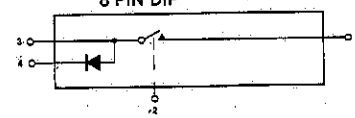
IH5019 ($r_{DS(ON)} \leq 100\Omega$)
IH5020 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP
(OUTLINE DWGS DE, PA, JE)



IH5021 ($r_{DS(ON)} \leq 100\Omega$)
IH5022 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP
(OUTLINE DWGS DD, PA, JD)



IH5023 ($r_{DS(ON)} \leq 100\Omega$)
IH5024 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP
(OUTLINE DWGS DE, PA)



(Note: Numbers in brackets refer to CERDIP packages.)

ABSOLUTE MAXIMUM RATINGS

Positive Analog Signal Voltage 30V
Negative Analog Signal Voltage ..... −15V
Diode Current 10mA
Power Dissipation (Note) 500mW
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

Operating Temperature
5009C Series ..... 0°C to +70°C
5009M Series ..... −55°C to +125°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 75°C. For higher temperature, derate at rate of 5mW/°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (per channel)

SYMBOL (Note 1)	CHARACTERISTIC	TYPE (Note 4)	TEST CONDITIONS (Note 2)	SPECIFICATION LIMIT −55°C (M) 0°C (C) MIN/MAX	SPECIFICATION LIMIT 25°C TYP.	SPECIFICATION LIMIT 25°C MIN/MAX	SPECIFICATION LIMIT +125°C (M) +70°C (C) MIN/MAX	UNITS
$I_{IN(ON)}$	Input Current-ON	All	V_{IN}=0V, I_D=2mA	0.1	.01	0.1	100	µA
$I_{IN(OFF)}$	Input Current-OFF	5V Logic Ckts	V_{IN}=+4.5V, V_A=±10V	0.2	.04	0.1	10	nA
$I_{IN(OFF)}$	Input Current-OFF	15V Logic Ckts	V_{IN}=+11V, V_A=±10V	0.2	.04	0.2	10	nA
$V_{IN(ON)}$	Channel Control Voltage-ON	5V Logic Ckts	See Figure 5, Note 3	0.5		0.5	0.5	V
$V_{IN(ON)}$	Channel Control Voltage-ON	15V Logic Ckts	See Figure 6, Note 3	1.5		1.5	1.5	V
$V_{IN(OFF)}$	Channel Control Voltage-OFF	5V Logic Ckts	See Figure 5, Note 3	4.5		4.5	4.5	V
$V_{IN(OFF)}$	Channel Control Voltage-OFF	15V Logic Ckts	See Figure 6, Note 3	11.0		11.0	11.0	V
$I_{D(OFF)}$	Leakage Current-OFF	5V Logic Ckts	V_{IN}=+4.5V, V_A=±10V	0.2	.02	0.2	10	nA
$I_{D(OFF)}$	Leakage Current-OFF	15V Logic Ckts	V_{IN}=+11V, V_A=±10V	0.2	.02	0.2	10	nA
$I_{D(ON)}$	Leakage Current-ON	5V Logic Ckts	V_{IN}=0V, I_S=1mA	1.0	0.30	1.0	1000 (M) 200 (C)	nA
$I_{D(ON)}$	Leakage Current-ON	15V Logic Ckts	V_{IN}=0V, I_S=1mA	0.5	0.10	0.5	500 (M) 100 (C)	nA
$I_{D(ON)}$	Leakage Current-ON	5V Logic Ckts	V_{IN}=0V, I_S=2mA	1.0		1.0	10	µA
$I_{D(ON)}$	Leakage Current-ON	15V Logic Ckts	V_{IN}=0V, I_S=2mA	2.0		2.0	1000	nA
$r_{DS(ON)}$	Drain-Source ON-Resistance	5V Logic Ckts	I_D=2mA, V_{IN}=0.5V	150	90	150	385 (M) 240 (C)	Ω
$r_{DS(ON)}$	Drain-Source ON-Resistance	15V Logic Ckts	I_D=2mA, V_{IN}=1.5V	100	60	100	250 (M) 160 (C)	Ω
$t_{(on)}$	Turn-ON Time	All	See Figures 3 & 4		150	500		ns
$t_{(off)}$	Turn-OFF Time	All	See Figures 3 & 4		300	500		ns
CT	Cross Talk	All	f=100Hz		120			dB

NOTE 1: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.
NOTE 2: Refer to Figure 2 for definition of terms.
NOTE 3: $V_{IN(ON)}$ and $V_{IN(OFF)}$ are test conditions guaranteed by the tests of respectively $r_{DS(ON)}$ and $I_{D(OFF)}$.
NOTE 4: "5V Logic CKTS" applies to even-numbered devices.
"15V Logic CKTS" applies to odd-numbered devices.

ORDERING INFORMATION

IH50XX — M — DE

PACKAGE:
- PA — 8-PIN PLASTIC DIP
- PD — 14-PIN PLASTIC DIP
- PE — 16-PIN PLASTIC DIP
- DD — 14-PIN CERAMIC DIP (Special Order Only)
- DE — 16-PIN CERAMIC DIP (Special Order Only)
- JD — 14-PIN CERDIP
- JE — 16-PIN CERDIP

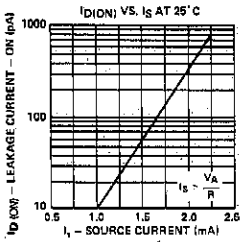
TEMPERATURE RANGE
M = MILITARY (−55°C to +125°C)
C = COMMERCIAL (0°C to +70°C)

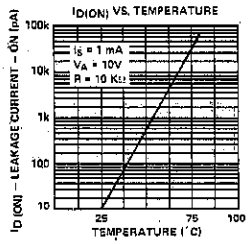
BASIC PART NUMBER

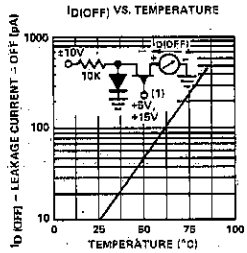
BASIC PART NUMBER	CHANNELS	LOGIC LEVEL	PACKAGES
IH5009	4	+15	JD,DD,PD
IH5010	4	+ 5	JD,DD,PD
IH5011	4	+15	JE,DE,PE
IH5012	4	+ 5	JE,DE,PE
IH5013	3	+15	JD,DD,PD
IH5014	3	+ 5	JD,DD,PD
IH5015	3	+15	JE,DE,PE
IH5016	3	+ 5	JE,DE,PE
IH5017	2	+15	JD,DD,PA
IH5018	2	+ 5	JD,DD,PA
IH5019	2	+15	JE,DE,PA
IH5020	2	+ 5	JE,DE,PA
IH5021	1	+15	JD,DD,PA
IH5022	1	+ 5	JD,DD,PA
IH5023	1	+15	JE,DE,PA
IH5024	1	+ 5	JE,DE,PA

NOTE: Mil-Temperature range (−55°C to +125°C) available ceramic packages only.

TYPICAL ELECTRICAL CHARACTERISTICS (per channel)







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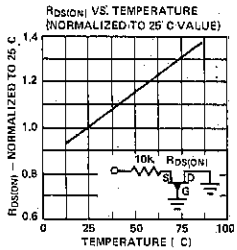
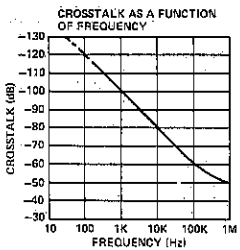
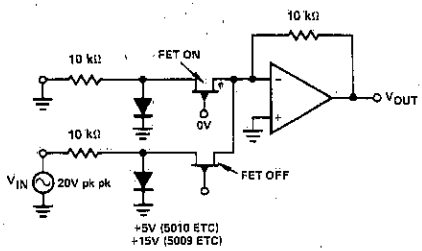




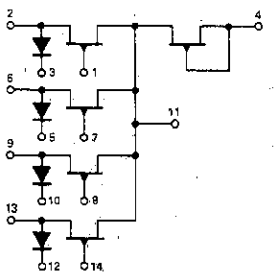
CROSSTALK MEASUREMENT CIRCUIT



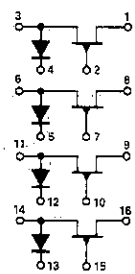
DEVICE SCHEMATICS AND PIN CONNECTIONS

FOUR CHANNEL

IH5009 ($r_{DS(ON)} \leq 100\Omega$)
IH5010 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP

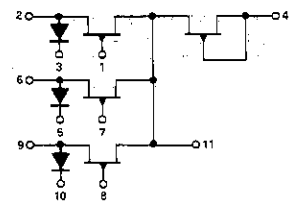


IH5011 ($r_{DS(ON)} \leq 100\Omega$)
IH5012 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN DIP

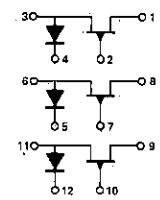


THREE CHANNEL

IH5013 ($r_{DS(ON)} \leq 100\Omega$)
IH5014 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP

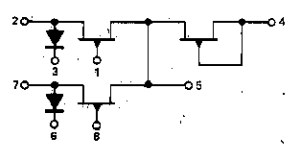


IH5015 ($r_{DS(ON)} \leq 100\Omega$)
IH5016 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN DIP

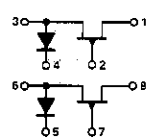


TWO CHANNEL

IH5017 ($r_{DS(ON)} \leq 100\Omega$)
IH5018 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP

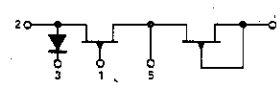


IH5019 ($r_{DS(ON)} \leq 100\Omega$)
IH5020 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP

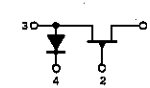


SINGLE CHANNEL

IH5021 ($r_{DS(ON)} \leq 100\Omega$)
IH5022 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



IH5023 ($r_{DS(ON)} \leq 100\Omega$)
IH5024 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



THEORY OF OPERATION

The signals seen at the drain of a junction FET type analog switch can be arbitrarily divided into two categories; those which are less than ±200mV, and those which are greater than ±200mV. The former category includes all those circuits where switching is performed at the virtual ground point of an op-amp, and it is primarily towards these applications that the IH5009 family of circuits is directed.

By limiting the analog signal at the switching point to ±200mV, no external driver is required and the need for additional power supplies is eliminated.

Devices are available with both common drains and with uncommitted drains.

Those devices which feature common drains have another FET in addition to the channel switches. This FET, which has gate and source connected such that $V_{GS} = 0$, is intended to compensate for the on-resistance of the switch. When placed in series with the feedback resistor (Figure 1) the gain is given by

$$\text{GAIN} = \frac{10k\Omega + r_{DS(ON)}\ \text{(compensator)}}{10k\Omega + r_{DS}\ \text{(switch)}}$$

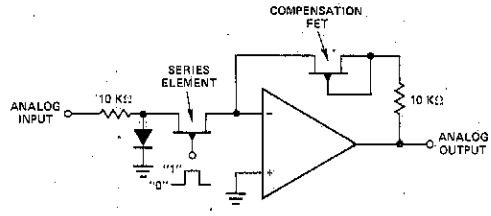


Figure 1. Use of Compensation FET

Clearly, the gain error caused by the switch is dependent on the match between the FETs rather than the absolute value of the FET on-resistance. For the standard product, all the FETs in a given package are guaranteed to match within 50Ω. Selections down to 5Ω are available however. Contact factory for details. Since the absolute value of $r_{DS(ON)}$ is guaranteed only to be less than 100Ω or 150Ω, a substantial improvement in gain accuracy can be obtained by using the compensating FET.

DEFINITION OF TERMS

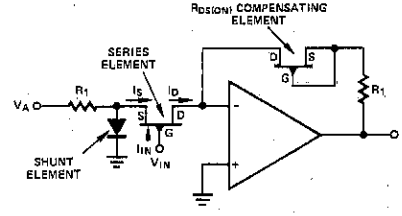


Figure 2.

NOISE IMMUNITY

The advantage of SPDT switching is high noise immunity when the series elements is OFF. For example, if a ±10V analog input is being switched by T²L open collector logic, the series switch is OFF when the logic level is at +15 volts. At this time, the diode conducts and holds the source at approximately +0.7 volts with an AC impedance to ground of 25 ohms. Thus random noise superimposed on the +10 volt analog input will not falsely trigger the FET since the noise voltage will be shunted to ground.

When switching a negative voltage, the input further increases the OFF voltage beyond pinch-off, so there is no danger of the FET turning on.

SWITCHING CHARACTERISTICS

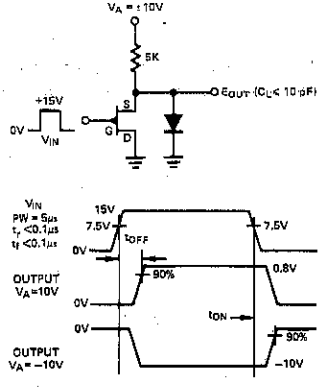


Figure 3. High Level Logic

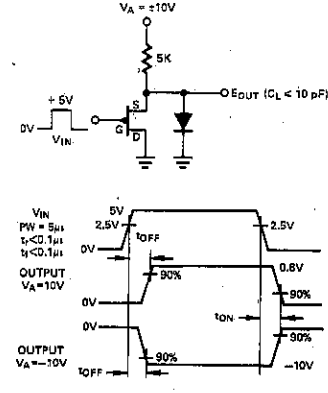


Figure 4. Standard DTL, TTL, RTL

LOGIC INTERFACE CIRCUITS

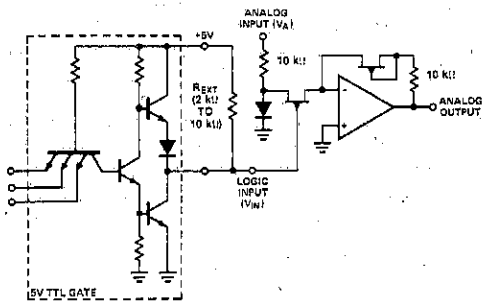


Figure 5. Interfacing with +5V Logic

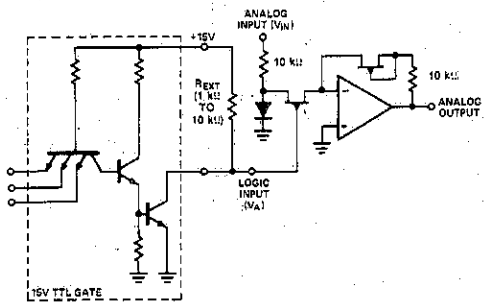
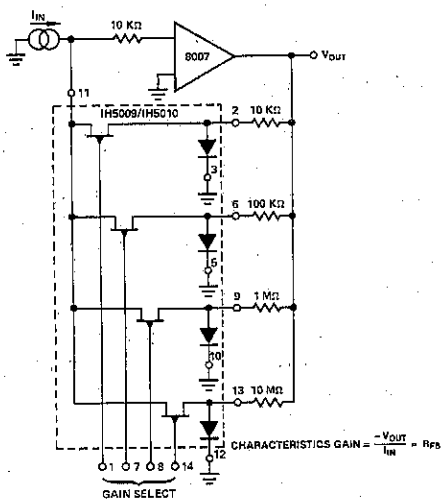
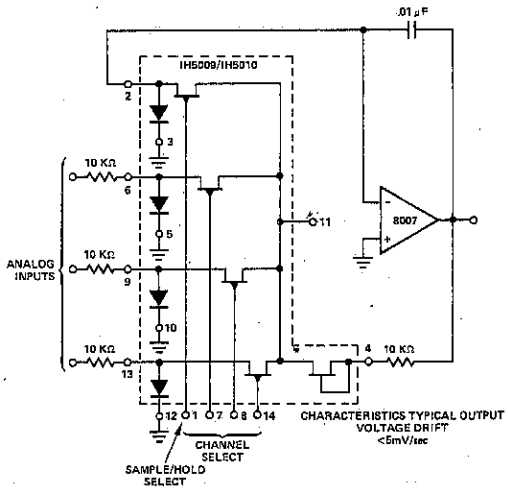


Figure 6. Interfacing with +15V Open Collector Logic

3

APPLICATIONS (Note)





NOTE: Additional applications information is given in Application Bulletins A003 "Understanding and Applying the Analog Switch" and A004 "The 5009 Series of Low Cost Analog Switches". See also September '79 issue of Product Engineering "Analog Switching" by Paresh Maniar.

IH5025 — IH5038
Positive Signal Analog Switches

FEATURES

- **Switches up to +20V into High Impedance Loads (i.e. Non-Inverting Input of Operational Amp.)**
- **Driven from TTL Open Collector Logic**
- **$I_{D(OFF)} < 50pA$**
- **$r_{DS(ON)} < 150\Omega$**
- **$r_{DS(ON)}$ Match $< 50\Omega$ Channel to Channel**
- **Switching Speeds < 100ns**

GENERAL DESCRIPTION

The IH5025 series of analog switches was designed to fill the need for an easy-to-use, inexpensive switch for both industrial and military applications. Although low cost is a primary design objective, performance and versatility have not been sacrificed.

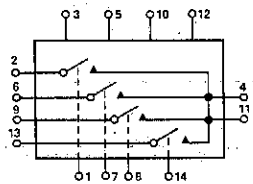
Each package contains up to four channels of analog gating and is designed to eliminate the need for an external driver.

3

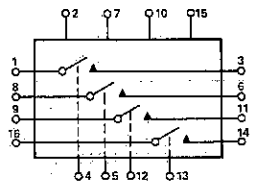
The entire family is designed to be driven from TTL open collector logic (15V), but can be driven from 5V logic if signal input is less than 1V. Alternatively, 20V switching is readily obtainable if TTL supply voltage is +25V. Normally, only positive signals can be switched; however, up to ±10V can be handled by the addition of a PNP stage (Figure 11) or by capacitor isolation (Figure 10). Each channel is a SPST switch. A logic "0" turns the channel ON and a logic "1" turns the channel OFF.

PIN CONNECTIONS

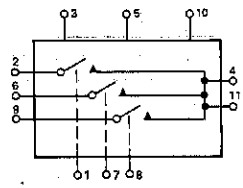
IH5025 ($r_{DS(ON)} \leq 100\Omega$)
IH5026 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP



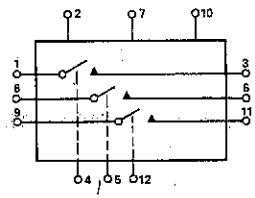
IH5027 ($r_{DS(ON)} \leq 100\Omega$)
IH5028 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN DIP



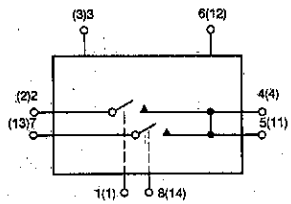
IH5029 ($r_{DS(ON)} \leq 100\Omega$)
IH5030 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP



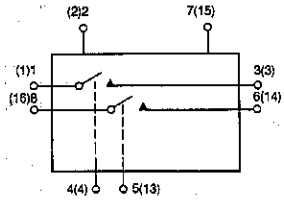
IH5031 ($r_{DS(ON)} \leq 100\Omega$)
IH5032 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN DIP



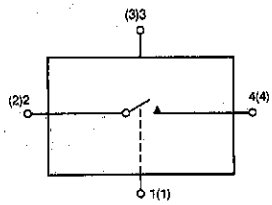
IH5033 ($r_{DS(ON)} \leq 100\Omega$)
IH5034 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



IH5035 ($r_{DS(ON)} \leq 100\Omega$)
IH5036 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



IH5037 ($r_{DS(ON)} \leq 100\Omega$)
IH5038 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



NUMBERS IN PARENTHESES INDICATE CERAMIC PACKAGE PIN-OUT

ABSOLUTE MAXIMUM RATINGS

Positive Analog Signal Voltage 25V
Negative Analog Signal Voltage ..... −0.5VDC
Drain Current 25mA
Power Dissipation (Note) 500mW
Storage Temperature ..... −65°C to +150°C

Operating Temperature
5025C Series ..... 0°C to +70°C
5025M Series ..... −55°C to +125°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 75°C. For higher temperature, derate at rate of 5mW/°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (per channel)

SYMBOL (Note 1)	CHARACTERISTIC	TYPE	TEST CONDITIONS	SPECIFICATION LIMIT				UNITS MIN/MAX
				−55°C (M) 0°C (C)	25°C		+125°C (M) +70°C (C)	
					TYP.	MIN/MAX		
$I_{IN(ON)}$	Input Current-ON	All	V_{IN} = 0V		0.30	1.0	100 (M) 25 (C)	nA (max)
$I_{IN(OFF)}$	Input Current-OFF	All	V_{IN} = 15V		0.20	1.0	50 (M) 10 (C)	nA (max)
$V_{IN(ON)}$	Channel Control Voltage-ON	All	See Figure 1	1.5		1.5	1.5	V (max)
$V_{IN(OFF)}$	Channel Control Voltage-OFF	All	See Figure 1	14.0		14.0	14.0	V (min)
$I_{D(OFF)}$	Leakage Current-OFF	All	V_{IN} = 15V		0.06	0.5	100 (M) 10 (C)	nA (max)
$I_{D(ON)}$	Leakage Current-ON	Odd Nos.	V_{IN} = 0V		1.00	10.0	5000 (M) 250 (C)	nA (max)
$I_{D(ON)}$	Leakage Current-ON	Even Nos.	V_{IN} = 0V		0.10	1.0	500 (M) 25 (C)	nA (max)
$r_{DS(ON)}$	Drain-Source ON-Resistance	Odd Nos.	V_{IN} = 0.5V, I_D = 1mA		60.00	100.0	250 (M) 150 (C)	Ω (max)
$r_{DS(ON)}$	Drain-Source ON-Resistance	Even Nos.	V_{IN} = 0.5V, I_D = 1mA		90.00	150.0	385 (M) 240 (C)	Ω (max)
$r_{DS(ON)}$	Drain-Source ON-Resistance	Odd Nos.	V_{IN} = 1.0V, I_D = 1mA		85.00	160.0	420 (M) 250 (C)	Ω (max)
$r_{DS(ON)}$	Drain-Source ON-Resistance	Even Nos.	V_{IN} = 1.0V, I_D = 1mA		110.00	200.0	400 (M) 250 (C)	Ω (max)
$t_{(on)}$	Turn-ON Time	All	See Figure 2		0.10	0.2	0.4	μs (max)
$t_{(off)}$	Turn-OFF Time	All	See Figure 2		0.10	0.2	0.4	μs (max)
$Q_{(INJ)}$	Charge Injection	All	See Figure 3		7.00	20.0		mV_{p-p} (max)
$V_{A(OFF)}$	Cross Coupling Rejection	All	See Figure 4		0.10	1.0		mV_{p-p} (max)
$\Delta r_{DS(ON)}$	Channel to Channel $r_{DS(ON)}$ Match	All	V_{IN} = 0.5V, I_D = 1mA		25.00	50.0	50	Ω (max)

NOTE 1: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.

ORDERING INFORMATION

IH50XX — M — DE

PACKAGE:
- PA — 8-PIN PLASTIC DIP
- PD — 14-PIN PLASTIC DIP
- PE — 16-PIN PLASTIC DIP
- DD — 14-PIN CERAMIC DIP (Special Order Only)
- DE — 16-PIN CERAMIC DIP (Special Order Only)
- JD — 14-PIN CERDIP
- JE — 16-PIN CERDIP

TEMPERATURE RANGE
M = MILITARY (−55°C to +125°C)
C = COMMERCIAL (0°C to +70°C)

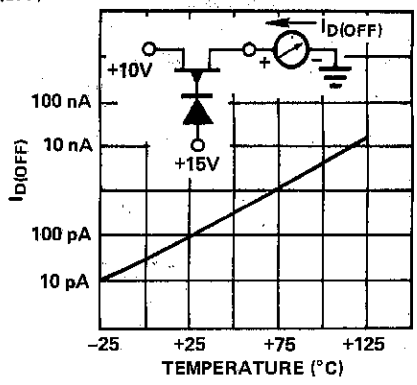
BASIC PART NUMBER

BASIC PART NUMBER	CHANNELS	LOGIC LEVEL	PACKAGES
IH5025	4	+15	JD,DD,PD
IH5026	4	+ 5	JD,DD,PD
IH5027	4	+15	JE,DE,PE
IH5028	4	+ 5	JE,DE,PE
IH5029	3	+15	JD,DD,PD
IH5030	3	+ 5	JD,DD,PD
IH5031	3	+15	JE,DE,PE
IH5032	3	+ 5	JE,DE,PE
IH5033	2	+15	JD,DD,PA
IH5034	2	+ 5	JD,DD,PA
IH5035	2	+15	JE,DE,PA
IH5036	2	+ 5	JE,DE,PA
IH5037	1	+15	JD,DD,PA
IH5038	1	+ 5	JD,DD,PA

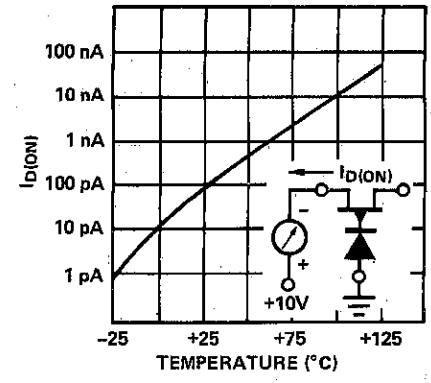
NOTE: Mil-Temperature range (−55°C to +125°C) available in ceramic packages only.

TYPICAL ELECTRICAL CHARACTERISTICS (per channel)

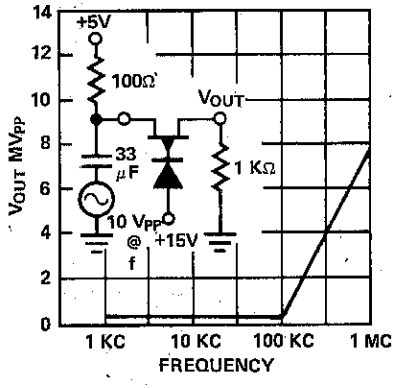
$I_{D(OFF)}$ VS. TEMPERATURE



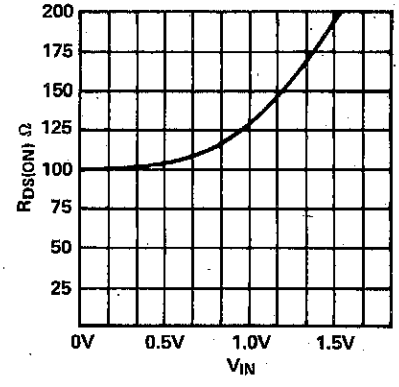
$I_{D(ON)}$ VS. TEMPERATURE



CROSS COUPLING REJECTION VS. FREQUENCY



$R_{DS(ON)}$ VS. V_{IN}



TEST CIRCUITS

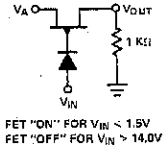


Figure 1

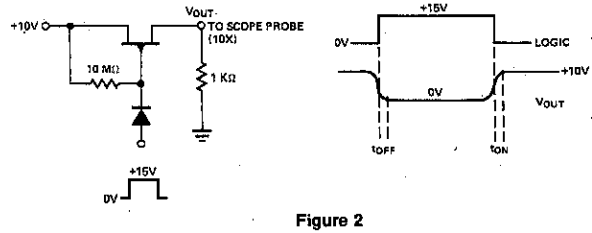


Figure 2

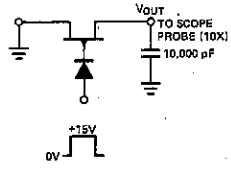


Figure 3

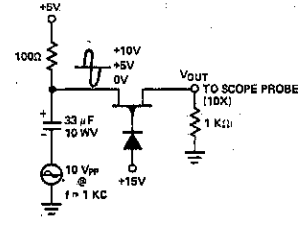
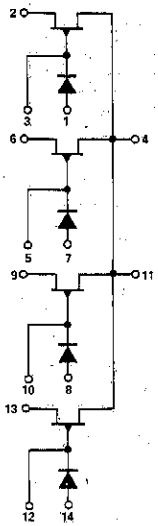


Figure 4

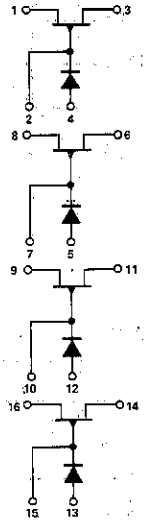
DEVICE SCHEMATICS

FOUR CHANNEL

IH5025 ($r_{DS(ON)} \leq 100\Omega$)
IH5026 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP

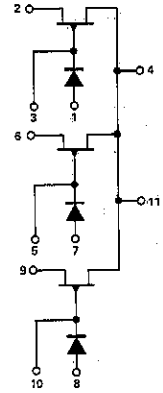


IH5027 ($r_{DS(ON)} \leq 100\Omega$)
IH5028 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN DIP

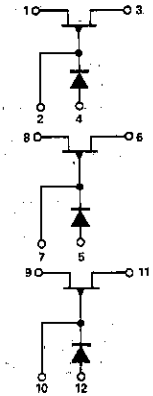


THREE CHANNEL

IH5029 ($r_{DS(ON)} \leq 100\Omega$)
IH5030 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP

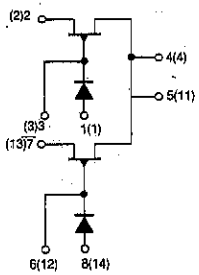


IH5031 ($r_{DS(ON)} \leq 100\Omega$)
IH5032 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN DIP

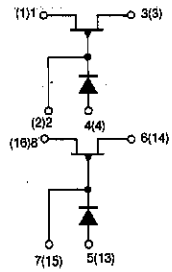


TWO CHANNEL

IH5033 ($r_{DS(ON)} \leq 100\Omega$)
IH5034 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP

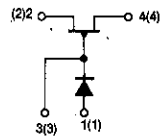


IH5035 ($r_{DS(ON)} \leq 100\Omega$)
IH5036 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



SINGLE CHANNEL

IH5037 ($r_{DS(ON)} \leq 100\Omega$)
IH5038 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



Numbers in parentheses indicate CERAMIC PACKAGE LAYOUT

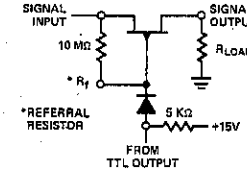
THEORY OF OPERATION

The IH5025 series differs from the IH5009 series in that they may be driven by floating outputs. This family is generally used when operating into the non-inverting input of an operational amplifier, while the IH5009 series is used in operations where the output feeds into the inverting (virtual ground) input.

The IH5025 model is a basic charge area switching device, in that proper gating action depends upon the capacity vs. voltage relationship for the diode junctions. This C vs. V, when integrated, produces total charge Q. It is Q total which is switched between the series diode and the gate to source and gate to drain junctions. The charge area (C vs. V) for the diode has been chosen to be a minimum of four (4) times the area of the gate to source junction, thus providing adequate safety margins to insure proper switching action.

If normal logical voltage levels of ground to +15V (open collector TTL) are used, only signals which are between 0V and +10V can be switched. The pinch-off range of the P-Channel FET has been selected between 2.0V and 3.9V; thus with +15V at the logical input, and a +10V signal input, 1.1V of margin exists for turn-off. When the IH5025 is used with 5V TTL logic, a maximum of +1V can be switched.

The gate of each FET has been brought out so that a "referral resistor" can be placed between gate and source. This is used to minimize charge injection effects. The connection is shown below:



For switching levels > +10V, the +15V power supply must be increased so that there is a minimum of 5V of difference between supply and signal. For example, to switch +15V level, +20V TTL supply is required. Up to +20V levels can be gated.

3

LOGIC INTERFACE CIRCUITS

When operating with TTL logic it is necessary to use pull-up resistors as shown in Figures 6 and 7. This ensures the necessary positive voltages for proper gating action.

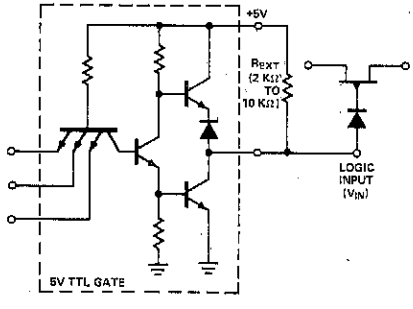


Figure 5. Interfacing with +5V Logic

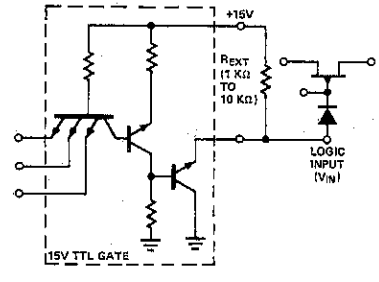


Figure 6. Interfacing with +15V Open Collector Logic

APPLICATIONS

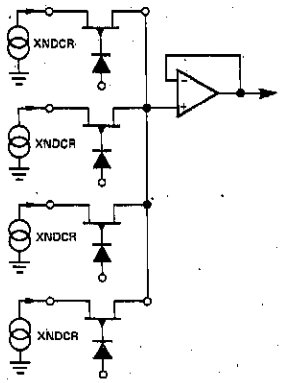


Figure 7. Multiplexer from Positive Output Transducers

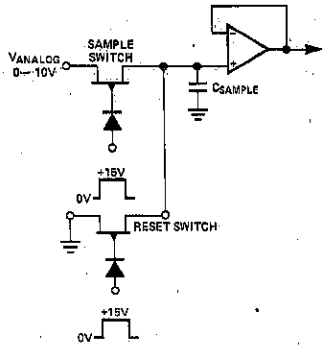


Figure 8. Sample and Hold Switch

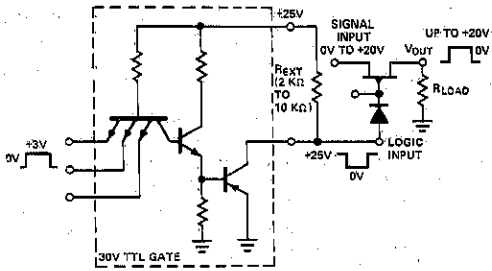
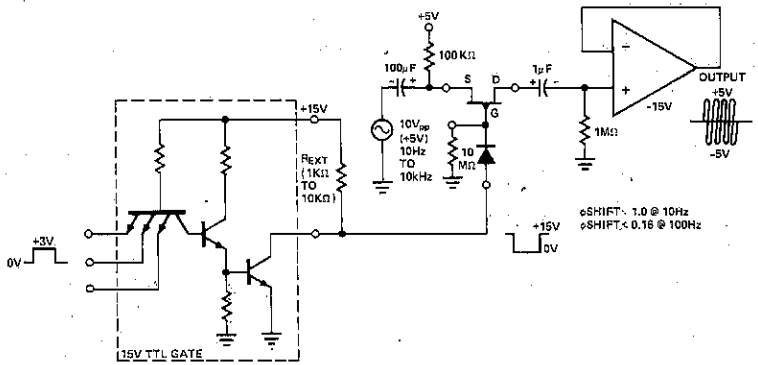
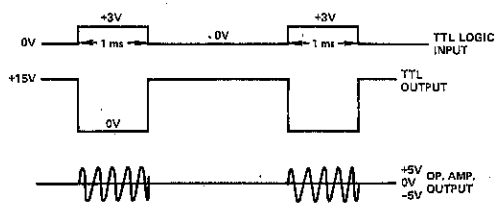


Figure 9. Switching up to +20V Signals with T²L Logic

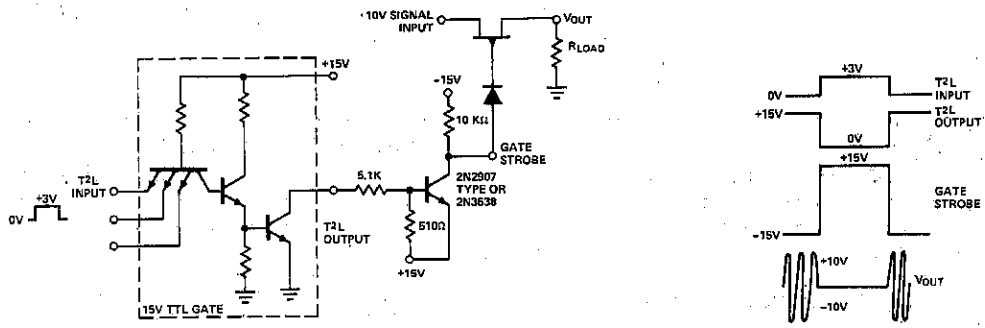




NOTE: TO SWITCH ±10 VAC (20Vpp): (1) INCREASE +5V SUPPLY TO +10V. (2) INCREASE TTL SUPPLY FROM +15V TO +25V.

Figure 10. Switching Bipolar Signals with T²L Logic

APPLICATIONS (Cont.)



ADVANTAGES OVER FIGURE NO. 10 METHOD
A. DC LEVELS OF UP TO ±10V CAN BE SWITCHED, AS WELL AS AC SIGNALS UP TO 100 KC; NO. 10 METHOD SWITCHES ONLY AC RANGE OF 10 Hz TO 10 kHz.
B. CKT IS NOW BREAK BEFORE MAKE

DISADVANTAGES:
A. PNP CKT DRAWS 3 mA, WHEN ON; THUS ADDS 3 mA X 30V = 90 mW POWER DISS.
B. t_{ON} TIME WILL BE CONSIDERABLY SLOWED DOWN FROM 100 ns (BEFORE IN FIGURE NO. 10) TO 1 - 2 µs NOW.

Figure 11. Switching Bipolar Signals with T²L Logic (Alternate Method)

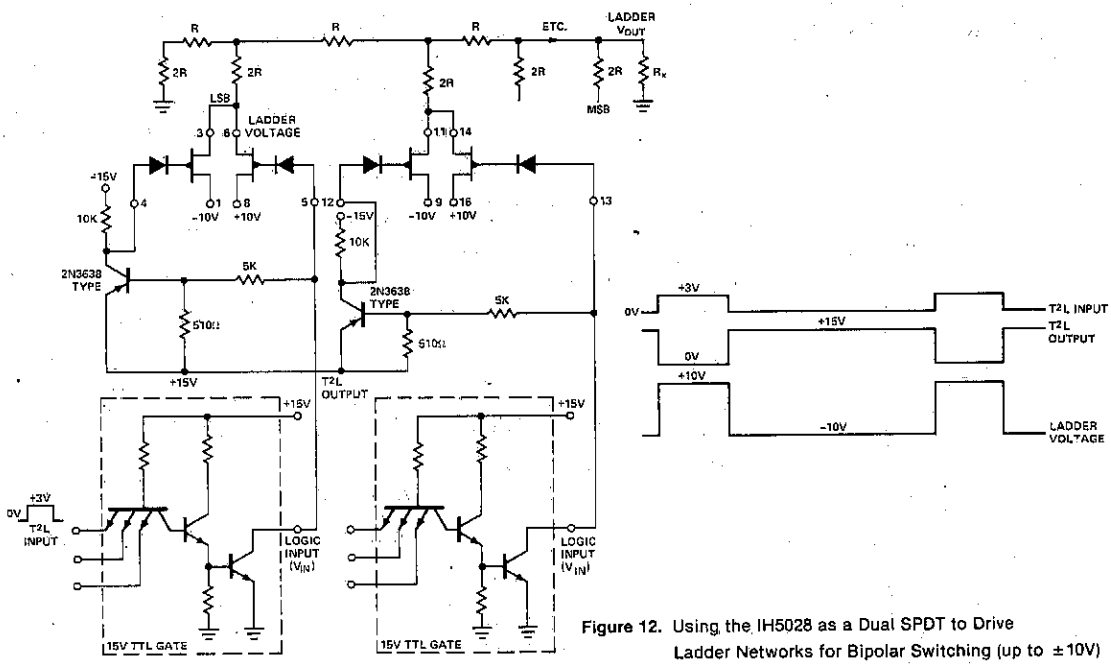
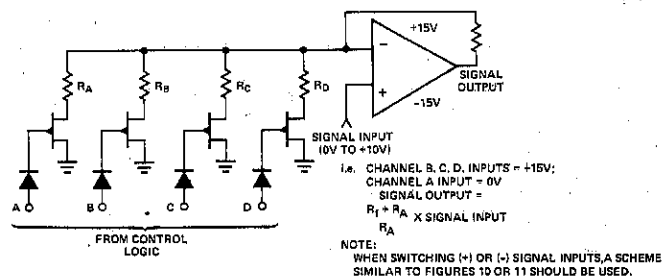


Figure 12. Using the IH5028 as a Dual SPDT to Drive Ladder Networks for Bipolar Switching (up to ±10V)



i.e. CHANNEL B, C, D, INPUTS = +15V;
CHANNEL A INPUT = 0V
SIGNAL OUTPUT =

$$\frac{R_f + R_A}{R_A} \times \text{SIGNAL INPUT}$$

NOTE:
WHEN SWITCHING (+) OR (-) SIGNAL INPUTS, A SCHEME SIMILAR TO FIGURES 10 OR 11 SHOULD BE USED.

Figure 13. Gain Control with High Input Impedance

IH5040-IH5051 Family High Level CMOS Analog Gates

FEATURES

- Switches Greater Than 20Vpp Signals With ±15V Supplies
- Quiescent Current Less Than 1μA
- Overvoltage Protection to ±25V
- Break-Before-Make Switching t_{off} 200 nsec, t_{on} 300 nsec Typical
- T^2L, DTL, CMOS, PMOS Compatible
- Non-Latching With Supply Turn-Off
- Low $r_{DS(on)}$ — 35Ω
- New DPDT & 4PST Configurations
- Complete Monolithic Construction IH5040 through IH5047

3

FUNCTIONAL DIAGRAM

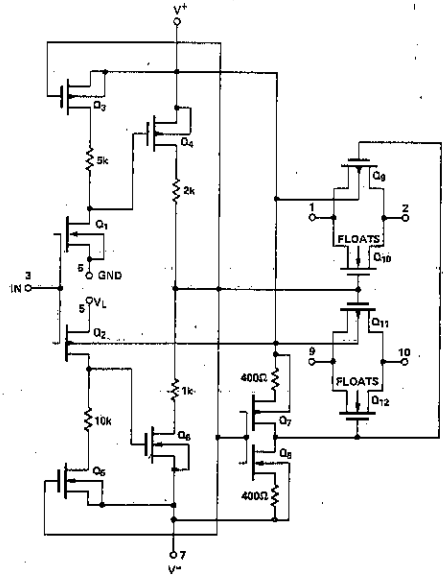
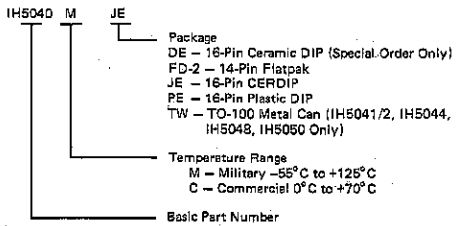


FIGURE 1. TYPICAL DRIVER, GATE — IH5042

ORDERING INFORMATION



GENERAL DESCRIPTION

The IH5040 family of solid state analog gates are designed using an improved, high voltage CMOS monolithic technology. These devices provide ease-of-use and performance advantages not previously available from solid state switches. This improved CMOS technology provides input overvoltage capability to ±25 volts without damage to the device, and destructive latch-up of solid state analog gates has been eliminated. Early CMOS gates were destroyed when power supplies were removed with an input signal present. The IH5040 CMOS technology has eliminated this serious systems problem.

Key performance advantages of the 5040 series are TTL compatibility and ultra low-power operation. The quiescent current requirement is less than 1μA. Also designed into the 5040 is guaranteed Break-Before-Make switching, which is accomplished by extending the t_{on} time (300 nsec TYP.) so that it exceeds t_{off} time (200 nsec TYP.). This insures that an ON channel will be turned OFF before an OFF channel can turn ON. This eliminates the need for external logic required to avoid channel to channel shorting during switching.

Many of the 5040 series improve upon and are pin-for-pin and electrical replacements for other solid state switches.

FUNCTIONAL DESCRIPTION

INTERSIL PART NO.	TYPE	$r_{DS(on)}$	PIN/FUNCTIONAL EQUIVALENT (Note 1)
IH5040	SPST	75Ω	
IH5041	Dual SPST	75Ω	
IH5042	SPDT	75Ω	DG 188AA/BA
IH5043	Dual SPDT	75Ω	DG 191AP/BP
IH5044	DPST	75Ω	
IH5045	Dual DPST	75Ω	DG 185AP/BP
IH5046	DPDT	75Ω	
IH5047	4PST	75Ω	
IH5048 Dual	SPST	35Ω	
IH5049 Dual	DPST	35Ω	DG 184AP/BP
IH5050	SPDT	35Ω	DG 187AA/BA
IH5051 Dual	SPDT	35Ω	DG 190AP/BP

NOTE 1. See Switching State diagrams for applicable package equivalency.

Pin and functional equivalent monolithic versions of the DG181, DG182, DG187 and DG188 are available. See data sheet for this and also IH181 to IH191.

ABSOLUTE MAXIMUM RATINGS

Current (Any Terminal) . . . . . < 30mA
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature . . . . . −55°C to +125°C
Power Dissipation 450mW
(All Leads Soldered to a P.C. Board)
Derate 6mW/°C Above 70°C
Lead Temperature (Soldering, 10 sec) . . . . . 300°C

$V^+ - V^-$	< 33V
$V^+ - V_D$	< 30V
$V_D - V^-$	< 30V
$V_D - V_S$	< ±22V
$V_L - V^-$	< 33V
$V_L - V_{IN}$	< 30V
V_L − GND	< 20V
V_{IN} − GND	< 20V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (@ 25°C, V^+ = +15 V, V^- = −15 V, V_L = +5 V)

PER CHANNEL		MIN./MAX. LIMITS							
		MILITARY			COMMERCIAL				
SYMBOL	CHARACTERISTIC	-55°C	+25°C	+125°C	0	+25°C	+70°C	UNITS	TEST CONDITIONS
$I_{IN(ON)}$	Input Logic Current	1	1	1	1	1	1	µA	V_{IN} = 2.4 V Note 1
$I_{IN(OFF)}$	Input Logic Current	1	1	1	1	1	1	µA	V_{IN} = 0.8 V Note 1
$r_{DS(on)}$	Drain–Source On Resistance	75(35)	75(35)	150(60)	80 (45)	80 (45)	130 (45)	Ω	(IH5048 Thru IH5051) I_S = 10 mA V_{ANALOG} = −10 V to +10 V
$\Delta r_{DS(ON)}$	Channel to Channel $r_{DS(ON)}$ Match		25 (15) (typ)			30(15) (typ)		Ω	(IH5048 thru IH5051)
V_{ANALOG}	Min. Analog Signal Handling Capability		±11(±10)			±10(±10)		V	
$I_{D(OFF)}$	Switch OFF Leakage Current	1(1)	1(1)	100(100)	5(5)	5(5)	100(100)	nA	V_{ANALOG} = −10 V to +10 V (IH5048 thru IH5051
$I_{D(ON)}$ + $I_{S(ON)}$	Switch On Leakage Current	2(2)	2(2)	200(200)	10 (10)	10 (10)	100(200)	nA	V_D = V_S = −10 V to + 10 V (IH5048 thru IH5051)
t_{on}	Switch "ON" Time		500(250)			500(300)		ns	R_L = 1 kΩ, V_{ANALOG} = −10 V to +10 V See Fig. A
t_{off}	Switch "OFF" Time		250(150)			250(150)		ns	R_L = 1 kΩ, V_{ANALOG} = −10 V to +10 V See Fig. A (IH5048 thru IH5051)
$Q_{(INJ.)}$	Charge Injection		15 (10)			20 (10)		mV	See Fig. B (IH5048 thru IH5051)
OIRR	Min. Off Isolation Rejection Ratio		54			50		dB	f = 1 MHz, R_L = 100Ω, C_L ≤ 5 pF See Fig. C, (Note 1)
I^+_Q	+ Power Supply Quiescent Current	1	1	10	10	10	100	µA	
I^-_Q	− Power Supply Quiescent Current	1	1	10	10	10	100	µA	V^+ = +15 V, V^- = −15 V, V_L = +5 V
I^-_{LQ}	+5 V Supply Quiescent Current	1	1	10	10	10	100	µA	
I_{GND}	Gnd Supply Quiescent Current	1	1	10	10	10	100	µA	
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio		54			50		dB	One Channel Off; Any Other Channel Switches as per Fig. E (Note 1)

Note 1: Not tested in production.

TEST CIRCUITS

FIG. A

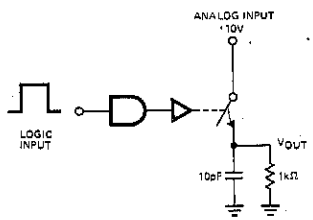


FIG. B

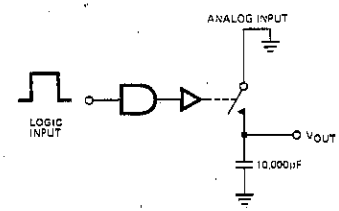
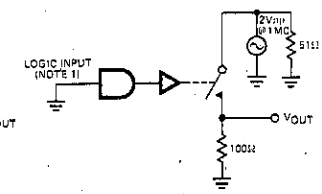
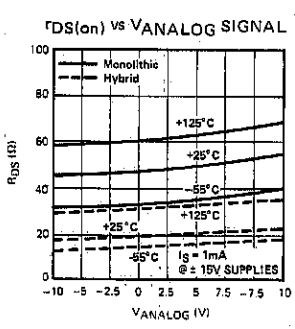


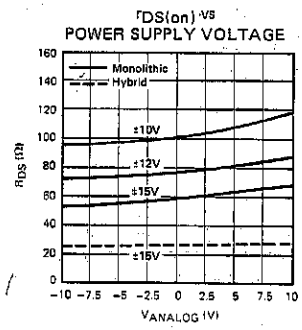
FIG. C



NOTE 1: Some channels are turned on by high "1" logic inputs and other channels are turned on by low "0" inputs; however 0.8V to 2.4V describes the min. range for switching properly. Refer to logic diagrams to see absolute value of logic input required to produce "ON" or "OFF" state.

TYPICAL ELECTRICAL CHARACTERISTICS (Per Channel)





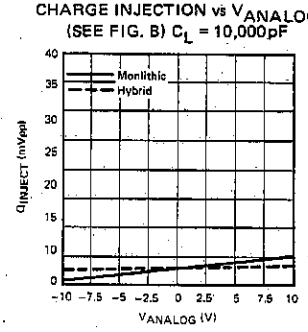
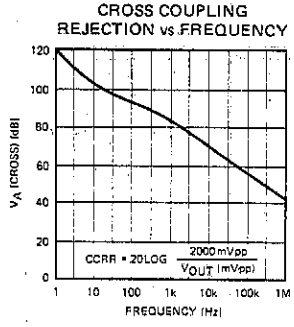


FIGURE D



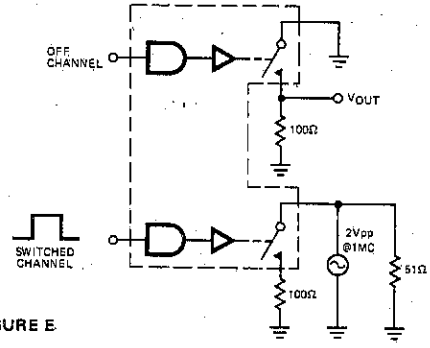
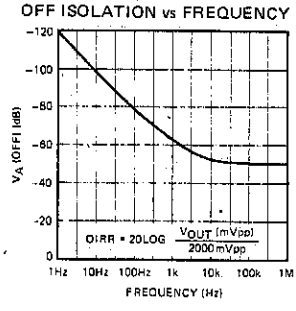


FIGURE E



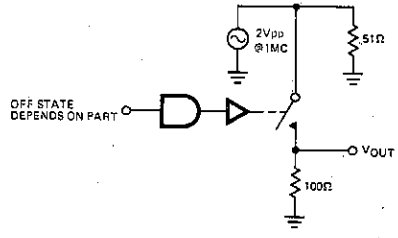
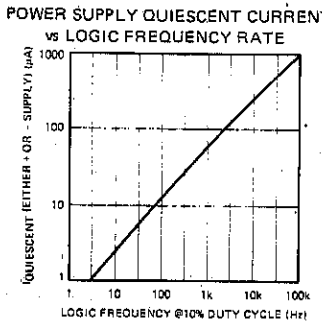


FIGURE F



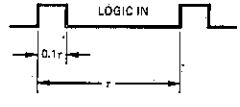
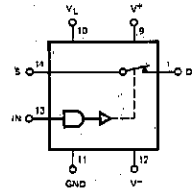
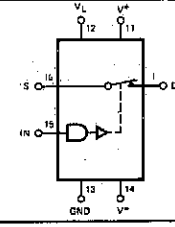
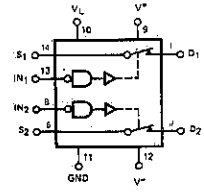
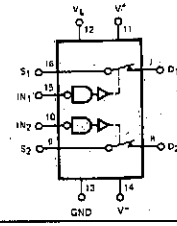
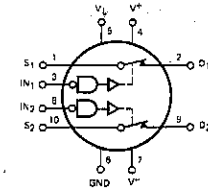
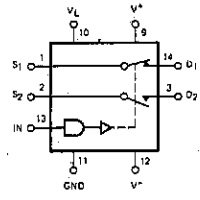
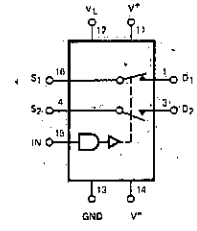
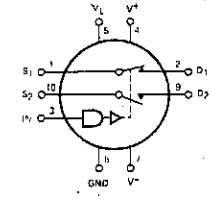
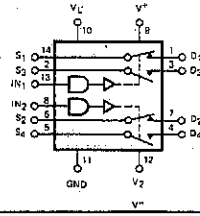
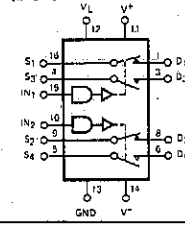
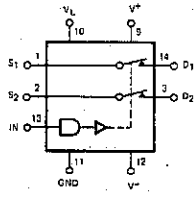
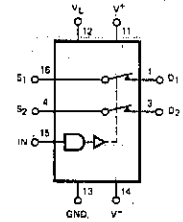
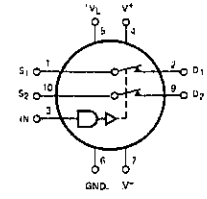
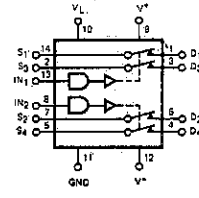
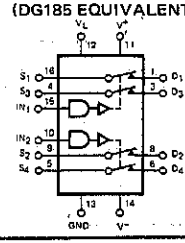


FIGURE G

SWITCHING STATE DIAGRAMS

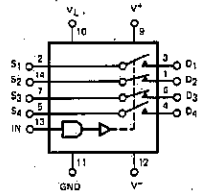
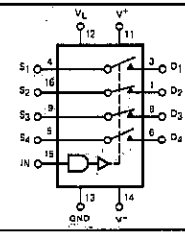
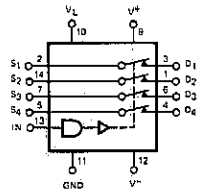
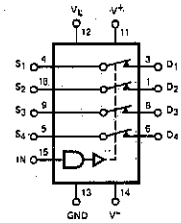
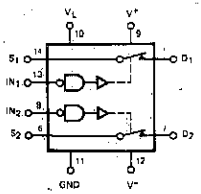
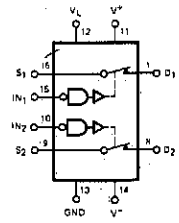
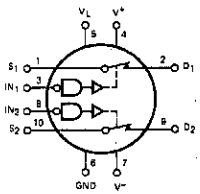
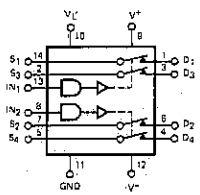
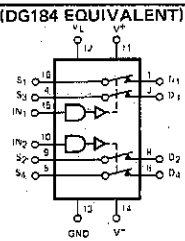
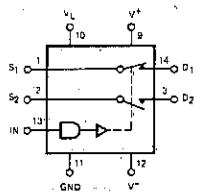
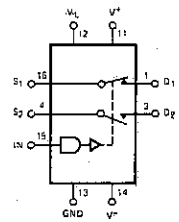
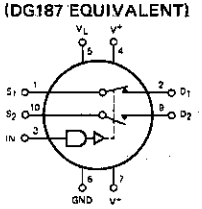
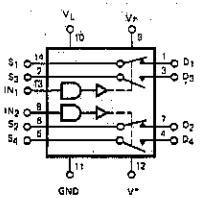
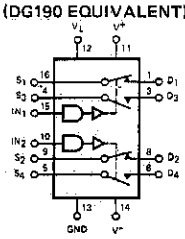
SWITCH STATES ARE FOR LOGIC "1" INPUT

	(OUTLINE DWG FD-2)	(OUTLINE DWGS DE, JE, PE)	(OUTLINE DWG TO-100)
SPST IH5040 ($r_{DS(on)}$ < 75Ω)			
DUAL SPST IH5041 ($r_{DS(on)}$ < 75Ω)			
SPDT IH5042 ($r_{DS(on)}$ < 75Ω)			(DG188 EQUIVALENT) 
DUAL SPDT IH5043 ($r_{DS(on)}$ < 75Ω)		(DG191 EQUIVALENT) 	
DPST IH5044 ($r_{DS(on)}$ < 75Ω)			
DUAL DPST IH5045 ($r_{DS(on)}$ < 75Ω)		(DG185 EQUIVALENT) 	

3

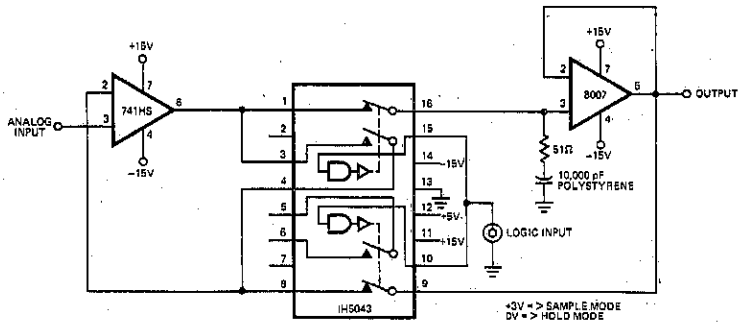
SWITCHING STATE DIAGRAMS (Cont.)

SWITCH STATES ARE FOR LOGIC "1" INPUT

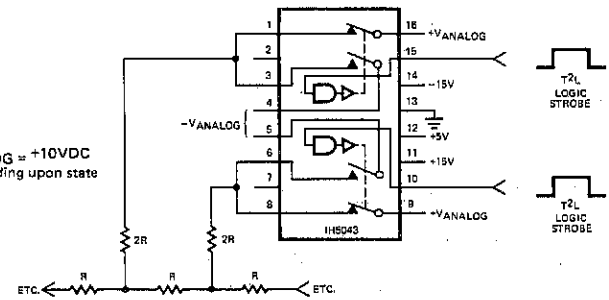
	FLAT PACKAGE (FD-2)	DIP (DE) PACKAGE	TO-100
DPDT **IH5046 (r_{DS} (ON) <75Ω)**			
4PST **IH5047 (r_{DS} (ON) <75Ω)**			
DUAL SPST **IH5048 (r_{DS} (ON) <35Ω)**			
DUAL DPST **IH5049 (r_{DS} (ON) <35Ω)**		(DG184 EQUIVALENT) 	
SPDT **IH5050 (r_{DS} (ON) <35Ω)**			(DG187 EQUIVALENT) 
DUAL SPDT **IH5051 (r_{DS} (ON) <35Ω)**		(DG190 EQUIVALENT) 	

APPLICATIONS

IMPROVED SAMPLE & HOLD
USING IH5043

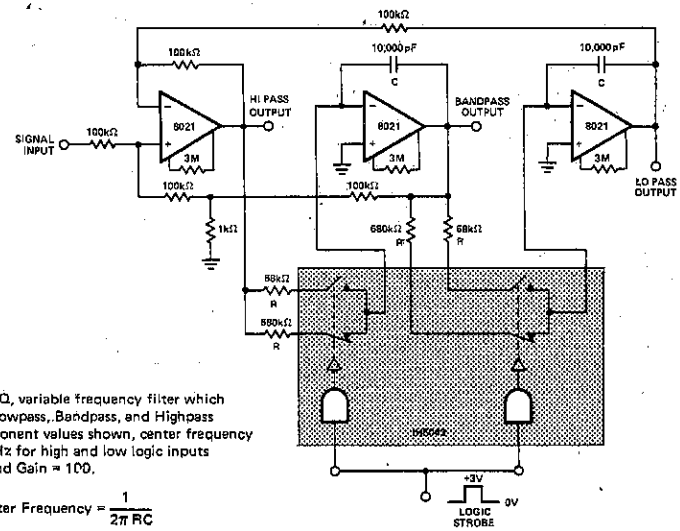


USING THE CMOS SWITCH TO DRIVE
AN R/2R LADDER NETWORK (2 LEGS)



EXAMPLE: If $-V_{ANALOG} = -10VDC$ and $+V_{ANALOG} = +10VDC$ then Ladder Legs are switched between ±10VDC, depending upon state of Logic Strobe.

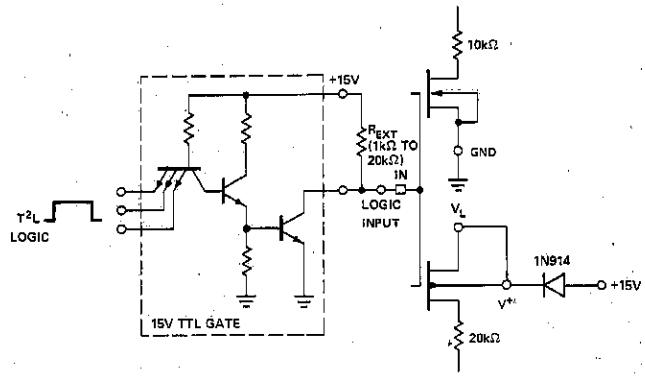
DIGITALLY TUNED
LOW POWER ACTIVE FILTER



Constant gain, constant Q, variable frequency filter which provides simultaneous Lowpass, Bandpass, and Highpass outputs. With the component values shown, center frequency will be 235Hz and 23.5Hz for high and low logic inputs respectively, Q = 100, and Gain = 100.

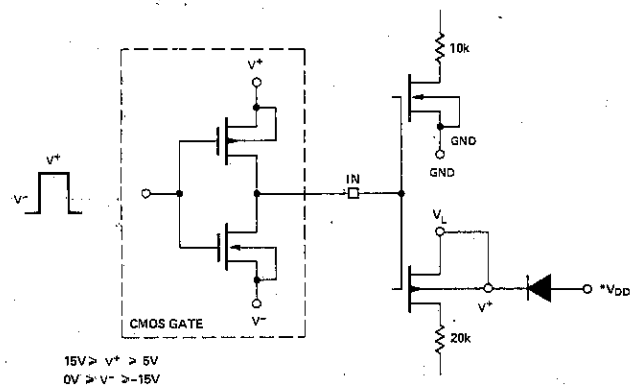
$$f_n = \text{Center Frequency} = \frac{1}{2\pi RC}$$

FOR INTERFACING WITH T²L OPEN COLLECTOR LOGIC.



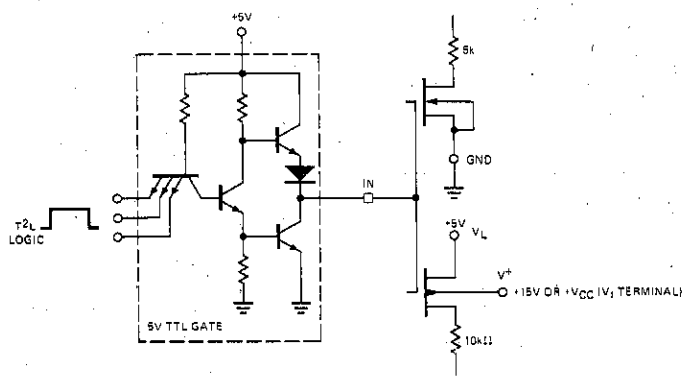
TYP. EXAMPLE FOR +15V CASE SHOWN

FOR USE WITH CMOS LOGIC.



15V ≥ V+ ≥ 5V
0V ≥ V- ≥ -15V

LOGIC INTERFACING



INTERSIL

MAXIMUM RATINGS

Current (Any Terminal) ..... <30mA
Storage Temperature ..... −65°C to +150°C
Operating Temperature ..... −55°C to +125°C
Power Dissipation 450mW
(All Leads Soldered to a P.C. Board)
Derate 6 mW/°C Above 70°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

$V^+ - V^-$ ..... <33V
$V^+ - V_D$ ..... <30V
$V_D - V^-$ ..... <30V
$V_D - V_S$ ..... < ±22V
$V_L - V^-$ ..... <33V
$V_L - V_{IN}$ ..... <30V
V_L-GND ..... <20V
V_{IN}-GND ..... <20V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (@25°C, $V^+ = +15V$, $V^- = -15V$, $V_L = +5V$, GND = 0V)

PER CHANNEL		MIN./MAX. LIMITS							TEST CONDITIONS
		MILITARY			COMMERCIAL				
SYMBOL	CHARACTERISTIC	−55°C	+25°C	+125°C	0	+25°C	+70°C	UNITS	
$I_{IN(ON)}$	Input Logic Current	1	1	1	1	1	1	µA	V_{IN} = 2.4V (IH5053) = 0.8V (IH5052)
$I_{IN(OFF)}$	Input Logic Current	1	1	1	1	1	1	µA	V_{IN} = 0.8V (IH5053) = 2.4V (IH5052)
$r_{DS(ON)}$	Drain-Source On Resistance	75	75	100	80	80	100	Ω	I_S = 10mA, V_{analog} = 10V to +10V
$\Delta r_{DS(ON)}$	Channel to Channel $R_{DS(ON)}$ Match		25 (typ)			30 (typ)		Ω	
V_{ANALOG}	Min. Analog Signal Handling Capability		±11			±10		V	
$I_{D(OFF)}$	Switch OFF Leakage Current	1	1	100	5	5	100	nA	V_{ANALOG} = −10V to +10V
$I_{D(ON)}$ + $I_{S(ON)}$	Switch On Leakage Current	2	2	200	10	10	100	nA	$V_D = V_S$ = −10V to +10V
t_{ON}	Switch "ON" Time		500			500		ns	R_L = 1kΩ, V_{analog} = −10V to +10V See Fig. A
t_{OFF}	Switch "OFF" Time		250			250		ns	R_L = 1kΩ, V_{analog} = −10V to +10V See Fig. A
$Q_{(INJ.)}$	Charge Injection		15			20		mV	See Fig. B
OIRR	Min. Off Isolation Rejection Ratio		54			50		dB	f = 1 MHz, R_L = 100Ω, $C_L \leq$ 5pF See Fig. C (Note 1)
I^+	+ Power Supply Quiescent Current	10	10	100	10	10	100	µA	
I^-	− Power Supply Quiescent Current	10	10	100	10	10	100	µA	V^+ = +15 V, V^- = −15 V, V_L = +5 V with GND
I_{VL}	+5V Supply Quiescent Current	10	10	100	10	10	100	µA	
I_{GND}	Gnd Supply Quiescent Current	10	10	100	10	10	100	µA	
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio		54			50		dB	One Channel Off; Any Other Channel Switches as per Fig. E (Note 1)

Note 1: Not tested in production.

TEST CIRCUITS

FIG. A

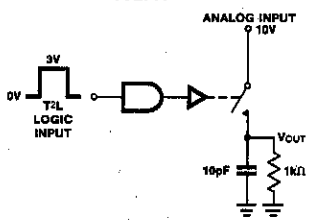


FIG. B

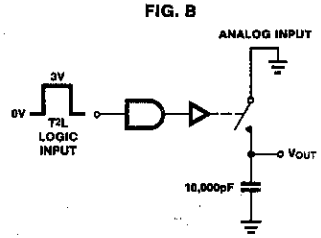
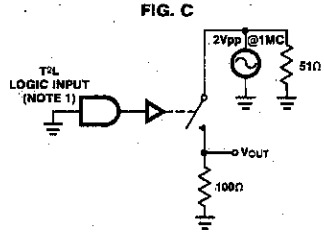


FIG. C



THEORY OF OPERATION

A. Floating Body CMOS Structure

In a conventional C-MOS structure, the body of the "n" channel device is tied to the negative supply, thus forming a reverse biased diode between the drain/source and the body (Fig. H). Under certain conditions this diode can become forward biased; for example, if the supplies are off (at ground) and a negative input is applied to the drain. This can have serious consequences for two reasons. Firstly, the diode has no current limiting and if excessive current flows, the circuit may be permanently damaged. Secondly, this diode forms part of a parasitic SCR in the conventional C-MOS structure. Forward biasing the diode causes the SCR to turn on, giving rise to a "latch-up" condition.

Intersil's improved C-MOS process incorporates an additional diode in series with the body (Fig. I). The cathode of this diode is then tied to V+, thus effectively floating the body. The inclusion of this diode not only blocks the excessive current path, but also prevents the SCR from turning on.

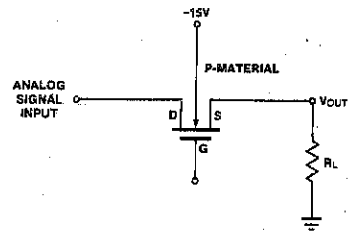


FIGURE H

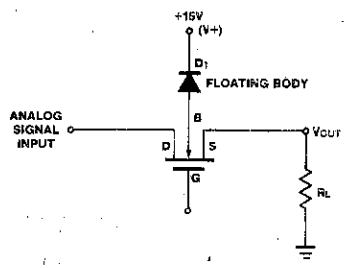


FIGURE I

B. Overvoltage Protection

The floating body construction inherently provides overvoltage protection. In the conventional C-MOS process, the body of all N-channel FETs is tied to the most negative power supply and the body of all P-channel devices to the most positive supply (i.e., ±15V). Thus, for an overvoltage spike of > ±15V, a forward bias condition exists between drain and body of the MOSFET. For example, in Fig. H if the analog signal input is more negative than −15V, the drain to body of the N-channel FET is forward biased and destruction of the device can result. Now by floating the body, using diode D1, the drain to body of the MOSFET is still forward biased, but D1 is reversed biased so no current flows (up to the breakdown of D1 which is ≥ 40V). Thus, negative excursions of the analog signal can go up to a maximum of −25V. When the signal goes positive (≥ +15V, D1 is forward biased, but now the drain to body junction is reversed for the N-channel FET; this allows the signal to go to a maximum of +25V with no appreciable current flow. While the explanation above has been restricted to N-channel devices, the same applies to P-channel FETs and the construction is as shown in Fig. J. Fig. J describes an output stage showing the paralleling of an N and P-channel to linearize the $r_{DS(on)}$ with signal input. The presence of diodes D1 and D2 effectively floats the bodies and provides overvoltage protection to a maximum of ±25V.

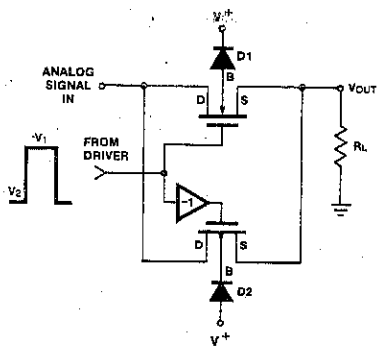
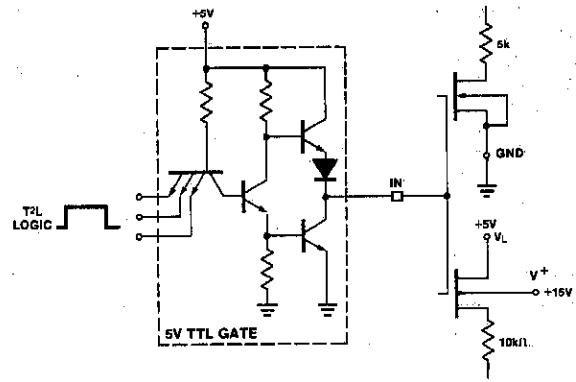
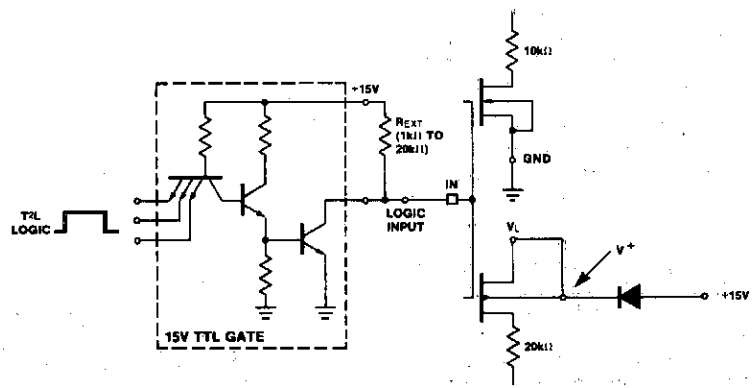


FIGURE J

LOGIC INTERFACING

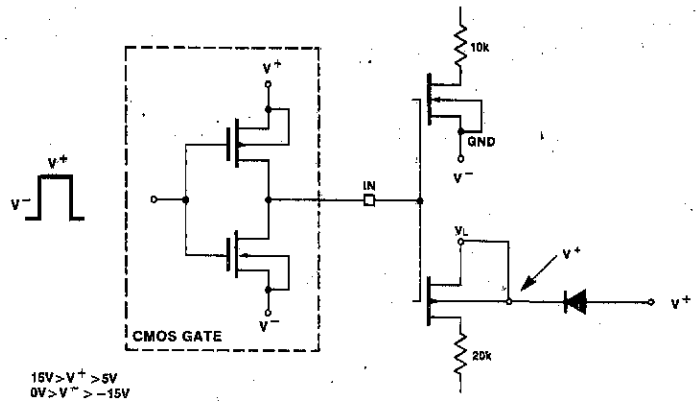


FOR INTERFACING WITH T²L OPEN COLLECTOR LOGIC.



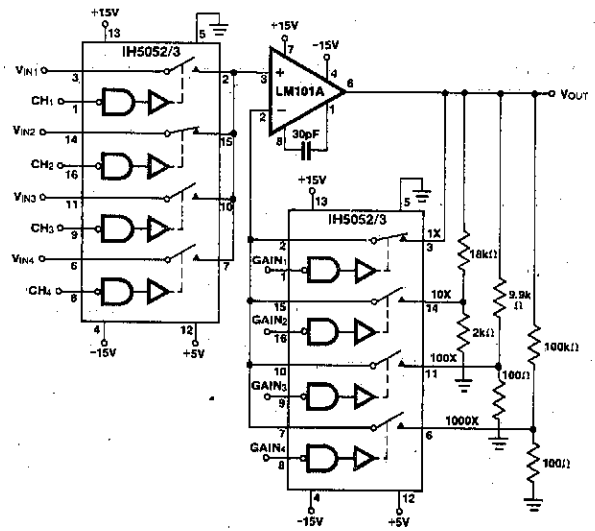
TYP. EXAMPLE FOR +15V CASE SHOWN

FOR USE WITH CMOS LOGIC.



APPLICATIONS

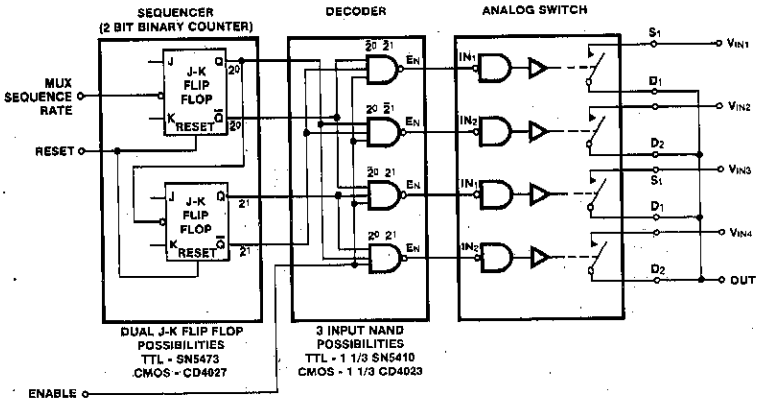
PROGRAMMABLE GAIN NON-INVERTING AMPLIFIER WITH SELECTABLE INPUTS



ACTIVE LOW PASS FILTER WITH DIGITALLY SELECTED BREAK FREQUENCY

APPLICATIONS (Continued)

4-CHANNEL SEQUENCING MUX

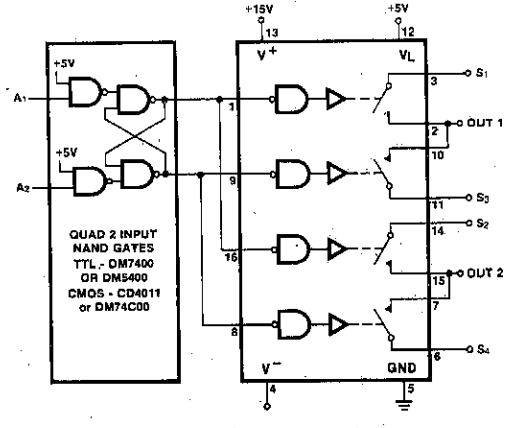


Truth Table (IH5052)

ENABLE	MUX SEQUENCE RATE	SEQUENCER OUTPUT		SWITCH STATES (– DENOTES OFF)			
		2^0	2^1	SW1	SW2	SW3	SW4
0	0	0	0	—	—	—	—
1	0	0	0	ON	—	—	—
1	1 pulse	1	0	—	ON	—	—
1	2 pulses	0	1	—	—	—	—
1	3 pulses	1	1	—	—	—	ON
1	4 pulses	0	0	ON	—	—	—

A Latching DPDT

The latch feature insures positive switching action in response to non-repetitive or erratic commands. The A_1 and A_2 inputs are normally low. A HIGH input to A_2 turns S_1 and S_2 ON, a HIGH to A_1 turns S_3 and S_4 ON. Desirable for use with limit detectors, peak detectors, or mechanical contact closures.



Truth Table (IH5052)

COMMAND		STATE OF SWITCHES AFTER COMMAND	
A_2	A_1	S_3 & S_4	S_1 & S_2
0	0	same	same
0	1	on	off
1	0	off	on
1	1	INDETERMINATE	

IH5108

8-Channel Fault Protected CMOS Analog Multiplexer

FEATURES

- **Ultra low leakage—$I_{D(off)} \leq 100pA$**
- **Power supply quiescent current less than 1mA**
- **±13V analog signal range**
- **No SCR latchup**
- **Break-before-make switching**
- **Pin compatible with DG508, HI508 and AD7508**
- **All channels OFF ($I_{ILK} \leq 100nA$) when power OFF, for analog signals up to ±25V**
- **Any channel turns OFF ($I_{ILK} \leq 100nA$) if input exceeds supply rails by up to ±25V. Throughput, always < ±14V (±15V supplies)**
- **TTL and CMOS compatible binary Address and ENable inputs**

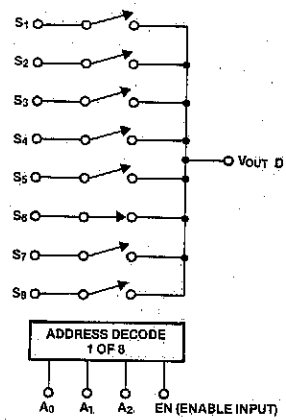
GENERAL DESCRIPTION

The IH5108 is a dielectrically isolated CMOS monolithic analog multiplexer, designed as a plug-in replacement for the DG508 and similar devices, but adding fault protection to the standard performance. A unique serial MOSFET switch ensures that an OFF channel will remain OFF when the input exceeds the supply rails by up to ±25V, even with the supply voltage at zero. Further, an ON channel will be limited to a throughput of about 1.5V less than the supply rails, thus affording protection to any following circuitry such as op amps, D/A converters, etc. Cross talk onto "good" channels is also prevented.

A binary 3-bit address code together with the ENable input allows selection of any one channel or none at all. These 4 inputs are all TTL compatible for easy logic interface; the ENable input also facilitates MUX expansion and cascading.

3

FUNCTIONAL DIAGRAM



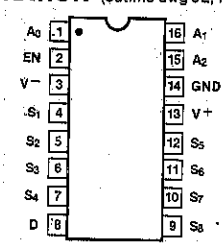
3 LINE BINARY ADDRESS INPUTS
(1 0 1) AND EN HI
ABOVE EXAMPLE SHOWS CHANNEL 6 TURNED ON

DECODE TRUTH TABLE

A_2	A_1	A_0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

A_0, A_1, A_2, EN
Logic "1" = $V_{AH} \geq 2.4V$
Logic "0" = $V_{AL} \leq 0.8V$

PIN CONFIGURATION (outline dwg JE, PE)



TOP VIEW

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH5108MJE	−55°C to +125°C	16 pin CERDIP
IH5108IJE	−20°C to +85°C	16 pin CERDIP
IH5108CPE	0°C to 70°C	16 pin plastic DIP

IH5108

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground ..... −15V to 15V
V_S or V_D to V^+ ..... +25V, −40V
V_S or V_D to V^- ..... −25V, +40V
V^+ to Ground 16V
V^- to Ground ..... −16V
Current (Any Terminal) 20mA

Operating Temperature ..... −55 to 125°C
Storage Temperature ..... −65 to 150°C
Power Dissipaton (Package)* 1200mW

*All leads soldered or welded to PC board. Derate 10mW/°C above 70°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS $V^+ = 15V$, $V^- = -15V$, $V_{EN} = 2.4V$, unless otherwise specified.

3

	CHARACTERISTIC		MEASURED TERMINAL	NO TESTS PER TEMP	TYP 25°C	MAX LIMITS M SUFFIX −55°C	M SUFFIX 25°C	M SUFFIX 125°C	I/C SUFFIX −20°C/ 0°C	I/C SUFFIX 25°C	I/C SUFFIX 85°C/ 70°C	UNIT	TEST CONDITIONS	
SWITCH	$r_{DS(on)}$		S to D	8	700	900	900	1200	1200	1200	1800	Ω	$V_D = 10V$, $I_S = -1.0mA$	Sequence each switch on
				8	500	900	900	1200	1200	1200	1800		$V_D = -10V$ $I_S = -1.0mA$	$V_{AL} = 0.8V$, $V_{AH} = 2.4V$
	$\Delta r_{DS(on)}$				5		10			10		%	$\Delta r_{DS(on)} = \frac{r_{DS(on)max} - r_{DS(on)min}}{r_{DS(on)avg.}}$ $V_S = \pm 10V$	
	$I_{S(off)}$		S	8	0.002		0.05	50		0.1	50	nA	$V_S = 10V$, $V_D = -10V$	$V_{EN} = 0$
				8	0.002		0.05	50		0.1	50		$V_S = -10V$, $V_D = 10V$	
	$I_{D(off)}$		D	1	0.03		0.1	100		0.2	100		$V_D = 10V$, $V_S = -10V$	
				1	0.03		0.1	100		0.2	100		$V_D = -10V$, $V_S = 10V$	
	$I_{D(on)}$		D	8	0.1		0.2	100		0.4	100		$V_{S(All)} = V_D = 10V$	Sequence each switch on
				8	0.1		0.2	100		0.4	100		$V_{S(All)} = V_D = -10V$	$V_{AL} = 0.8V$, $V_{AH} = 2.4V$
FAULT	I_S with Power OFF		S	8	1		100	1000	50	50	5000	nA	$V^+ = V^- = 0V$, $V_S = \pm 25V$, $V_{EN} = V_O = 0V$, A_0, A_1, $A_2 = 0V$ or 5V	
	$I_{S(off)}$ with Overvoltage (Note 1)		S	8	1		2000	5000		5000	5000		$V_S = \pm 25V$, $V_D = \mp 10V$	Sequence each switch
IN	$I_{EN(on)}$ $I_{A(on)}$ or $I_{EN(off)}$ $I_{A(off)}$		A_0, A_1, EN	4	.01		−10	−30		−10	−30	μA	$V_A = 2.4V$ or 0V	
				4	.01		10	30		10	30		$V_A = 15V$ or 0V	
DYNAMIC	$t_{transition}$		D		0.3		1					μs	See Figure 1	
	t_{open}		D		0.2								See Figure 2	
	$t_{on(EN)}$		D		0.6		1.5						See Figure 3	
	$t_{off(EN)}$		D		0.4		1							
	t_{on}−t_{off} Break-Before-Make Delay Settling Time		D	8	50		25			10		ns	$V_{EN} = +5V$, A_0, A_1, A_2 Strobed $V_{IN} = \pm 10V$, Figure 4	
	"OFF" Isolation		D		60							dB	$V_{EN} = 0$, $R_L = 200\Omega$, $C_L = 3pF$, $V_S = 3$ VRMS, f = 500 KHz	
	$C_{S(off)}$		S		5							pF	$V_S = 0$	$V_{EN} = 0V$, f = 140 KHz to 1 MHz
	$C_{D(off)}$		D		25								$V_D = 0$	
	$C_{DS(off)}$		D to S		1								$V_S = 0$, $V_D = 0$	
SUP	Supply Current	+	V^+	1	500	900	750	600		1000		μA	All V_A, $V_{EN} = 0$ or 5V	
		−	V^-	1	500	900	750	600		1000				

Note 1. Readings taken 400ms after the overvoltage occurs.

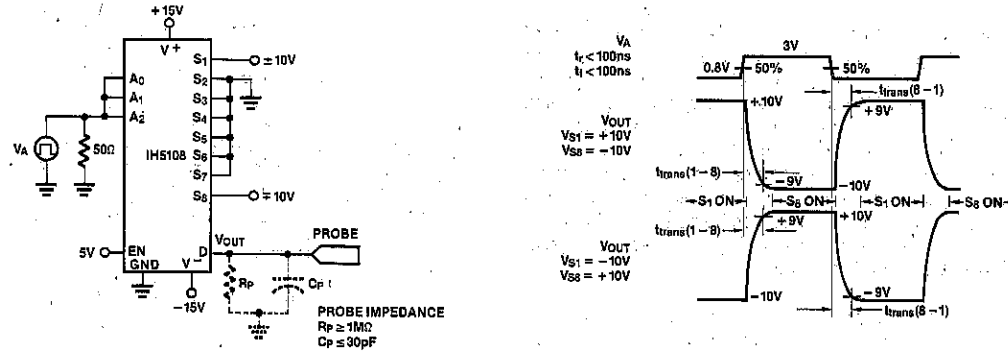


Figure 1. $t_{transition}$ Switching Test

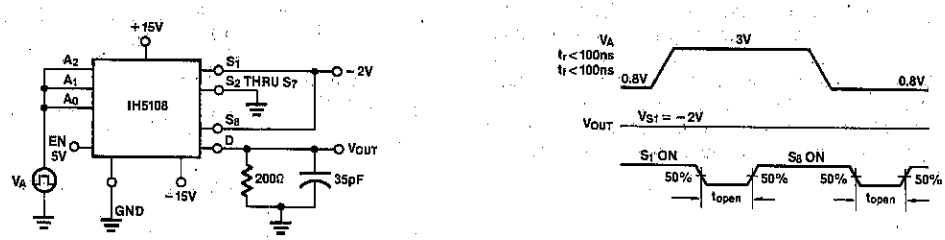


Figure 2. t_{open} (Break-Before-Make) Switching Test

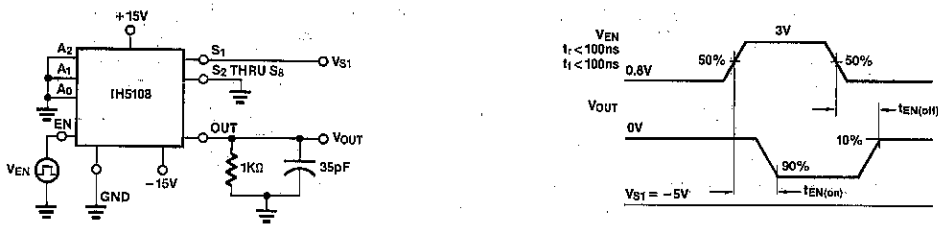


Figure 3. t_{on} and t_{off} Switching Test

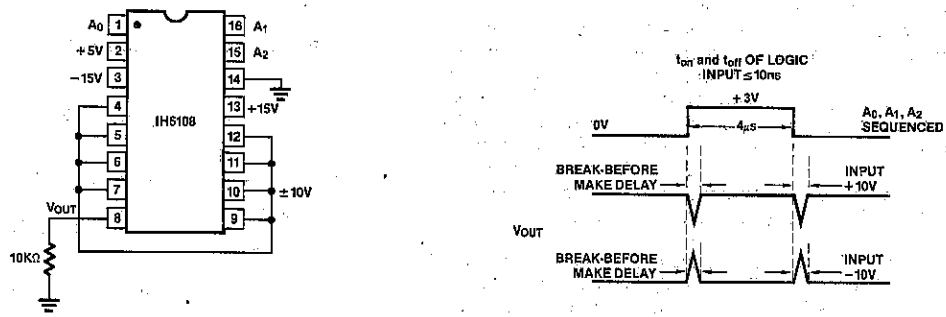


Figure 4. Break-Before-Make Delay Test

DETAILED DESCRIPTION

The IH5108, like all Intersil's multiplexers, contains a set of CMOS switches forming the channels, and driver and decoder circuitry to control which channel turns ON, if any. In addition, the IH5108 contains an internal regulator which provides a fully TTL compatible ENable input that is identical in operation to the Address inputs. This does away with the special treatment that many multiplexer enable inputs require for proper logic swings. This identical circuit treatment of the ENable and Address lines also helps ensure the extension of break-before-make switching to wider multiplexer systems (see applications section).

Another, and more important, difference lies in the switching channel. Previous devices have used parallel n- and p-channel MOSFET switches, and while this scheme yields reasonably good ON resistance characteristics and allows the switching of rail-to-rail input signals, it also has a number of drawbacks. The sources and drains of the switch transistors will conduct to the substrate if the input goes outside the supply rails, and even careful use of diodes cannot avoid channel-to-output and channel-to-channel coupling in cases of input overrange. The IH5108 uses a novel series arrangement of the p- and n-channel switches (Figure 5) combined with a dielectrically isolated process to obviate these problems.

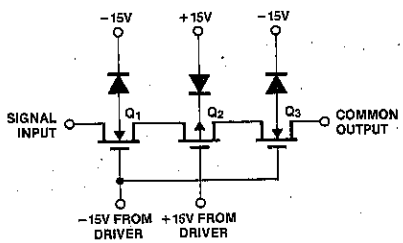
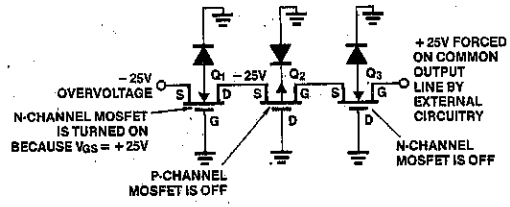


Figure 5. Series Connection of Channel Switches

Within the normal analog signal band, the inherent variation of switch ON resistance will balance out almost as well as the customary parallel configuration, but as the analog signal approaches either supply rail, even for an ON channel, either the p- or the n-channel will become a source follower, disconnecting the channel (Figure 6). Thus protection is provided to any input or output channel against overvoltage on any (or several) input or output channels even in the absence of multiplexer supply voltages, and applies up to the breakdown voltage of the respective switches, drawing only leakage currents. Figure 7 shows a more detailed schematic of the channel switches, including the back-gate driver devices which ensure optimum channel ON resistances and breakdown voltage under the various conditions.

Under some circumstances, if the logic inputs are present but the multiplexer supplies are not, the circuit will use the logic inputs as a sort of phantom supply; this could result in an output up to that logic level. To prevent this from occurring, simply ensure that the ENable pin is LOW any time the multiplexer supply voltages are missing (Figure 8).

(a) OVERVOLTAGE WITH MUX POWER OFF



(b) OVERVOLTAGE WITH MUX POWER ON

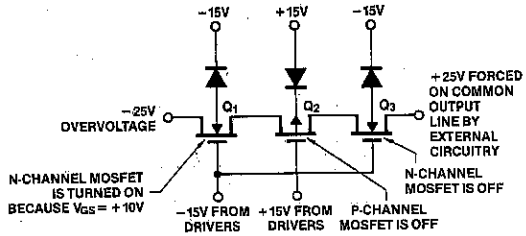


Figure 6. Overvoltage Protection

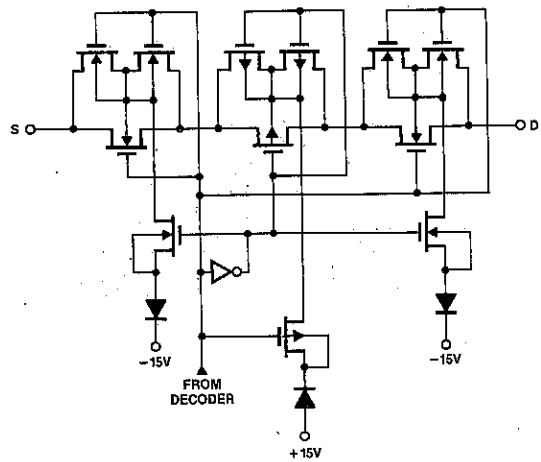


Figure 7. Detailed Channel Switch Schematic

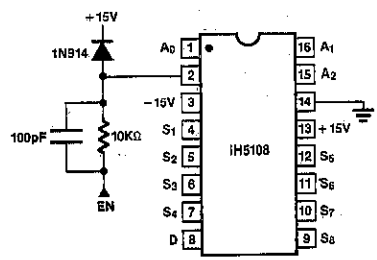


Figure 8. Protection Against Logic Input

MAXIMUM SIGNAL HANDLING CAPABILITY

The IH5108 is designed to handle signals in the ±10V range, with a typical $r_{DS(on)}$ of 600Ω; it can successfully handle signals up to ±13V, however, $r_{DS(on)}$ will increase to about 1.8K. Beyond ±13V the device approaches an open circuit, and thus ±12V is about the practical limit, see Figure 9.

Figure 10 shows the input/output characteristics of an ON channel, illustrating the inherent limiting action of the series switch connection (see Detailed Description), while Figure 11 gives the ON resistance variation with temperature.

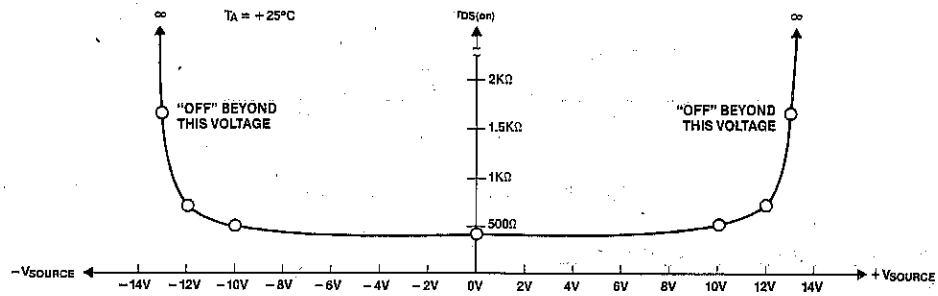


Figure 9. $r_{DS(on)}$ vs Signal Output Voltage @ T_A = +25°C

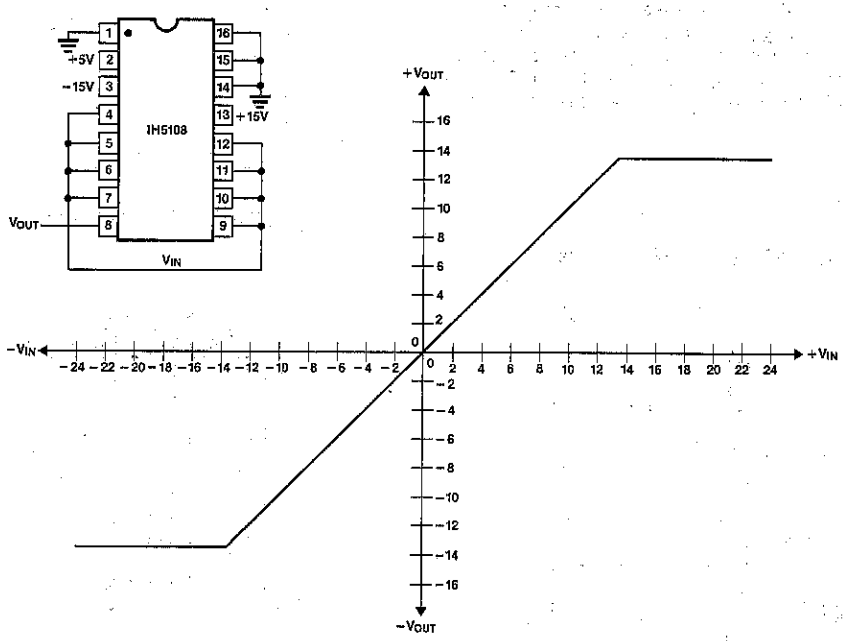


Figure 10. MUX Output Voltage vs Input Voltage
Channel 1 Shown; All Channels Similar

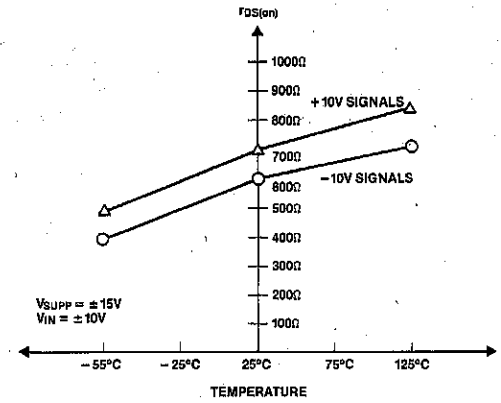


Figure 11. Typical $r_{DS(on)}$ vs Temperature

3

USING THE IH5108 WITH SUPPLIES OTHER THAN ±15V

The IH5108 will operate successfully with supply voltages from ±5V to ±15V; $r_{DS(on)}$ increases as supply voltage decreases, see Figure 12. Leakage currents, however, decrease with a lowering of supply voltage, and therefore the error term product of $r_{DS(on)}$ and leakage current remains reasonably constant. $r_{DS(on)}$ also decreases as signal levels decrease. For high system accuracy [acceptable levels of $r_{DS(on)}$] the maximum input signal should be 3V less than the supply voltages. The logic levels will remain TTL compatible.

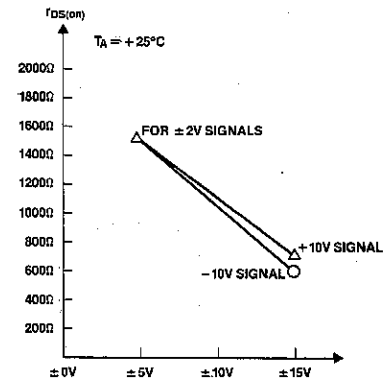
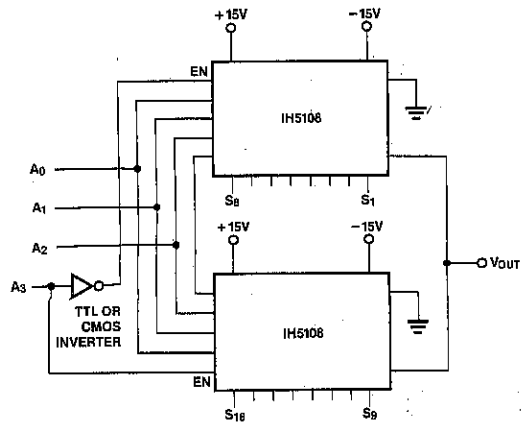


Figure 12. $r_{DS(on)}$ vs Supply Voltages

IH5108 APPLICATIONS INFORMATION

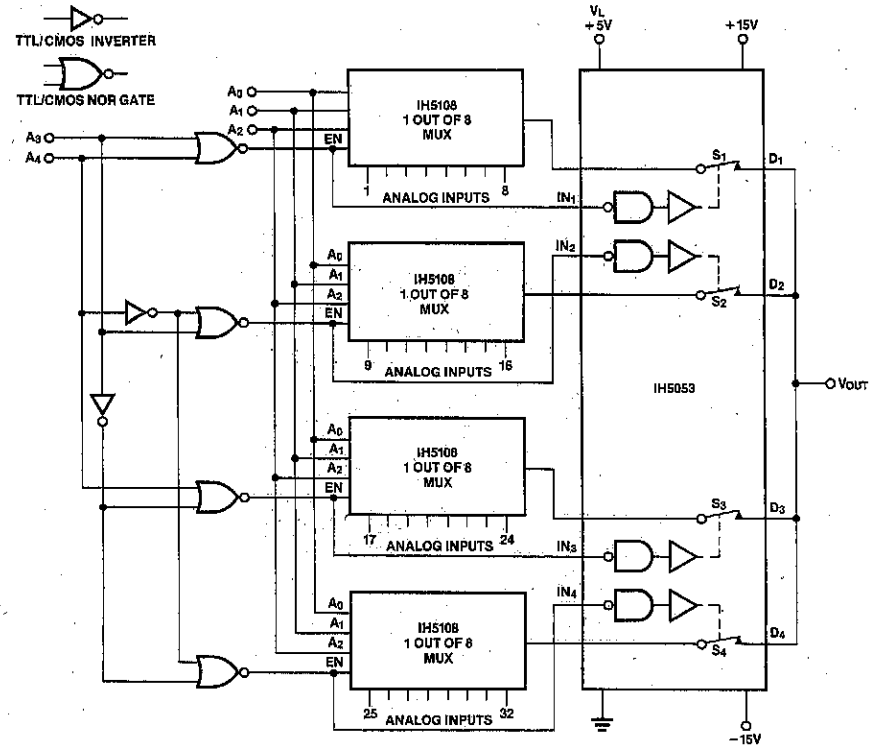


DECODE TRUTH TABLE

A_3	A_2	A_1	A_0	ON SWITCH
0	0	0	0	S1
0	0	0	1	S2
0	0	1	0	S3
0	0	1	1	S4
0	1	0	0	S5
0	1	0	1	S6
0	1	1	0	S7
0	1	1	1	S8
1	0	0	0	S9
1	0	0	1	S10
1	0	1	0	S11
1	0	1	1	S12
1	1	0	0	S13
1	1	0	1	S14
1	1	1	0	S15
1	1	1	1	S16

Figure 13. 1 of 16 channel multiplexer using two IH5108s. Overvoltage protection is maintained between all channels, as is break-before-make switching.

IH5108 APPLICATIONS INFORMATION (Continued)



DECODE TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	ON SWITCH
0	0	0	0	0	S1
0	0	0	0	1	S2
0	0	0	1	0	S3
0	0	0	1	1	S4
0	0	1	0	0	S5
0	0	1	0	1	S6
0	0	1	1	0	S7
0	0	1	1	1	S8
0	1	0	0	0	S9
0	1	0	0	1	S10
0	1	0	1	0	S11
0	1	0	1	1	S12
0	1	1	0	0	S13
0	1	1	0	1	S14
0	1	1	1	0	S15
0	1	1	1	1	S16

DECODE TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	ON SWITCH
1	0	0	0	0	S17
1	0	0	0	1	S18
1	0	0	1	0	S19
1	0	0	1	1	S20
1	0	1	0	0	S21
1	0	1	0	1	S22
1	0	1	1	0	S23
1	0	1	1	1	S24
1	1	0	0	0	S25
1	1	0	0	1	S26
1	1	0	1	0	S27
1	1	0	1	1	S28
1	1	1	0	0	S29
1	1	1	0	1	S30
1	1	1	1	0	S31
1	1	1	1	1	S32

Figure 14. 1 of 32 multiplexer using 4 IH5108s and an IH5053 as a submultiplexer. Note that the IH5053 is protected against overvoltages by the IH5108s. Submultiplexing reduces output leakage and capacitance.

APPLICATION NOTES

Further information may be found in:

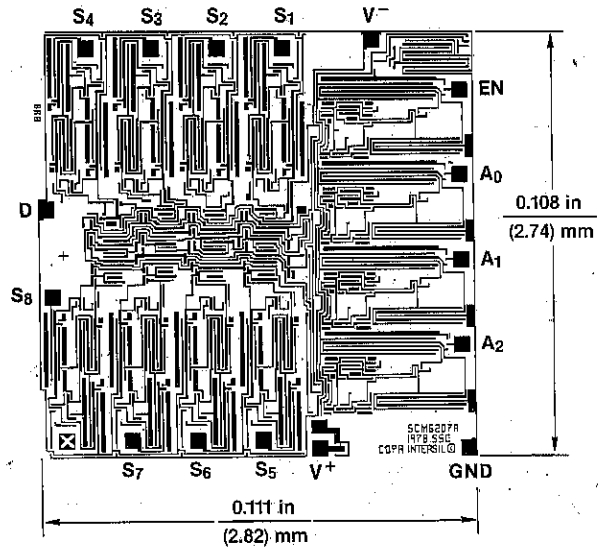
A003 "Understanding and Applying the Analog Switch," by Dave Fullagar

A006 "A New CMOS Analog Gate Technology," by Dave Fullagar

A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing," by Ed Slieger

R009 "Reduce CMOS Multiplexer Troubles Through Proper Device Selection," by Dick Wilenken

CHIP TOPOGRAPHY



IH5140 Family High Level CMOS Analog Gates

FEATURES

- **Super fast break before make switching t_{on} 80ns typ, t_{off} 50ns typ (SPST switches)**
- **Power supply currents less than 1μA**
- **OFF leakages less than 100pA @ 25°C guaranteed**
- **Non-latching with supply turn-off**
- **Single monolithic CMOS chip**
- **Plug-in replacements for IH5040 family and part of the DG180 family to upgrade speed and leakage**
- **Greater than 1MHz toggle rate**
- **Switches greater than 20Vp-p signals with ±15V supplies**
- **T^2L, CMOS direct compatibility**

GENERAL DESCRIPTION

The IH5140 Family of CMOS monolithic switches utilizes Intersil's latch-free junction isolated processing to build the fastest switches now available. These switches can be toggled at a rate of greater than 1 MHz with super fast t_{on} times (80ns typical) and faster t_{off} times (50ns typical), guaranteeing break before make switching. This family of switches therefore combines the speed of the hybrid FET DG 180 Family with the reliability and low power consumption of a monolithic CMOS construction.

OFF leakages are guaranteed to be less than 100pA at 25°C. No quiescent power is dissipated in either the ON or the OFF state of the switch. Maximum power supply current is 1μA from any supply and typical quiescent currents are in the 10nA range which makes these devices ideal for portable equipment and military applications.

The IH5140 Family is completely compatible with TTL (5V) logic, TTL open collector logic and CMOS logic gates. It is pin compatible with Intersil's IH5040 Family and part of the DG180/190 Family as shown in the switching state diagrams.

3

ORDERING INFORMATION

Order Part Number	Function	Package	Temperature Range
IH5140 MJE	SPST	16 Pin CERDIP	-55°C to 125°C
IH5140 CJE	SPST	16 Pin CERDIP	0°C to 70°C
IH5140 CPE	SPST	16 Pin Plastic DIP	0°C to 70°C
IH5140 MFD	SPST	14 Pin Flat Pack	-55°C to 125°C
IH5141 MJE	Dual SPST	16 Pin CERDIP	-55°C to 125°C
IH5141 CJE	Dual SPST	16 Pin CERDIP	0°C to 70°C
IH5141 CPE	Dual SPST	16 Pin Plastic DIP	0°C to 70°C
IH5141 MFD	Dual SPST	14 Pin Flat Pack	-55°C to 125°C
IH5141 CTW	Dual SPST	TO-100	0°C to 70°C
IH5141 MTW	Dual SPST	TO-100	-55°C to 125°C
IH5142 MJE	SPDT	16 Pin CERDIP	-55°C to 125°C
IH5142 CJE	SPDT	16 Pin CERDIP	0°C to 70°C
IH5142 CPE	SPDT	16 Pin Plastic DIP	0°C to 70°C
IH5142 MFD	SPDT	14 Pin Flat Pack	-55°C to 125°C
IH5142 CTW	SPDT	TO-100	0°C to 70°C
IH5142 MTW	SPDT	TO-100	-55°C to 125°C
IH5143 MJE	Dual SPDT	16 Pin CERDIP	-55°C to 125°C
IH5143 CJE	Dual SPDT	16 Pin CERDIP	0°C to 70°C
IH5143 CPE	Dual SPDT	16 Pin Plastic DIP	0°C to 70°C
IH5143 MFD	Dual SPDT	14 Pin Flat Pack	-55°C to 125°C
IH5144 MJE	DPST	16 Pin CERDIP	-55°C to 125°C
IH5144 CJE	DPST	16 Pin CERDIP	0°C to 70°C
IH5144 CPE	DPST	16 Pin Plastic DIP	0°C to 70°C
IH5144 MFD	DPST	14 Pin Flat Pack	-55°C to 125°C
IH5144 CTW	DPST	TO-100	0°C to 70°C
IH5144 MTW	DPST	TO-100	-55°C to 125°C
IH5145 MJE	Dual DPST	16 Pin CERDIP	-55°C to 125°C
IH5145 CJE	Dual DPST	16 Pin CERDIP	0°C to 70°C
IH5145 CPE	Dual DPST	16 Pin Plastic DIP	0°C to 70°C
IH5145 MFD	Dual DPST	14 Pin Flat Pack	-55°C to 125°C

Note:
1. Ceramic (side braze) devices also available; consult factory.
2. MIL temp range parts also available with MIL-STD-883 processing.

FUNCTIONAL DIAGRAM

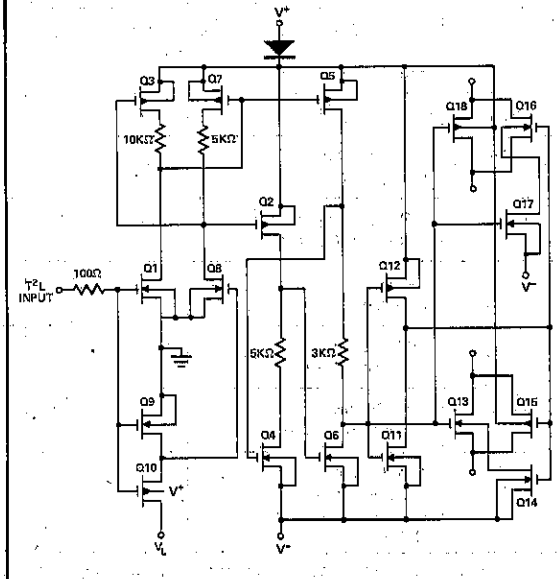


FIGURE 1. Typical Driver/Gate — IH5142

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Current (Any Terminal) ..... < 30 mA
Storage Temperature ..... -65°C to +150°C
Operating Temperature .... -55°C to +125°C
Power Dissipation ..... 450 mW
(All Leads Soldered to a P.C. Board)
Derate 6 mW/°C Above 70°C
Lead Temperature (Soldering 10 sec.) .. 300°C

$V^+ - V^-$	<33V
$V^+ - V_D$	<30V
$V_D - V^-$	<30V
$V_D - V_S$	<±22V
$V_L - V^-$	<33V
$V_L - V_{IN}$	<30V
V_L	<20V
V_{IN}	<20V

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (@ 25°C, V^+ = +15V, V^- = -15V, V_L = +5V)

PER CHANNEL		MIN./MAX. LIMITS							
		MILITARY			COMMERCIAL				
SYMBOL	CHARACTERISTIC	-55°C	+25°C	+125°C	0	+25°C	+70°C	UNITS	TEST CONDITIONS
I_{INH}	Input Logic Current	1	1	1	1	1	1	µA	V_{IN} = 2.4 V Note 1
I_{INL}	Input Logic Current	1	1	1	1	1	1	µA	V_{IN} = 0.8 V Note 1
$r_{DS(on)}$	Drain—Source On Resistance	50	50	75	75	75	100	Ω	I_S = -10 mA V_{ANALOG} = -10 V to +10 V
$\Delta r_{DS(on)}$	Channel to Channel $r_{DS(on)}$ Match		25 (typ)			30 (typ)		Ω	
V_{ANALOG}	Min. Analog Signal Handling Capability		±11			±10		V	
$I_{D(off)}$+	Switch OFF Leakage	0.1	0.1	20	0.5	0.5	20	nA	V_D = +10 V, V_S = -10 V
$I_{S(off)}$	Current	0.1	0.1	20	0.5	0.5	20		V_D = -10V, V_S = +10 V
$I_{D(on)}$+ $I_{S(on)}$	Switch On Leakage Current	0.2	0.2	40	1	1	40	nA	V_D = V_S = -10 V to +10 V
t_{on} t_{off}	Switch "ON" Time Switch "OFF" Time	See switching time specifications and timing diagrams.							
$Q_{(INJ.)}$	Charge Injection		100			150		pC	See Fig. 4, Note 2
OIRR	Min. Off Isolation Rejection Ratio		54			50		dB	f = 1 MHz, R_L = 100Ω, C_L ≤ 5 pF See Fig. 5, Note 2
I^+	+ Power Supply Quiescent Current	1.0	1.0	10.0	10	10	100	µA	
I^-	- Power Supply Quiescent Current	1.0	1.0	10.0	10	10	100	µA	V^+ = +15 V, V^- = -15 V, V_L = +5 V
I_L	+5 V Supply Quiescent Current	1.0	1.0	10.0	10	10	100	µA	See Fig. 6
I_{GND}	Gnd Supply Quiescent Current	1.0	1.0	10.0	10	10	100	µA	
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio		54			50		dB	One Channel Off; Any Other Channel Switches See Fig. 7, Note 2

Note: 1. Some channels are turned on by high (1) logic inputs and other channels are turned on by low (0) inputs; however 0.8V to 2.4V describes the min. range for switching properly. Refer to logic diagrams to find logical value of logic input required to produce ON or OFF state.

2. Charge injection, OFF isolation, and Channel to Channel isolation are only sample tested in production.

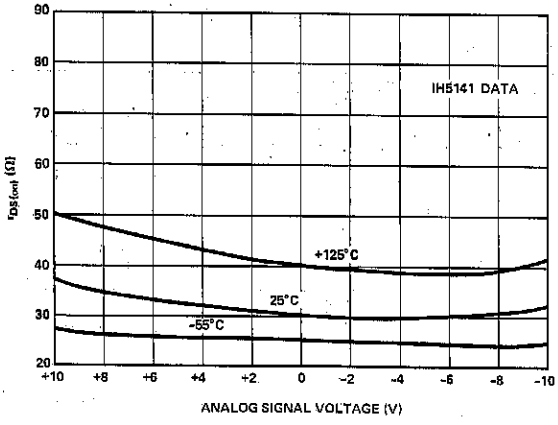


FIGURE 2. $r_{DS(on)}$ vs. Temp., @ ±15V, +5V Supplies.

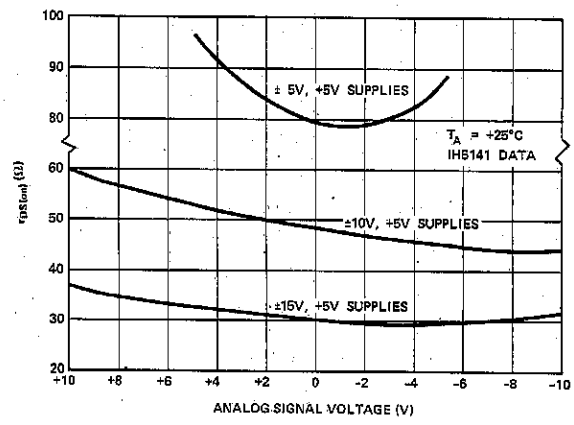


FIGURE 3. $r_{DS(on)}$ vs. Power Supplies.

3

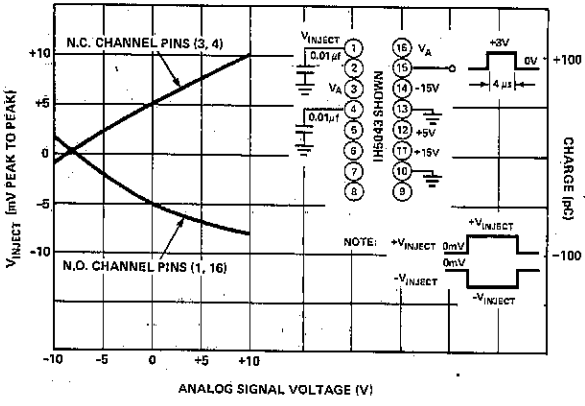


FIGURE 4. Charge Injection vs. Analog Signal.

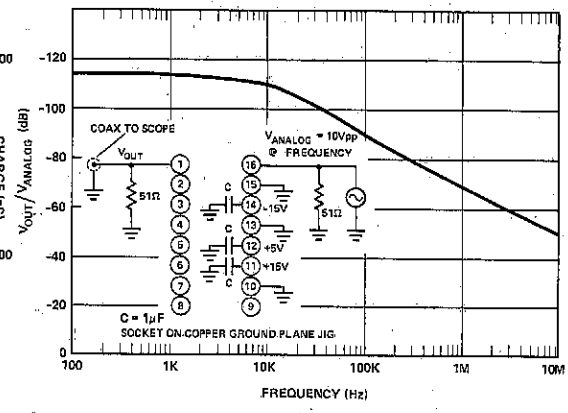


FIGURE 5. "OFF" Isolation vs. Frequency.

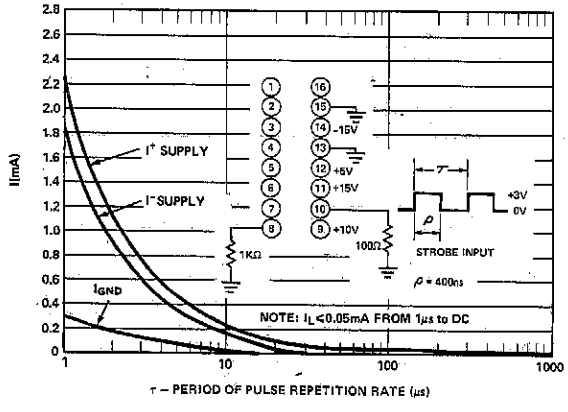


FIGURE 6. Power Supply Currents vs. Logic Strobe Rate.

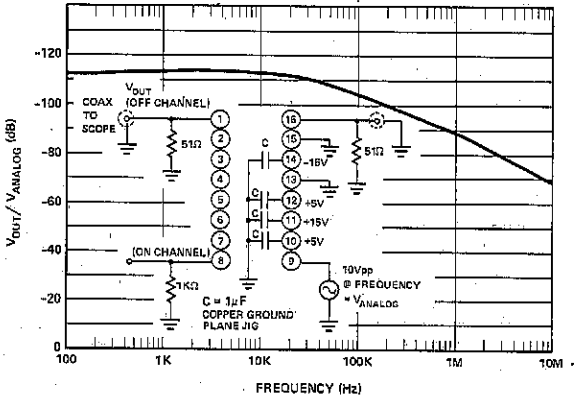


FIGURE 7. Channel to Channel Cross Coupling Rejection vs. Frequency.

SWITCHING TIME SPECIFICATIONS

(t_{on}, t_{off} are maximum specifications and t_{on}-t_{off} is minimum specifications)

Part Number	Symbol	Characteristics	MILITARY -55°C	MILITARY +25°C	MILITARY +125°C	COMMERCIAL 0°C	COMMERCIAL +25°C	COMMERCIAL +70°C	Units	Test Conditions
IH5140-5141	t_{on}	Switch "ON" time		100			150		ns	Figure 8
	t_{off}	Switch "OFF" time		75			125			
	t_{on}-t_{off}	Break-before-make		10			5			
	t_{on}	Switch "ON" time		150			175		ns	Figure 9
	t_{off}	Switch "OFF" time		125			150			
	t_{on}-t_{off}	Break-before-make		10			5			
IH5142-5143	t_{on}	Switch "ON" time		175			250		ns	Figure 8
	t_{off}	Switch "OFF" time		125			150			
	t_{on}-t_{off}	Break-before-make		10			5			
	t_{on}	Switch "ON" time		200			300		ns	Figure 9
	t_{off}	Switch "OFF" time		125			150			
	t_{on}-t_{off}	Break-before-make		10			5			
	t_{on}	Switch "ON" time		175			250		ns	Figure 10
	t_{off}	Switch "OFF" time		125			150			
	t_{on}-t_{off}	Break-before-make		10			5			
	t_{on}	Switch "ON" time		200			300		ns	Figure 11
	t_{off}	Switch "OFF" time		125			150			
	t_{on}-t_{off}	Break-before-make		10			5			
IH5144-5145	t_{on}	Switch "ON" time		175			250		ns	Figure 8
	t_{off}	Switch "OFF" time		125			150			
	t_{on}-t_{off}	Break-before-make		10			5			
	t_{on}	Switch "ON" time		200			300		ns	Figure 9
	t_{off}	Switch "OFF" time		125			150			
	t_{on}-t_{off}	Break-before-make		10			5			

3

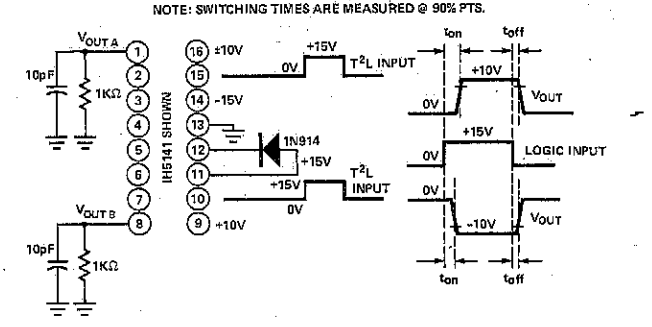


FIGURE 8.

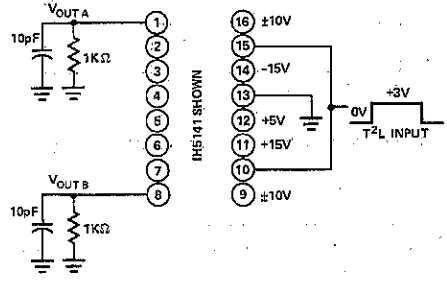


FIGURE 9.

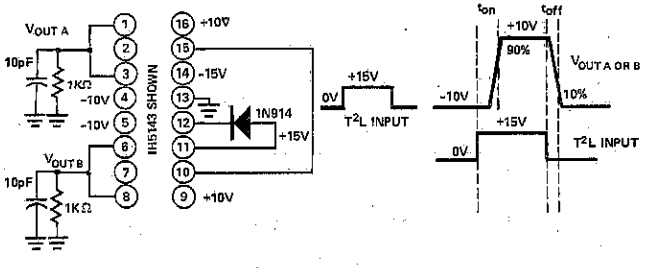


FIGURE 10.

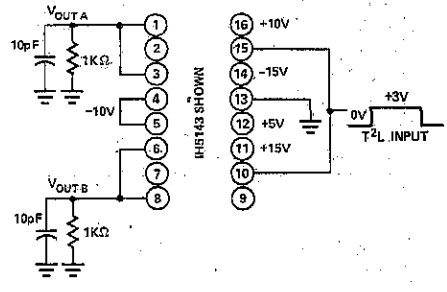
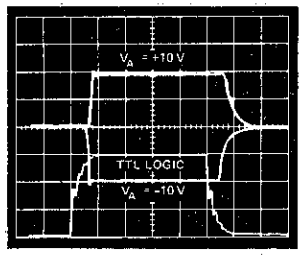


FIGURE 11.

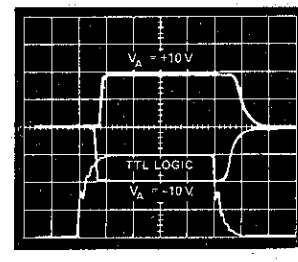
TYPICAL SWITCHING WAVEFORMS

SCALE: VERT. = 5V/DIV.
HORIZ. = 100ns/DIV.

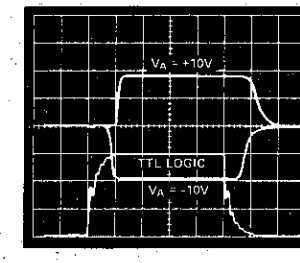
TTL OPEN COLLECTOR LOGIC DRIVE (Corresponds to Figure 8)



-55°C



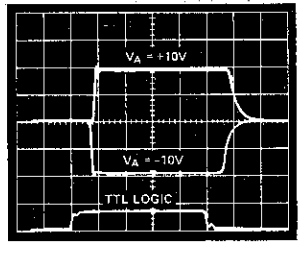
+25°C



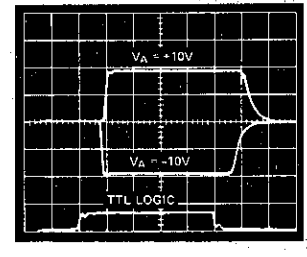
+125°C

3

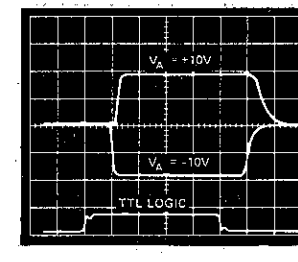
TTL OPEN COLLECTOR LOGIC DRIVE (Corresponds to Figure 9)



-55°C

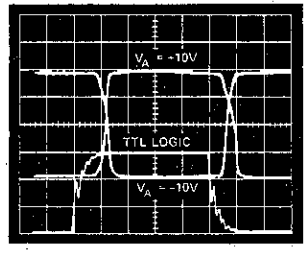


+25°C



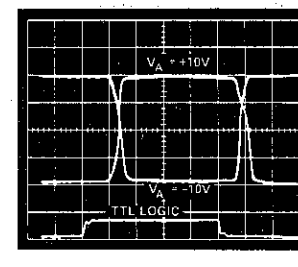
+125°C

TTL OPEN COLLECTOR LOGIC DRIVE
(Corresponds to Figure 10)



+25°C

TTL OPEN COLLECTOR LOGIC DRIVE
(Corresponds to Figure 11)



+25°C

APPLICATION NOTE

To maximize switching speed on the IH5140 family use TTL open collector logic (15V with a 1kΩ or less collector resistor). This configuration will result in (SPST) t_{on} and t_{off} times of 80ns and 50ns, for signals between -10V and +10V. The SPDT and DPST switches are approximately 30ns slower in both t_{on} and t_{off} with the same drive configuration. 15V CMOS logic levels can be used (0V to +15V), but propagation delays in the CMOS logic will slow down the switching (typical 50ns – 100ns delays).

When driving the IH5140 Family from either +5V TTL or CMOS logic, switching times run 20ns slower than if they were driven from +15V logic levels. Thus t_{on} is about 105ns, and t_{off} 75ns for SPST switches, and 135ns and 105ns (t_{on}, t_{off}) for SPDT or DPST switches. The low level drive can be made as fast as the high level drive if ±5V strobe levels are used instead of the usual 0V→+3.0V drive. Pin 13 is taken to -5V instead of the usual GND and strobe input is taken from +5V to -5V levels as shown in Figure 12.

The typical channel of the IH5140 family consists of both P and N-channel MOS-FETs. The N-channel MOS-FET uses a "Body Puller" FET to drive the body to -15V(±15V supplies) to get good breakdown voltages when the switch is in the off state (See Fig. 13). This "Body Puller" FET also allows the N-channel body to electrically float when the switch is in the on state producing a fairly constant $R_{DS}(ON)$ with different signal voltages. While this "Body Puller" FET improves switch performance, it can cause a problem when analog input signals are present (negative signals only) and power supplies are off. This fault condition is shown in Figure 14.

Current will flow from -10V analog voltage through the drain to body junction of Q1, then through the drain to body junction of Q3 to GND. This means that there is 10V across two forward-biased silicon diodes and current will go to whatever value the input signal source is capable of supplying. If the analog input signal is derived from the same supplies as the switch this fault condition cannot occur. Turning off the supplies would turn off the analog signal at the same time.

This fault situation can also be eliminated by placing a diode in series with the negative supply line (pin 14) as shown in Figure 15. Now when the power supplies are off and a negative input signal is present this diode is reverse biased and no current can flow.

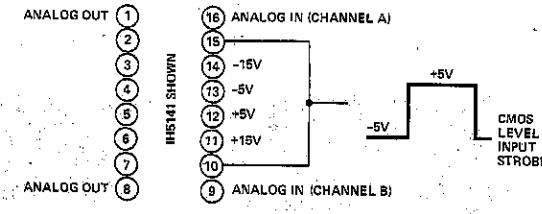


FIGURE 12.

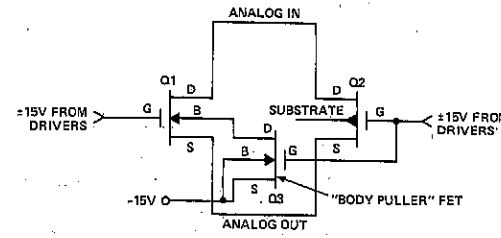


FIGURE 13.

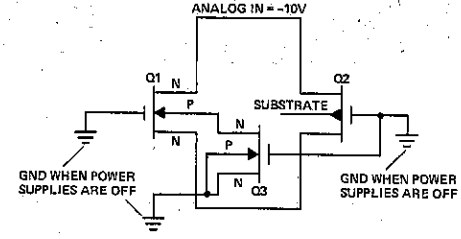


FIGURE 14.

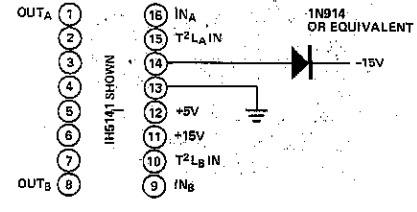


FIGURE 15.

APPLICATIONS

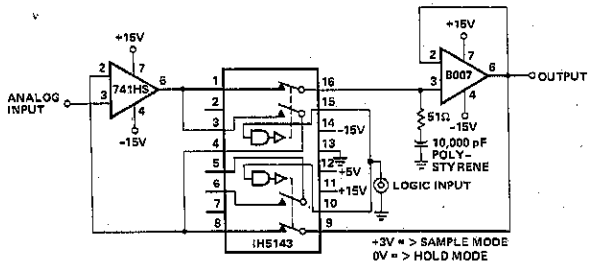
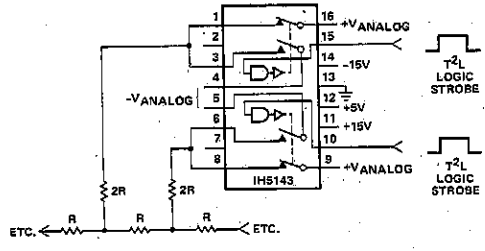


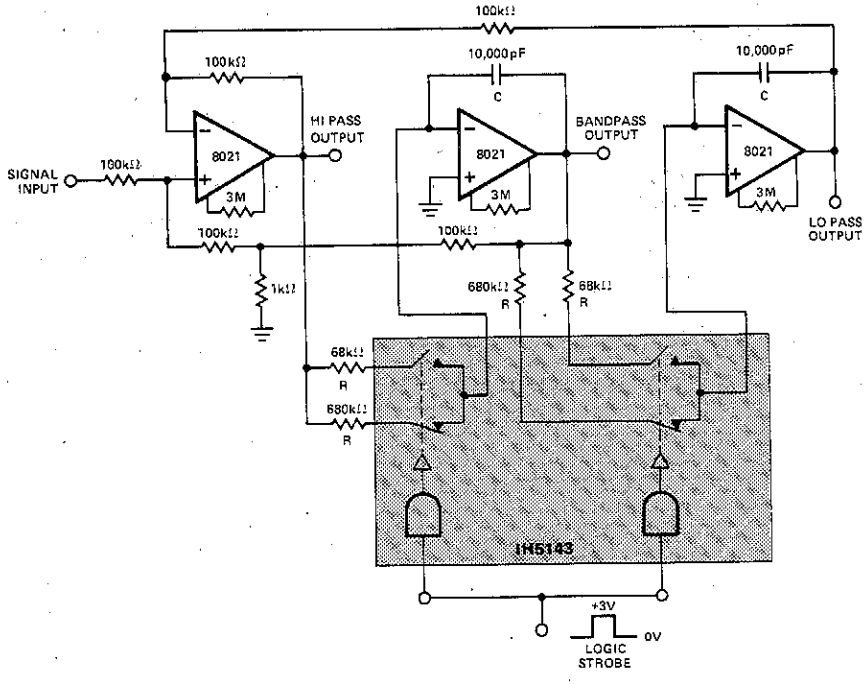
FIGURE 16. Improved Sample and Hold Using IH5143



EXAMPLE: If $-V_{ANALOG} = -10VDC$ and $+V_{ANALOG} = +10VDC$ then Ladder Legs are switched between ±10VDC, depending upon state of Logic Strobe.

FIGURE 17. Using the CMOS Switch to Drive an R/2R Ladder Network (2 Legs)

3



CONSTANT GAIN, CONSTANT Q, VARIABLE FREQUENCY FILTER WHICH PROVIDES SIMULTANEOUS LOWPASS, BANDPASS, AND HIGHPASS OUTPUTS. WITH THE COMPONENT VALUES SHOWN, CENTER FREQUENCY WILL BE 235Hz AND 23.5Hz FOR HIGH AND LOW LOGIC INPUTS RESPECTIVELY, Q = 100, AND GAIN = 100.

$$f_n = \text{CENTER FREQUENCY} = \frac{1}{2\pi RC}$$

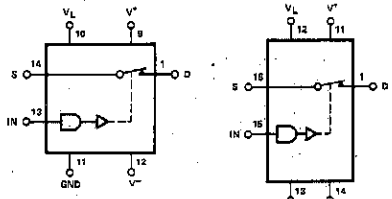
FIGURE 18. Digitally Tuned Low Power Active Filter.

INTERSIL

SWITCHING STATE DIAGRAMS

SWITCH STATES ARE FOR LOGIC "1" INPUT

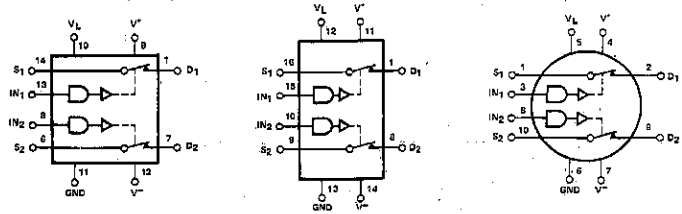
FLATPACK (FD-2) DIP (JE, PE)



SPST

IH5140 ($r_{DS(on)}$ < 75Ω)

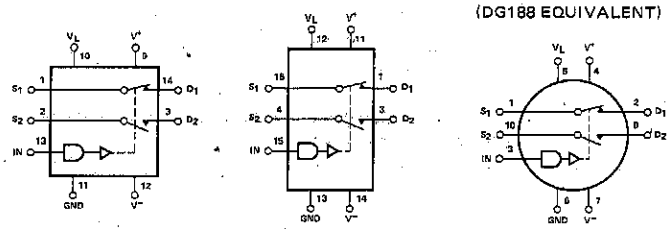
FLATPACK (FD-2) DIP (JE, PE) TO-100



DUAL SPST

IH5141 ($r_{DS(on)}$ < 75Ω)

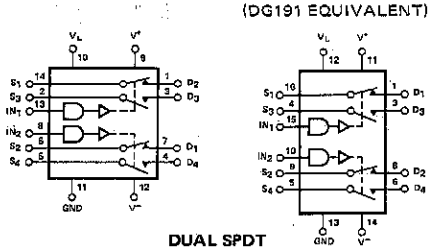
FLATPACK (FD-2) DIP (JE, PE) TO-100 (DG188 EQUIVALENT)



SPDT

IH5142 ($r_{DS(on)}$ < 75 Ω)

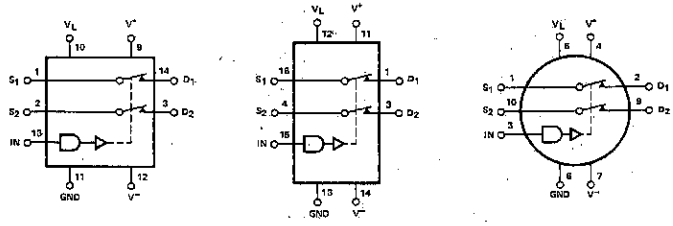
FLATPACK (FD-2) DIP (JE, PE) (DG191 EQUIVALENT)



DUAL SPDT

IH5143 ($r_{DS(on)}$ < 75Ω)

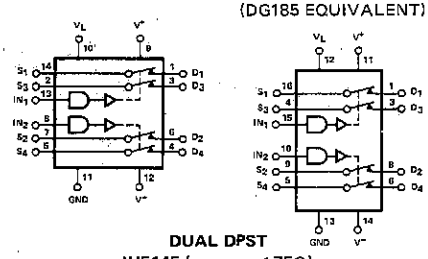
FLATPACK (FD-2) DIP (JE, PE) TO-100



DPST

IH5144 ($r_{DS(on)}$< 75Ω)

FLATPACK (FD-2) DIP (JE, PE) (DG185 EQUIVALENT)



DUAL DPST

IH5145 ($r_{DS(on)}$ < 75Ω)

IH5208

4-Channel Differential Fault Protected CMOS Analog Multiplexer

FEATURES

- Ultra low leakage — $I_{D(off)} \leq 100pA$
- Power supply quiescent current less than 1μA
- ±13V analog signal range
- No SCR latchup
- Break-before-make switching
- TTL and CMOS compatible strobe control
- Pin compatible with HI509, DG509 and AD7509
- All channels OFF ($I_{ILK} \leq 100nA$) when power OFF, for analog signals up to ±25V
- Any channel turns OFF ($I_{ILK} \leq 100nA$) if input exceeds supply rails by up to ±25V. Throughput always < ±14V (±15V supplies)
- TTL and CMOS compatible binary Address and ENable inputs

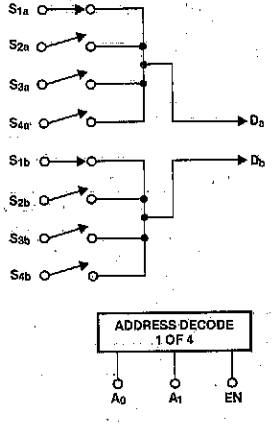
GENERAL DESCRIPTION

The IH5208 is a dielectrically isolated CMOS monolithic analog multiplexer, designed as a plug-in replacement for the DG509 and similar devices, but adding fault protection to the standard performance. A unique serial MOSFET switch ensures that an OFF channel will remain OFF when the input exceeds the supply rails by up to ±25V, even with the supply voltage at zero. Further, an ON channel will be limited to a throughput of about 1.5V less than the supply rails, thus affording protection to any following circuitry such as op amps, D/A converters, etc. Cross talk onto "good" channels is also prevented.

A binary 2-bit address code together with the ENable input allows selection of any channel pair or none at all. These 3 inputs are all TTL compatible for easy logic interface; the ENable input also facilitates MUX expansion and cascading.

3

FUNCTIONAL DIAGRAM



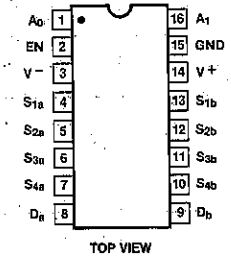
2 LINE BINARY ADDRESS INPUTS
(0 0) AND EN = 1
ABOVE EXAMPLE SHOWS CHANNELS 1a AND 1b ON

DECODE TRUTH TABLE

A_1	A_0	EN	ON SWITCH PAIR
X	X	0	NONE
0	0	1	1a, 1b
0	1	1	2a, 2b
1	0	1	3a, 3b
1	1	1	4a, 4b

A_0, A_1, EN
Logic "1" = $V_{AH} \geq 2.4V$
Logic "0" = $V_{AL} \leq 0.8V$

PIN CONFIGURATION (outline dwg JE, PE)



TOP VIEW

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH5208MJE	−55°C to +125°C	16 pin CERDIP
IH5208IJE	−20°C to +85°C	16 pin CERDIP
IH5208CPE	0°C to 70°C	16 pin plastic DIP

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground ..... −15V, +15V
V_S or V_D to V^+ ..... +25V, −40V
V_S or V_D to V^- ..... −25V, +40V
V^+ to Ground 16V
V^- to Ground ..... −16V
Current (Any Terminal) 20mA

Operating Temperature ..... −55 to 125°C
Storage Temperature ..... −65 to 150°C
Power Dissipaton (Package)* 1200mW

*All leads soldered or welded to PC board. Derate 10mW/°C above 70°C.

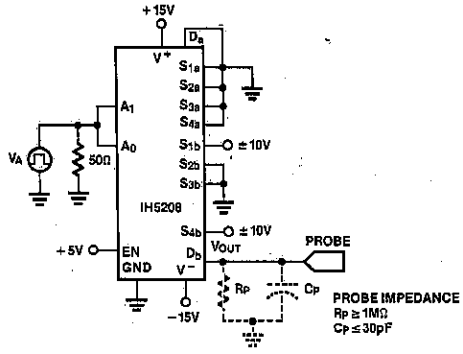
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS $V^+ = 15V$, $V^- = -15V$, $V_{EN} = 2.4V$, unless otherwise specified.

3

	CHARACTERISTIC		MEASURED TERMINAL	NO TESTS PER TEMP	TYP 25°C	MAX LIMITS M SUFFIX −55°C	M SUFFIX 25°C	M SUFFIX 125°C	I/C SUFFIX −20°C/ 0°C	I/C SUFFIX 25°C	I/C SUFFIX 85°C/ 70°C	UNIT	TEST CONDITIONS	
SWITCH	$r_{DS(on)}$		S to D	8	700	900	900	1200	1200	1200	1800	Ω	$V_D = 10V$, $I_S = -1.0mA$	Sequence each switch on
				8	500	900	900	1200	1200	1200	1800	Ω	$V_D = -10V$ $I_S = -1.0mA$	$V_{AL} = 0.8V$, $V_{AH} = 2.4V$
	$\Delta r_{DS(on)}$				5		10			10		%	$\Delta r_{DS(on)} = \frac{r_{DS(on)max} - r_{DS(on)min}}{r_{DS(on)avg.}}$ $V_S = \pm 10V$	
	$I_{S(off)}$		S	8	0.002		0.05	50		0.1	50	nA	$V_S = 10V$, $V_D = -10V$	
				8	0.002		0.05	50		0.1	50		$V_S = -10V$, $V_D = 10V$	
	$I_{D(off)}$		D	1	0.03		0.1	100		0.2	100		$V_D = 10V$, $V_S = -10V$	$V_{EN} = 0$
				1	0.03		0.1	100		0.2	100		$V_D = -10V$, $V_S = 10V$	
	$I_{D(on)}$		D	8	0.1		0.2	100		0.4	100		$V_{S(All)} = V_D = 10V$	Sequence each switch on
				8	0.1		0.2	100		0.4	100		$V_{S(All)} = V_D = -10V$	$V_{AL} = 0.8V$, $V_{AH} = 2.4V$
FAULT	I_S with Power OFF		S	8	1		100	1000	50	50	5000	nA	$V^+ = V^- = 0V$, $V_S = \pm 25V$, $V_{EN} = V_O = 0V$, A_0, A_1, $A_2 = 0V$ or 5V	
	$I_{S(off)}$ with Overvoltage (Note 1)		S	8	1		2000	5000		5000	5000		$V_S = \pm 25V$, $V_D = \mp 10V$	Sequence each switch
IN	$I_{EN(on)}$ $I_{A(on)}$ or $I_{EN(off)}$ $I_{A(off)}$		A_0, A_1, A_2, or EN	4	.01		−10	−30		−10	−30	μA	$V_A = 2.4V$ or 0V	
				4	.01		10	30		10	30		$V_A = 15V$ or 0V	
DYNAMIC	$t_{transition}$		D		0.3		1					μs	See Figure 1	
	t_{open}		D		0.2								See Figure 2	
	$t_{on(EN)}$		D		0.6		1.5						See Figure 3	
	$t_{off(EN)}$		D		0.4		1							
	t_{on}-t_{off} Break-Before-Make Delay Settling Time		D	8	50		25			10		ns	$V_{EN} = +5V$, A_0, A_1, A_2 Strobed $V_{IN} = \pm 10V$, Figure 4	
	"OFF" Isolation		D		60							dB	$V_{EN} = 0$, $R_L = 200\Omega$, $C_L = 3pF$, $V_S = 3$ VRMS, f = 500 KHz	
	$C_{S(off)}$		S		5							pF	$V_S = 0$	$V_{EN} = 0V$, f = 140 KHz to 1 MHz
	$C_{D(off)}$		D		25								$V_D = 0$	
	$C_{DS(off)}$		D to S		1								$V_S = 0$, $V_D = 0$	
SUP	Supply Current	+	V^+	1	500	900	750	600		1000		μA	All V_A, $V_{EN} = 0$ or 5V	
		−	V^-	1	500	900	750	600		1000				

Note 1. Readings taken 400ms after the overvoltage occurs.



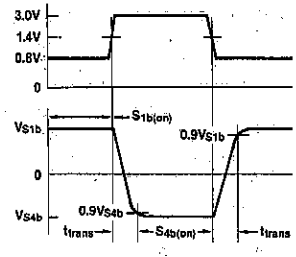
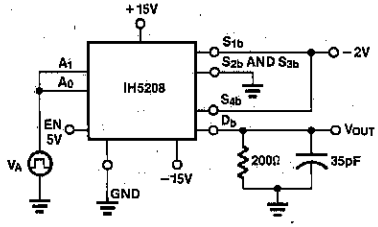


Figure 1. t_{trans} Switching Test



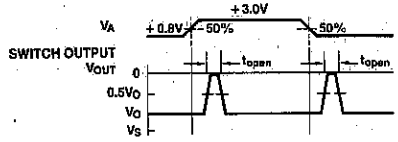
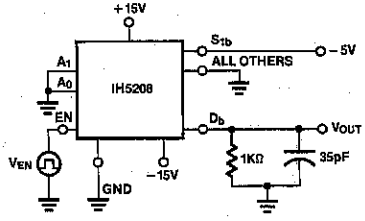


Figure 2. t_{open} (Break-Before-Make) Switching Test



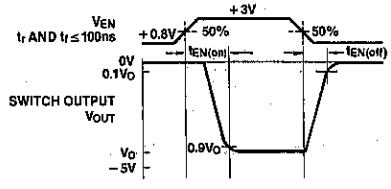
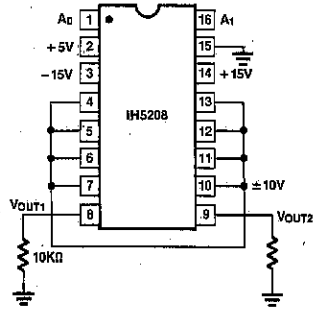


Figure 3. t_{on} and t_{off} Switching Test



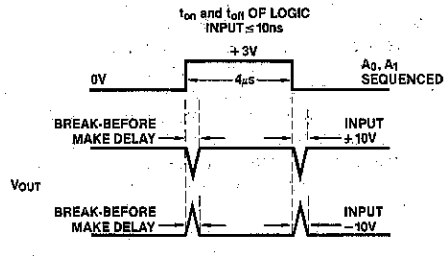


Figure 4. Break-Before-Make Delay Test

DETAILED DESCRIPTION

The IH5208, like all Intersil's multiplexers, contains a set of CMOS switches forming the channels, and driver and decoder circuitry to control which channel turns ON, if any. In addition, the IH5208 contains an internal regulator which provides a fully TTL compatible ENable input that is identical in operation to the Address inputs. This does away with the special treatments that many multiplexer enable inputs require for proper logic swings. This identical circuit treatment of the ENable and Address lines also helps ensure the extension of break-before-make switching to wider multiplexer systems (see applications section).

Another, and more important, difference lies in the switching channel. Previous devices have used parallel n- and p-channel MOSFET switches, and while this scheme yields reasonably good ON resistance characteristics and allows the switching of rail-to-rail input signals, it also has a number of drawbacks. The sources and drains of the switch transistors will conduct to the substrate if the inpout goes outside the supply rails, and even careful use of diodes cannot avoid channel-to-output and channel-to-channel coupling in cases of input overrange. The IH5208 uses a novel series arrangement of the p- and n-channel switches (Figure 5) combined with the dielectrically isolated process to obviate these problems.

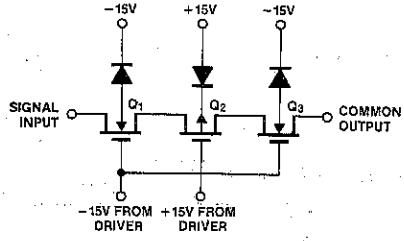


Figure 5. Series Connection of Channel Switches

Within the normal analog signal band, the inherent variation of switch ON resistance will balance out almost as well as the customary parallel configuration, but as the analog signal approaches either supply rail, even for an ON channel, either the p- or the n-channel will become a source follower, disconnecting the channel (Figure 6). Thus protection is provided to any input or output channel against overvoltage on any (or several) input or output channels even in the absence of multiplexer supply voltages, and applies up to the breakdown voltage of the respective switches, drawing only leakage currents. Figure 7 shows a more detailed schematic of the channel switches, including the back-gate driver devices which ensure optimum channel ON resistances and breakdown voltage under the various conditions.

Under some circumstances, if the logic inputs are present but the multiplexer supplies are not, the circuit will use the logic inputs as a sort of phantom supply; this could result in an output up to that logic level. To prevent this from occurring, simply ensure that the ENable pin is LOW any time the multiplexer supply voltages are missing (Figure 8).

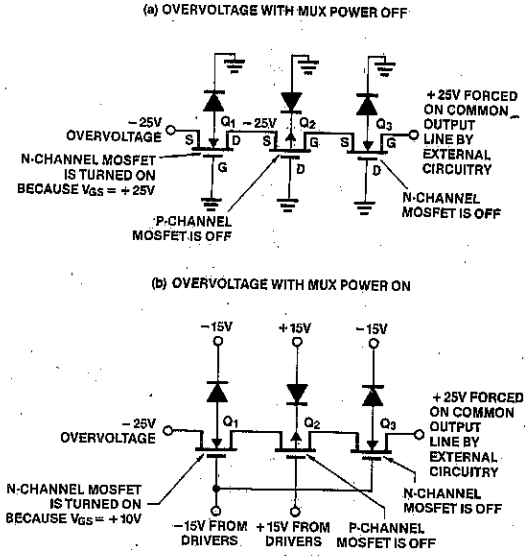


Figure 6. Overvoltage Protection

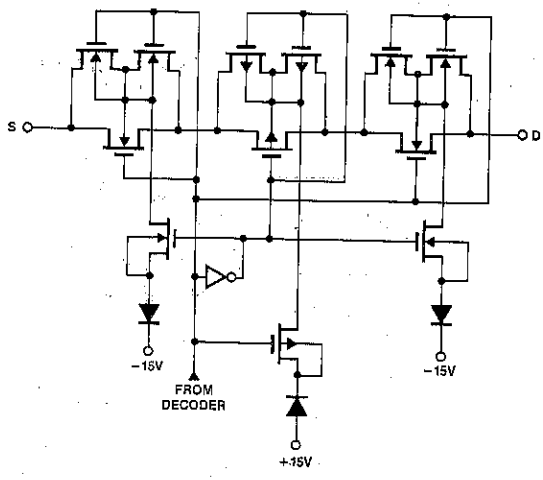


Figure 7. Detailed Channel Switch Schematic

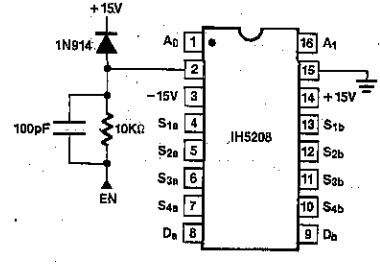


Figure 8. Protection Against Logic Input

MAXIMUM SIGNAL HANDLING CAPABILITY

The IH5208 is designed to handle signals in the ±10V range, with a typical $r_{DS(on)}$ of 600Ω; it can successfully handle signals up to ±13V, however, $r_{DS(on)}$ will increase to about 1.8K. Beyond ±13V the device approaches an open circuit, and thus ±12V is about the practical limit, see Figure 9.

Figure 10 shows the input/output characteristics of an ON channel, illustrating the inherent limiting action of the series switch connection (see Detailed Description), while Figure 11 gives the ON resistance variation with temperature.

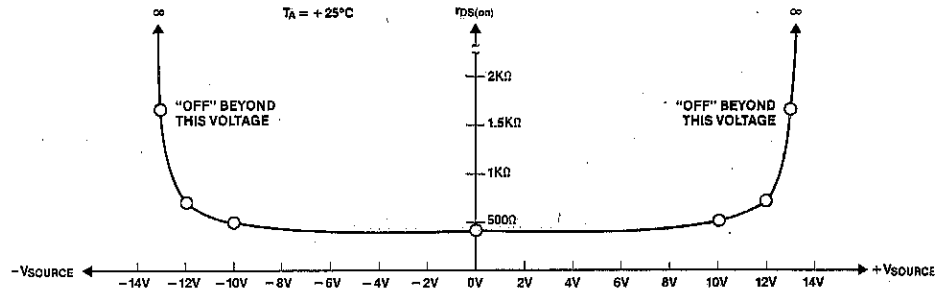


Figure 9. $r_{DS(on)}$ vs Signal Input Voltage @ T_A = +25°C

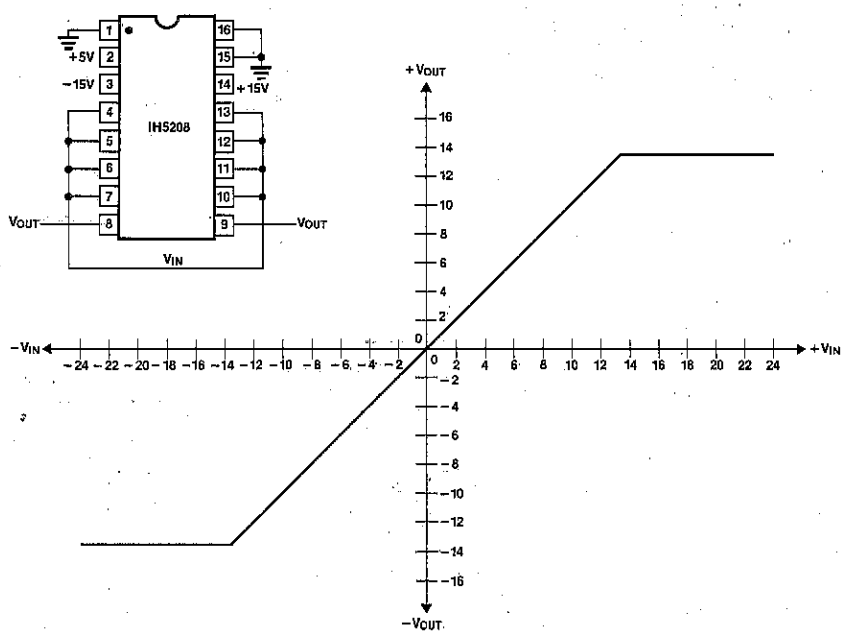


Figure 10. MUX Output Voltage vs Input Voltage
Channel 1 Shown; All Channels Similar

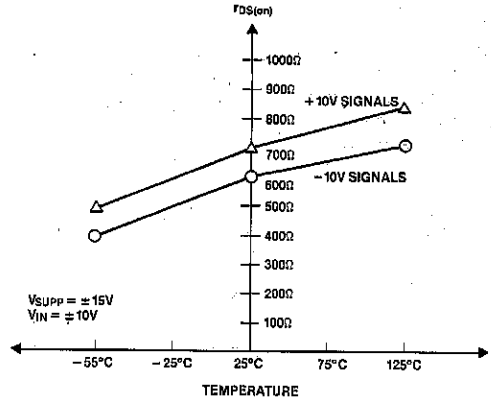


Figure 11. Typical $r_{DS(on)}$ vs Temperature

3

USING THE IH5208 WITH SUPPLIES OTHER THAN ±15V

The IH5208 will operate successfully with supply voltages from ±5V to ±15V; $r_{DS(on)}$ increases as supply voltage decreases, see Figure 12. Leakage currents, however, decrease with a lowering of supply voltage, and therefore the error term product of $r_{DS(on)}$ and leakage current remains reasonably constant. $r_{DS(on)}$ also decreases as signal levels decrease. For high system accuracy [acceptable levels of $r_{DS(on)}$] the maximum input signal should be 3V less than the supply voltages. The logic thresholds will remain TTL compatible.

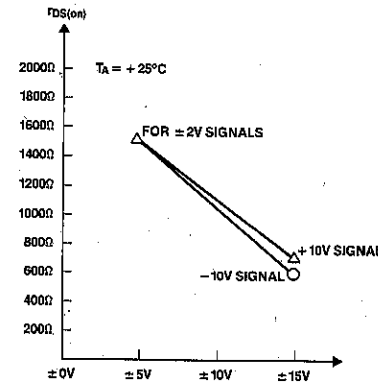
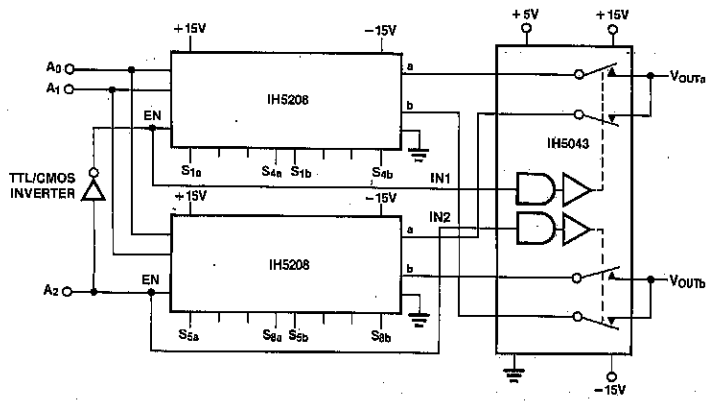


Figure 12. $r_{DS(on)}$ vs Supply Voltages

IH5208 APPLICATIONS INFORMATION

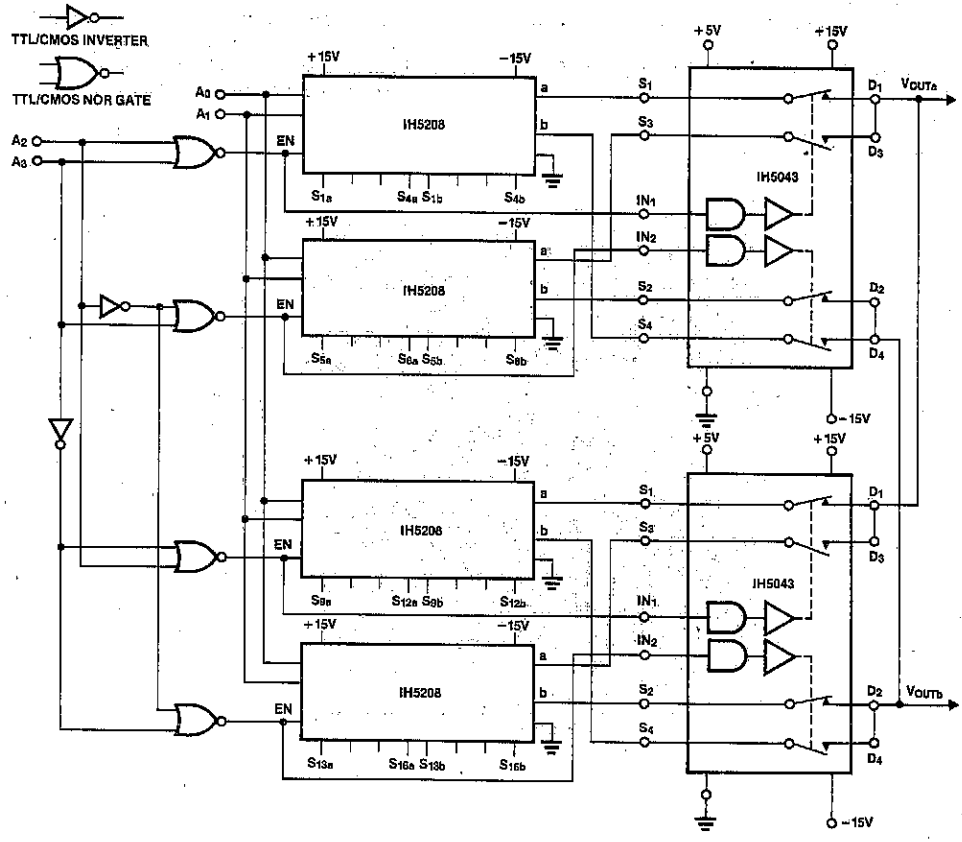


DECODE TRUTH TABLE

A_2	A_1	A_0	ON SWITCH PAIR
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

Figure 13. 2 of 16 channel multiplexer using two IH5208s. Overvoltage protection and break-before-make switching are extended to all channels.

IH5208 APPLICATIONS INFORMATION (Continued)



DECODE TRUTH TABLE

A_3	A_2	A_1	A_0	ON SWITCH		ON SWITCH	
0	0	0	0	S1a		S1b	
0	0	0	1	S2a		S2b	
0	0	1	0	S3a		S3b	
0	0	1	1	S4a		S4b	
0	1	0	0	S5a		S5b	
0	1	0	1	S6a		S6b	
0	1	1	0	S7a		S7b	
0	1	1	1	S8a	V_{OUTa}	S8b	V_{OUTb}
1	0	0	0	S9a		S9b	
1	0	0	1	S10a		S10b	
1	0	1	0	S11a		S11b	
1	0	1	1	S12a		S12b	
1	1	0	0	S13a		S13b	
1	1	0	1	S14a		S14b	
1	1	1	0	S15a		S15b	
1	1	1	1	S16a		S16b	

Figure 14. Submultiplexed 2 of 32 system. The two IH5043s are overvoltage protected by the IH5208s. Submultiplexing reduces output capacitance and leakage currents.

APPLICATION NOTES

Further information may be found in:

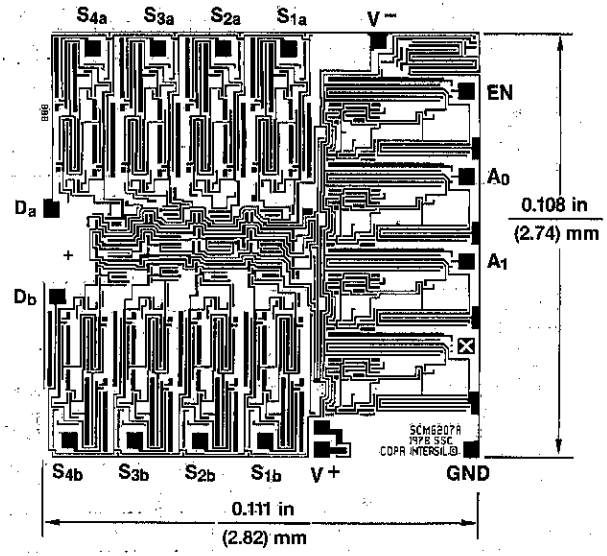
A003 "Understanding and Applying the Analog Switch," by Dave Fullagar

A006 "A New CMOS Analog Gate Technology," by Dave Fullagar

A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing," by Ed Slieger

R009 "Reduce CMOS Multiplexer Troubles Through Proper Device Selection," by Dick Wilenken

CHIP TOPOGRAPHY



IH5341
CMOS Monolithic RF/Video Switch

FEATURES

- $r_{ds(on)} < 75\Omega$, flat from DC to 100MHz (< 3dB)
- "OFF" isolation > 60dB @ 10MHz
- Cross coupling isolation > 60dB @ 10MHz
- Directly compatible with TTL, CMOS
- Wide operating power supply range
- Power supply current < 1μA
- "Break-before-Make" switching
- Fast switching (80ns/150ns typ)

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH5341CPD	0 to +70°C	14-Pin DIP
IH5341ITW	−20°C to +85°C	TO-100
IH5341MTW	−55°C to +125°C	TO-100

GENERAL DESCRIPTION

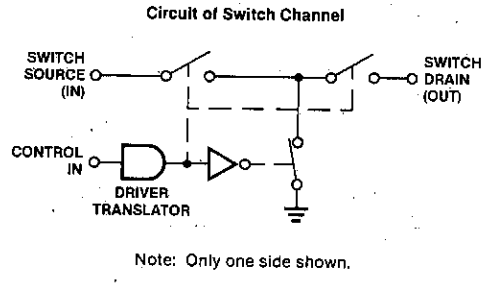
The IH5341 is a dual SPST, CMOS monolithic switch which uses a "Series/Shunt" ("T" switch) configuration to obtain high "OFF" isolation while maintaining good frequency response in the "ON" condition.

Construction of remote and portable video equipment with extended battery life is facilitated by the extremely low current requirements. Switching speeds are typical $t_{on} = 150ns$ and $t_{off} = 80ns$, and guaranteed "Break-before-Make" switching.

Switch "ON" resistance is typically 40Ω–50Ω with ±15V power supplies, increasing to typically 175Ω for ±5V supplies. The devices are available in TO-100 and 14-pin epoxy DIP packages.

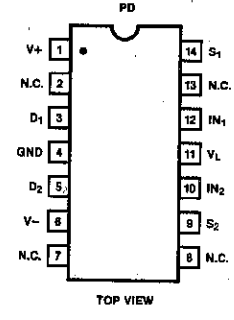
3

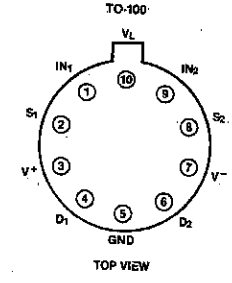
FUNCTIONAL DIAGRAM



Note: Only one side shown.

PIN CONFIGURATIONS





ABSOLUTE MAXIMUM RATINGS

Supply Voltages V^+ and V^- ..... ±17V
Current in any Terminal 50mA
Analog Input Voltage ..... V^+ to V^-
Operating Temperature
(M Version) ..... −55°C to +125°C
(I Version) ..... −20°C to +85°C
(C Version) ..... 0 to +70°C

Storage Temperature ..... −65°C to +160°C
Power Dissipation 250mW
Derate above 25°C @ ..... 7.5mW/°C
Logic Control Voltage ..... V^+ to V^-
Voltage on Pin 10 ..... V^+ to V^-
Lead Temperature (soldering, 10 seconds) ..... 300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

$V^+ = +15V$, $V_L = +5V$, $V^- = -15V$, $T_A = 25°C$ unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	TYP	M GRADE DEVICE			I/C GRADE DEVICE			UNITS
				−55°C	+25°C	+125°C	−20/0°C	+25°C	+85/ +70°C	
Supply Voltage Ranges										
Positive Supply	V^+		4.5>16		5 to 15			5 to 15		
Logic Supply	V_L	(Note 3)	4.5>V^+		5 to V^+			5 to V^+		V
Negative Supply	V^-		−4> −16		−5 to −15			−5 to −15		
Switch "ON" Resistance (Note 4)	$r_{ds(on)}$	V_D = −5V to +5V, I_S = 10mA, V_{IN} = 2.4V		75	75	100	75	75	100	Ω
		V_D = −15V to +15V		125	125	175	150	150	175	
Switch "ON" Resistance	$r_{ds(on)}$	$V^+ = V_L = 5V$, V_{IN} = 3V, $V^- = 5V$, $V_D = \pm 5V$		250	250	350	300	300	350	
On Resistance Match		I_S = 10mA, $V_D = \pm 5V$	5							
Switch "OFF" Leakage (Notes 2 and 4)	$I_{D(off)}$ or $I_{S(off)}$	$V_{S/D}$ = +5V to −5V, V_{IN} = 0.8V		0.1	0.1	20	0.5	0.5	20	nA
		$V_{S/D}$ = +14V to −14V		0.2	0.2	50	1.0	1.0	100	
Switch "ON" Leakage	$I_{D(on)}$ + $I_{S(on)}$	V_D = +5V or −5V, V_{IN} = 2.4V		0.3	0.3	50	1.0	1.0	40	
		V_D = +14V to −14V		0.5	0.5	100	1.0	1.0	100	
Input Logic Current	I_{IN}	V_{IN} > 2.4V or < 0		1	1	10	1	1	10	µA
Positive Supply Quiescent Current	I^+	V_{IN} = 0V or +5V		1	1	10	1	1	10	
Negative Supply Quiescent Current	I^-	V_{IN} = 0V or +5V		1	1	10	1	1	10	
Logic Supply Quiescent Current	I_L	V_{IN} = 0V or +5V		1	1	10	1	1	10	

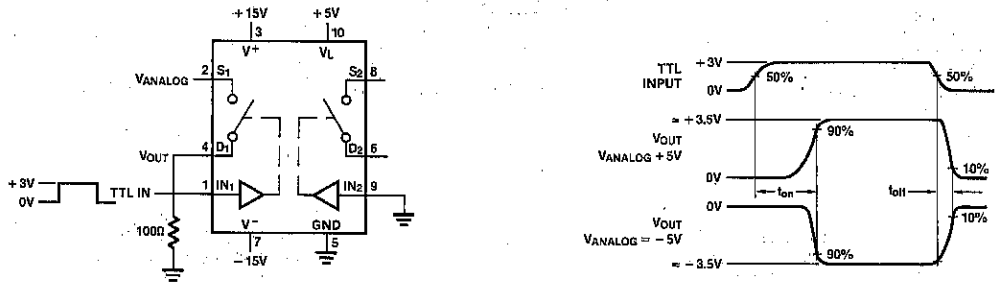
Note 1: Typical values are not tested in production. They are given as a design aid only.
Note 2: Positive and negative voltages applied to opposite sides of switch, in both directions successively.
Note 3: These are the operating voltages at which the other parameters are tested, and are not directly tested.
Note 4: The logic inputs are either greater than or equal to 2.4V or less than or equal to 0.8V, as required, for this test.

AC ELECTRICAL CHARACTERISTICS $V^+ = +15V$, $V_L = +5V$, $V^- = 0V$, $T_A = 25°C$ unless otherwise specified (Note 5).

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Switch "ON" Time	t_{on}	See Figure 1			300	ns
Switch "OFF" Time	t_{off}	See Figure 1			150	
"OFF" Isolation Rejection Ratio	OIRR	See Figure 2 (Note 6)	60			dB
Cross Coupling Rejection Ratio	CCRR	See Figure 3 (Note 6)	60			
Frequency where $r_{ds(on)} = 0.7 \times DC$		See Figure 4 (Note 6)	100			MHz

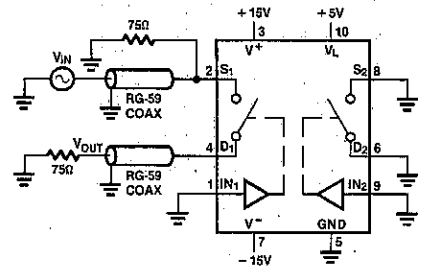
Note 5: All AC parameters are sample tested only.
Note 6: Test circuit should be built on copper clad ground plane board, with correctly terminated coax leads, etc.

TEST CIRCUITS



Note: Only one side shown. Other acts identically.

Figure 1. Switching Time Test Circuit and Waveforms

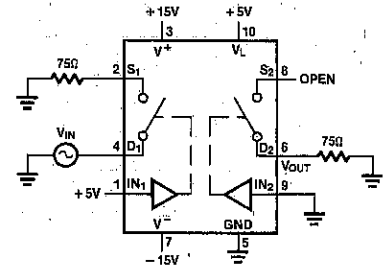


$V_{IN} = \pm 5V$ (10Vp-p) @ f = 10MHz

$OIRR = 20 \log \frac{V_{IN}}{V_{OUT}}$

Note: Only one side shown. Other acts identically.

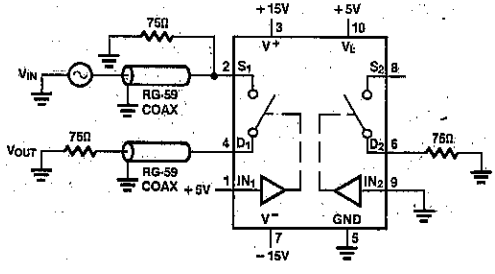
Figure 2. OFF Isolation Test Circuit



$V_{IN} = 225mVrms$ @ f = 10MHz

$CCRR = 20 \log \frac{V_{IN}}{V_{OUT}}$

Figure 3. Cross-Coupling Rejection Test Circuit



Note: Only one side shown. Other acts identically.

Figure 4. $r_{ds(AC)}$ Pole Frequency Test Circuit

$r_{ds(on)3dB}$ = > frequency where $20 \log \frac{V_{OUT}}{V_{IN}}$ changes by +3dB

i.e., from DC to f = 40MHz, $20 \log \frac{V_{OUT}}{V_{IN}} \cong -4dB$;

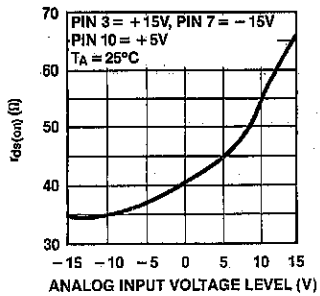
when this ratio reaches −1dB, the frequency causing this is $r_{ds(on)3dB}$ frequency.

$V_{IN} = 225mVrms$ @ f = 10MHz -100MHz

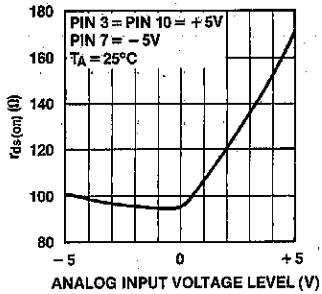
$\frac{V_{OUT}}{V_{IN}} = \frac{75\Omega\ (load)}{75\Omega + r_{ds(on)}} = \frac{141mVrms}{225mVrms}$ typically @ f = 10MHz

TYPICAL CHARACTERISTICS

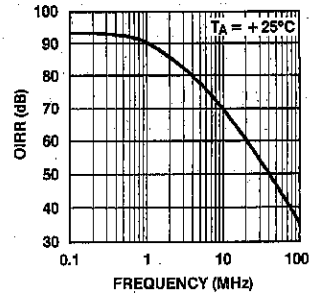
$r_{ds(on)}$ vs Analog Input Voltage with ±15V Power Supplies



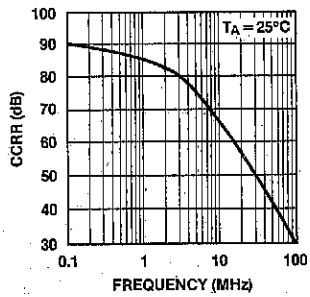
$r_{ds(on)}$ vs Analog Input Level with ±5V Power Supplies



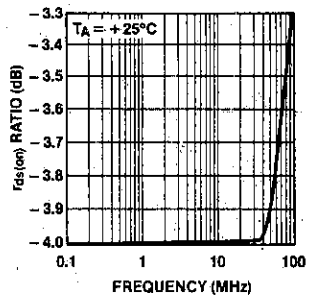
OIRR (OFF Isolation Rejection) vs Frequency (See Figure 2)



CCRR (Cross Coupling Rejection) vs Frequency (See Figure 3)



Switch $r_{ds(on)}$ Change with Frequency (Expressed in Voltage Divider Terms with a 75Ω Load (See Figure 4)



DETAILED DESCRIPTION

As can be seen in the Functional Diagram, the switch circuitry is of the so-called "T" configuration, where a shunt switch is closed when the switch is open. This provides much *better isolation between* the input and the output than does the single series switch, especially at high frequencies, and the result is excellent performance in the Video and RF region compared to conventional Analog Switches.

The input level shifting circuit is similar to that of the IH5140 Series of Analog Switches, and gives very high speed and guaranteed "Break-before-Make" action, with negligible static power consumption and TTL compatibility.

APPLICATIONS

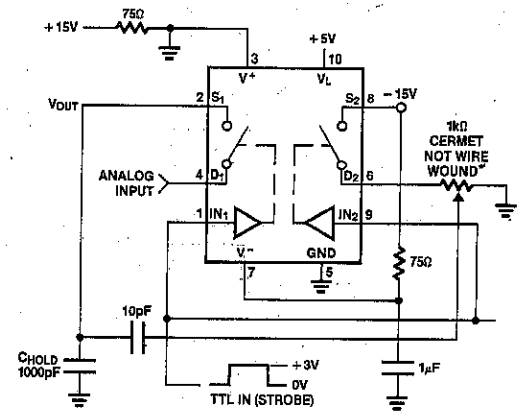
Charge Compensation Techniques

Charge injection results from the signals out of the level translation circuit being coupled through the gate-channel and gate-source/drain capacitances to the switch inputs and outputs. This feedthrough is particularly troublesome in Sample-and-Hold or Track-and-Hold applications, as it causes a Sample (Track) to Hold offset. The IH5341 devices have a typical injected charge of 30pC–50pC (corresponding to 30mV–50mV in a 1000pF capacitor), at $V_{S/D}$ of about 0V.

This Sample (Track) to Hold offset can be compensated by bringing in a signal equal in magnitude but of the opposite polarity. The circuit of Figure 5 accomplishes this charge injection compensation by using one side of the device as a S & H (T & H) switch, and the other side as a generator of a compensating signal. The 1k potentiometer allows the user to adjust the net injected charge to exactly zero for any analog voltage in the −5V to +5V range.

Since the individual parts are very consistent in their charge injection, it is possible to replace the potentiometer with a pair of fixed resistors, and achieve less than 5mV error for all devices without adjustment.

An alternative arrangement, using a standard TTL inverter to generate the required inversion, is shown in Figure 6. The capacitor needs to be increased, and becomes the only method of adjustment. A fixed value of 22pF is good for analog values referred to ground, while 35pF is optimum for AC coupled signals referred to −5V as shown in the figure. The choice of −5V is based on the virtual disappearance at this analog level of the transient component of switching charge injection. This combination will lead to a virtually "glitch-free" switch.



*Adjust pot for 0mVp-p step @ V_{OUT} with no analog (AC) signal present

Figure 5. Charge Injection Compensation

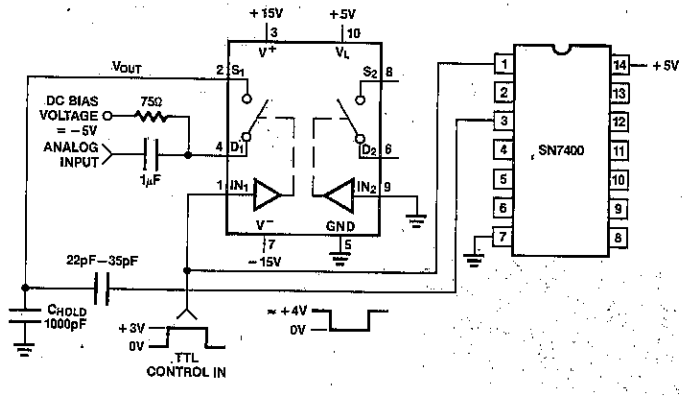


Figure 6. Alternative Compensation Circuit

Overvoltage Spike Protection

If sustained operation with no supplies but with analog signals applied is possible, it is recommended that diodes (such as 1N914) be inserted in series with the supply lines to the IH5341. Such conditions can occur if these signals come from a separate power supply or another location, for example. The diodes will be reverse biased under this type of operation, preventing heavy currents from flowing from the analog source through the IH5341.

The same method of protection will provide over ±25V overvoltage protection on the analog inputs when the supplies are present. The schematic for this connection is shown in Figure 7.

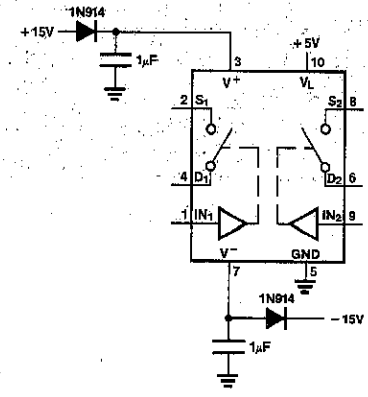
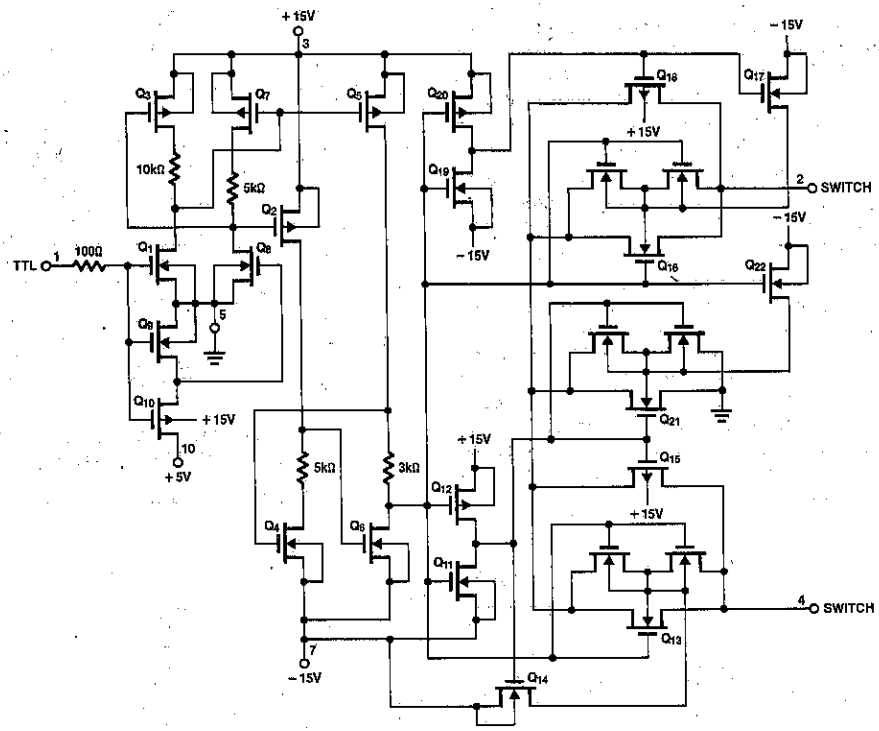
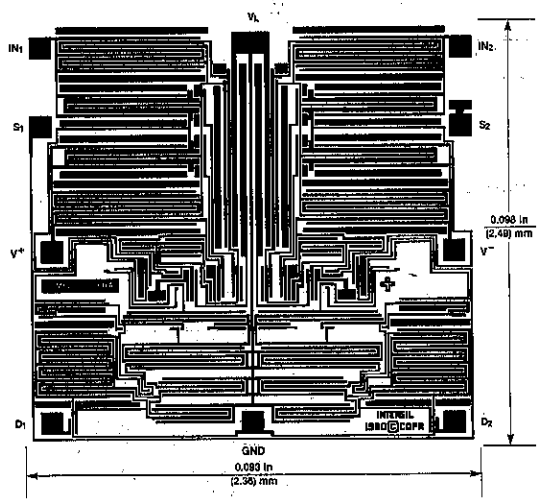


Figure 7. Overvoltage Protection Circuit

EQUIVALENT SCHEMATIC DIAGRAM (1/2 of actual circuit on chip shown)



CHIP TOPOGRAPHY



IH6108
8-Channel CMOS Analog Multiplexer

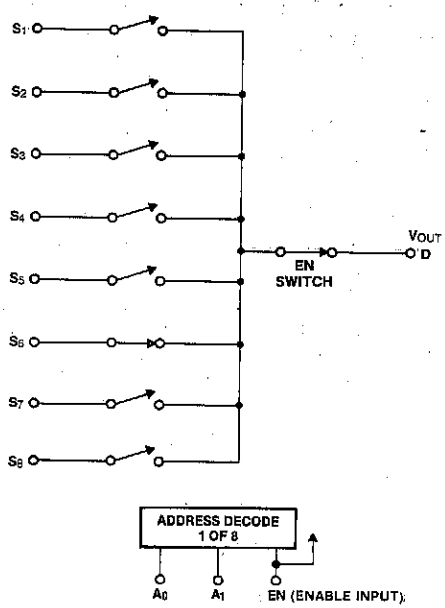
FEATURES
- **Ultra Low Leakage — $I_{D(off)} \leq 100pA$**
- **$r_{DS(on)}$ < 400 ohms over full signal and temperature range**
- **Power supply quiescent current less than 100μA**
- **±14V analog signal range**
- **No SCR latchup**
- **Break-before-make switching**
- **Binary Address control (3 Address inputs control 8 channels)**
- **TTL and CMOS compatible strobe control**
- **Pin compatible with DG508, HI-508 & AD7508**

GENERAL DESCRIPTION

The IH6108 is a CMOS monolithic, one of 8 multiplexer. The part is a plug-in replacement for the DG508. Three line binary decoding is used so that the 8 channels can be controlled by 3 Address inputs; additionally a fourth input is provided to use as a system enable. When the ENable input is high (5V) the channels are sequenced by the 3 line Address inputs, and when low (0V) all channels are off. The 3 Address inputs are controlled by TTL logic or CMOS logic elements, a "0" corresponding to any voltage greater than 2.4V. Note that the ENable input (EN) must be taken to 5V to enable the system and less than 0.8V to disable the system.

3

FUNCTIONAL DIAGRAM



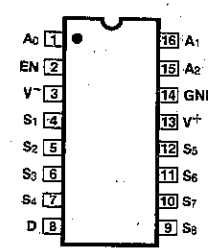
3 LINE BINARY ADDRESS INPUTS
(1 0 1) AND EN @ 5V
ABOVE EXAMPLE SHOWS CHANNEL 6 TURNED ON

DECODE TRUTH TABLE

A_2	A_1	A_0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

A_0, A_1, A_2
Logic "1" = $V_{AH} \geq 2.4V$ $V_{ENH} \geq 4.5V$
Logic "0" = $V_{AL} \leq 0.8V$

PIN CONFIGURATION



ORDERING INFORMATION

Ceramic package available as special order only (IH6108MDE/CDE)

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH6108MJE	-55°C to +125°C	16 pin CERDIP
IH6108CJE	0°C to 70°C	16 pin CERDIP
IH6108CPE	0°C to 70°C	16 pin plastic DIP

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground ..... −15V to 15V
V_S or V_D to V^+ ..... 0, −32V
V_S or V_D to V^- 0, 32V
V^+ to Ground 16V
V^- to Ground ..... −16V
Current (Any Terminal) ..... 30 mA
Current (Analog Source or Drain) ..... 20 mA
Operating Temperature ..... −55 to 125°C
Storage Temperature ..... −65 to 150°C
Lead Temp (Soldering, 10 sec) ..... 300°C
Power Dissipation (Package)* ..... 1200 mW

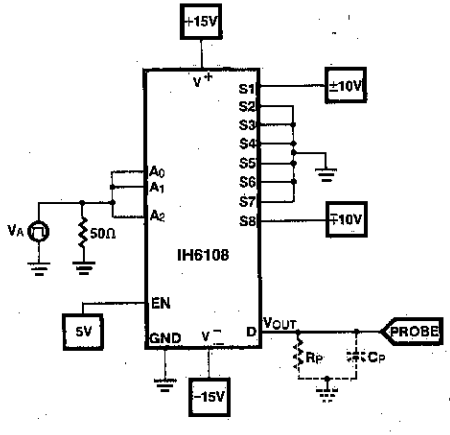
*All leads soldered or welded to PC board. Derate 10 mW/°C above 70°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS $V^+ = 15V$, $V^- = -15V$, $V_{EN} = +5V$ (Note 1), Ground = 0V, unless otherwise specified.

CHARACTERISTIC			MEASURED TERMINAL	NO TESTS PER TEMP	TYP 25°C	MAX LIMITS M SUFFIX −55°C	M SUFFIX 25°C	M SUFFIX 125°C	C SUFFIX 0°C	C SUFFIX 25°C	C SUFFIX 70°C	UNIT	TEST CONDITIONS	
SWITCH	$r_{DS(ON)}$		S to D	8	180	300	300	400	350	350	450	Ω	V_D = 10V, I_S = −1.0mA	Sequence each switch on
				8	150	300	300	400	350	350	450		V_D = −10V, I_S = −1.0mA	V_{AL} = 0.8V, V_{AH} = 2.4V
	$\Delta r_{DS(ON)}$				20							%	$\Delta r_{DS(on)} = \frac{r_{DS(on)max} - r_{DS(on)min}}{r_{DS(on)avg.}}$	$V_S = \pm 10V$
	$I_{S(OFF)}$		S	8	0.002		0.05	50		0.1	50	nA	V_S = 10V, V_D = −10V	V_{EN} = 0
				8	0.002		0.05	50		0.1	50		V_S = −10V, V_D = 10V	
	$I_{D(OFF)}$		D	1	0.03		0.1	100		0.2	100		V_D = 10V, V_S = −10V	
				1	0.03		0.1	100		0.2	100		V_D = −10V, V_S = 10V	
	$I_{D(ON)}$		D	8	0.1		0.2	100		0.4	100		$V_{S(All)}$ = V_D = 10V	Sequence each switch on
				8	0.1		0.2	100		0.4	100		$V_{S(All)}$ = V_D = −10V	V_{AL} = 0.8V, V_{AH} = 2.4V
INPUT	$I_{AN(ON)}$ or $I_{A(on)}$		A_0, A_1 or A_2	3	.01		−10	−30		−10	−30	μA	V_A = 2.4V or 0V	
	$I_{AN(OFF)}$	$I_{A(off)}$	Inputs	3	.01		10	30		10	30		V_A = 15V or 0V	
	I_A		A_0 A_1 A_2	3			−10	−30		−10	−30		V_{EN} = 5V	All V_A = 0 (Address pins)
			EN	1			−10	−30		−10	−30		V_{EN} = 0	
DYNAMIC	$t_{transition}$		D		0.3		1					μs	See Fig. 1	
	t_{open}		D		0.2								See Fig. 2	
	$t_{on(EN)}$		D		0.6		1.5						See Fig. 3	
	$t_{off(EN)}$		D		0.4		1							
	"OFF" Isolation		D		60							dB	V_{EN} = 0, R_L = 200Ω, C_L = 3pF, V_S = 3 VRMS, f = 500 kHz	
	$C_{S(off)}$		S		6							pF	V_S = 0	V_{EN} = 0V, f = 140 kHz to 1 MHz
	$C_{d(off)}$		D		25								V_D = 0	
	$C_{DS(off)}$		D to S		1								V_S = 0, V_D = 0	
SUPPLY	Supply Current	+	V^+	1	40		200			1000		μA	V_{EN} = 5V	All V_A = 0 or 5V
		−	V^-	1	2		100			1000				
	Standby Current	+	V^+	1	1		100			1000			V_{EN} = 0	
		−	V^-	1	1		100			1000				

NOTE 1: See Enable Input Strobing Levels, Section 1.



PROBE IMPEDANCE
$R_P \geq 1M\Omega$.
$C_P \leq 30pF$

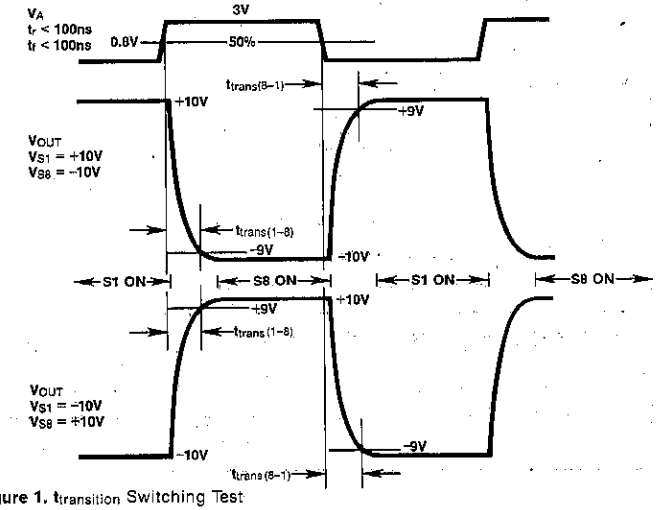


Figure 1. $t_{transition}$ Switching Test

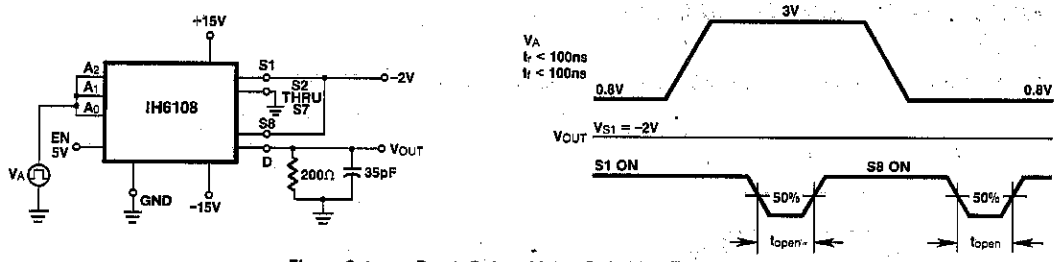


Figure 2. t_{open} (Break-Before-Make) Switching Test

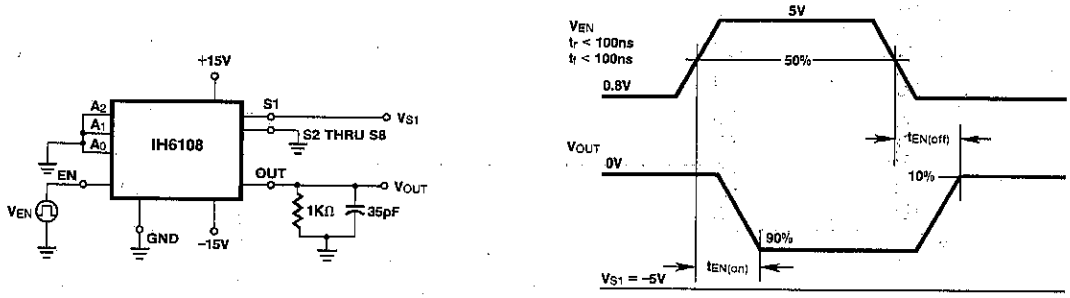


Figure 3. t_{on} and t_{off} Switching Test

IH6108 APPLICATION INFORMATION

I. ENable Input Strobing Levels

The ENable input on the IH6108 requires a minimum of +4.5V to trigger to the "1" state and a maximum of +0.8V to trigger to the "0" state. If the ENable input is being driven from TTL logic, a pull-up resistor of 1k to 3kΩ is required from the gate output to +5V supply. (See Figure 4)

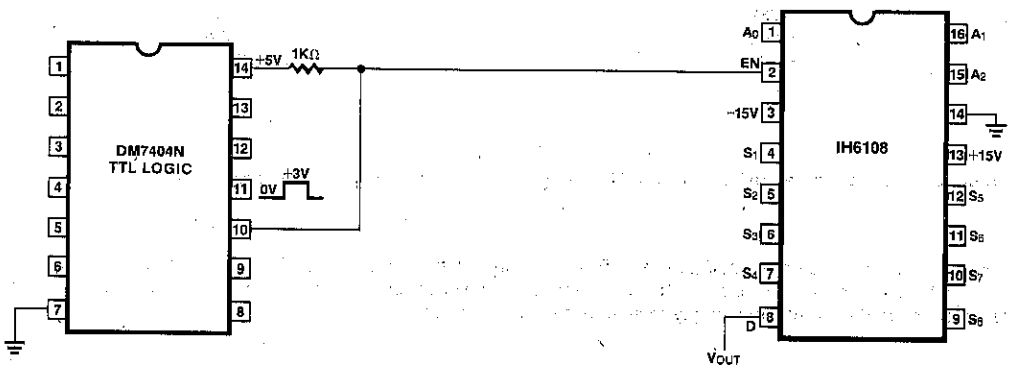


Figure 4. ENable Input Strobing from TTL Logic

IH6108 APPLICATION INFORMATION (Continued)

When the EN input is driven from CMOS logic, no pullup is necessary, see Fig. 5.

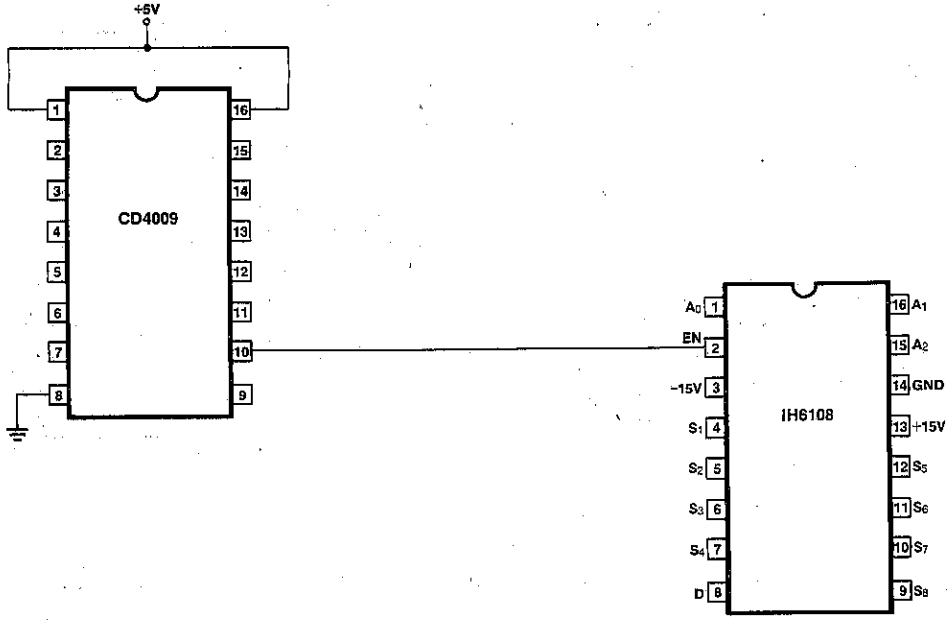


Figure 5. ENable Input Driven from CMOS Logic

The supply voltage of the CD4009 affects the switching speed of the IH6108; the same is true for TTL supply voltage levels. The chart below shows the effect, on t_{trans} for a supply varying from +4.5V to +5.5V.

CMOS OR TTL SUPPLY VOLTAGE	TYPICAL t_{trans} @ 25°C
+4.5V	400ns
+4.75V	300ns
+5.00V	250ns
+5.25V	200ns
+5.50V	175ns

The throughput rate can therefore be maximized by using a +5V to +5.5V supply for the ENable Strobe Logic.

The examples shown in Figures 4 and 5 deal with ENable strobing when expansion to more than eight channels is required; in these cases the EN terminal acts as a fourth address input. If eight channels or less are being multiplexed, the EN terminal can be directly connected to +5V logic supply to enable the IH6108 at all times.

IH6108 APPLICATION INFORMATION (Continued)

II. Using the IH6108 with supplies other than ±15V

The IH6108 can be used with power supplies ranging from ±6V to ±16V. The switch $r_{DS(on)}$ will increase as the supply voltages decrease, however the multiplexer error term (the product of leakage times $r_{DS(on)}$) will remain approximately constant since leakage decreases as the supply voltages are reduced.

Caution must be taken to ensure that the enable (EN) voltage is at least 0.7V below V^+ at all times. If this is not done the Address input strobing levels will not function properly. This may be achieved quite simply by connecting EN (pin 2) to V^+ (pin 13) via a silicon diode as shown in Figure 6. When using this type of configuration, a further requirement must be met-the strobe levels at A0 and A1 must be within 2.5V of the EN voltage in order to define a binary "1" state. For the case shown in Figure 6 the EN voltage is 11.3V which means that logic high at A0 and A1 is = +8.8V (logic low continues to be = 0.8V). In this configuration the IH6108 cannot be driven by TTL (+5V) or CMOS (+5V) logic. It can be driven by TTL open collector logic or CMOS logic with +12V supplies.

If the logic and the IH6108 have common supplies, the EN pin should again be connected to the supply through a silicon diode. In this case, tying EN to the logic supply directly will not work since it violates the 0.7V differential voltage required between V^+ and EN. (See Figure 7) A 1μF capacitor can be placed across the diode to minimize switching glitches.

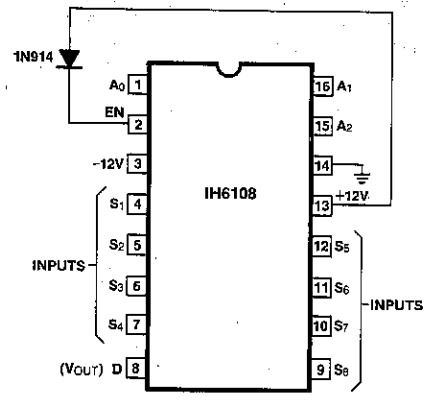


Figure 6. IH6108 Connection Diagram for less than ±15V Supply Operation.

IH6108 APPLICATION INFORMATION (Continued)

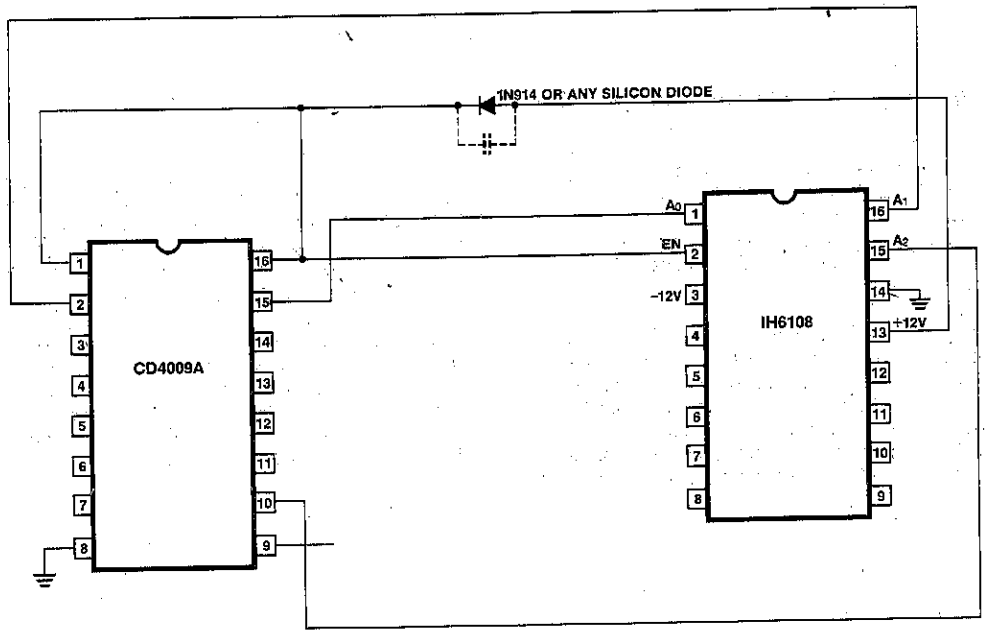


Figure 7. IH6108 Connection Diagram with ENable Input Strobing for less than ±15V Supply Operation.

III. Peak-to-Peak Signal Handling Capability

The IH6108 can handle input signals up to ±14V (actually −15V to +14.3V because of the input protection diode) when using ±15V supplies.

The electrical specifications of the IH6108 are guaranteed for ±10V signals, but the specifications have very minor changes for ±14V signals. The notable changes are slightly lower $r_{DS(on)}$ and slightly higher leakages.

IH6116

16-Channel CMOS Analog Multiplexer

FEATURES

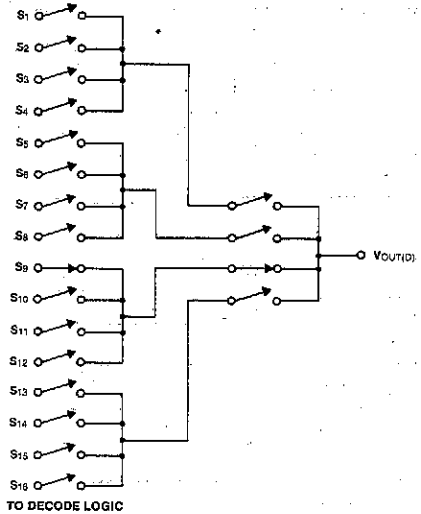
- **Pin compatible with DG506, HI-506 & AD7506**
- **Ultra Low Leakage — $I_{D(off)} \leq 100pA$**
- **±11 analog signal range**
- **$r_{DS(on)}$ <700 ohms over full signal and temperature range**
- **Break-before-make switching**
- **TTL and CMOS compatible Address control**
- **Binary Address control (4 Address inputs control 16 channels)**
- **Two tier submultiplexing to facilitate expandability**
- **Power supply quiescent current less than 100μA**
- **No SCR latchup**

GENERAL DESCRIPTION

The IH6116 is a CMOS monolithic, one of 16 multiplexer. The part is a plug-in replacement for the DG506. Four line binary decoding is used so that the 16 channels can be controlled by 4 Address inputs; additionally a fifth input is provided to use as system enable. When the ENable input is high (5V) the channels are sequenced by the 4 line Address inputs, and when low (0V), all channels are off. The 4 Address inputs are controlled by TTL logic or CMOS logic elements with a "0" corresponding to any voltage less than 0.8V and a "1" corresponding to any voltage greater than 3.0V. Note that the ENable input must be taken to 5V to enable the system and less than 0.8V to disable the system.

3

FUNCTIONAL DIAGRAM

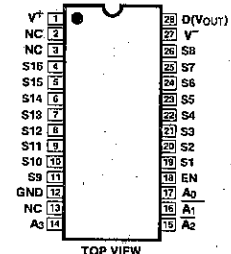


DECODE TRUTH TABLE

A_3	A_2	A_1	A_0	EN	ON SWITCH
x	x	x	x	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

Logic "1" = $V_{AH} \geq 3.0V$ $V_{ENH} \geq 4.5V$
Logic "0" = $V_{AL} \leq 0.8V$

PIN CONFIGURATION



TOP VIEW
V^+ COMMON TO SUBSTRATE

ORDERING INFORMATION

Ceramic package available as special order only (IH6116MDI/CDI)

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH6116MJI	−55°C to +125°C	28 pin CERDIP
IH6116CJI	0°C to 70°C	28 pin CERDIP
IH6116CPI	0°C to 70°C	28 pin Plastic DIP

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground ..... −15V to 15V
V_S or V_D to V^+ ..... 0, −32V
V_S or V_D to V^- 0, 32V
V^+ to Ground 16V
V^- to Ground ..... −16V
Current (Any Terminal) ..... 30 mA
Current (Analog Source or Drain) ..... 20 mA
Operating Temperature ..... −55 to 125°C
Storage Temperature ..... −65 to 150°C
Lead Temperature (Soldering, 10 secs) ..... 300°C
Power Dissipation (Package)* ..... 1200 mW

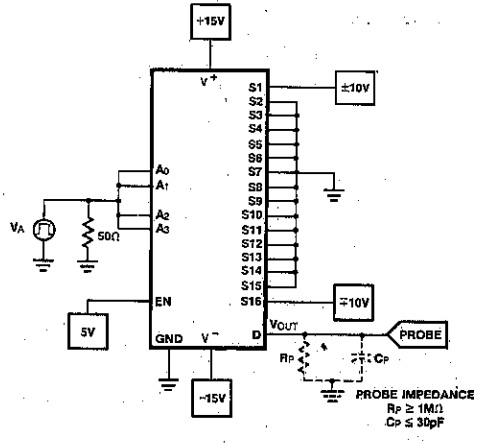
*All leads soldered or welded to PC board. Derate 10 mW/°C above 70°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS $V^+ = 15V$, $V^- = -15V$, $V_{EN} = +5V$ (Note 1), Ground = 0V, unless otherwise specified.

	CHARACTERISTIC		MEASURED TERMINAL	NO TESTS PER TEMP	TYP 25°C	MAX LIMITS M SUFFIX −55°C	M SUFFIX 25°C	M SUFFIX 125°C	C SUFFIX 0°C	C SUFFIX 25°C	C SUFFIX 70°C	UNIT	TEST CONDITIONS	
SWITCH	$r_{DS(ON)}$		S to D	16	480	600	600	700	650	650	750	Ω	$V_D = 10V$, $I_S = -10mA$	Sequence each switch on
				16	300	600	600	700	650	650	750		$V_D = -10V$, $I_S = 10mA$	$V_{AL} = 0.8V$, $V_{AH} = 3V$
	$\Delta r_{DS(ON)}$				20							%	$\Delta r_{DS(on)} = \frac{r_{DS(on)max} - r_{DS(on)min}}{r_{DS(on)avg.}}$ $V_S = \pm 10V$	
	$I_{S(OFF)}$		S	16	0.01		0.1	50		0.2	50	nA	$V_S = 10V$, $V_D = -10V$	$V_{EN} = 0$
				16	0.01		0.1	50		0.2	50		$V_S = -10V$, $V_D = 10V$	
	$I_{D(OFF)}$		D	1	0.1		0.2	100		0.4	100		$V_D = 10V$, $V_S = -10V$	
				1	0.1		0.2	100		0.4	100		$V_D = -10V$, $V_S = 10V$	
	$I_{D(ON)}$		D	16	0.1		0.2	100		0.4	100		$V_{S(All)} = V_D = 10V$	Sequence each switch on
				16	0.1		0.2	100		0.4	100		$V_{S(All)} = V_D = -10V$	$V_{AL} = 0.8V$, $V_{AH} = 3V$
INPUT	$I_{A(on)}$ or $I_{A(off)}$		A_0 A_1 A_2 A_3	4	.01		−10	−30		−10	−30	µA	$V_A = 3.0V$	
				4	.01		10	30		10	30		$V_A = 15V$	
	I_A			4			−10	−30		−10	−30		$V_{EN} = 5V$	All $V_A = 0$
			EN	1			−10	−30		−10	−30		$V_{EN} = 0$	
DYNAMIC	t_{trans}		D		0.6		1					µs	See Fig. 1	
	t_{open}		D		0.2								See Fig. 2	
	$t_{EN(on)}$		D		0.8		1.5						See Fig. 3	
	$t_{EN(off)}$		D		0.3		1							
	"OFF" Isolation		D		60							dB	$V_{EN} = 0$, $R_L = 200\Omega$, $C_L = 3pF$, $V_S = 3$ VRMS, f = 500 kHz	
	$C_{S(OFF)}$		S		5							pF	$V_S = 0$	$V_{EN} = 0$, f = 140 kHz to 1 MHz
	$C_{d(OFF)}$		D		40								$V_D = 0$	
	$C_{ds(OFF)}$		D to S		1								$V_S = 0$, $V_D = 0$	
SUPPLY	Supply Current	+	V^+	1	55		200			1000		µA	$V_{EN} = 5V$	All $V_A = 0$ or 3V
		−	V^-	1	2		100			1000				
	Standby Current	+	V^+	1	1		100			1000			$V_{EN} = 0$	
		−	V^-	1	1		100			1000				

NOTE 1: See Section V. Enable Input Strobing Levels.



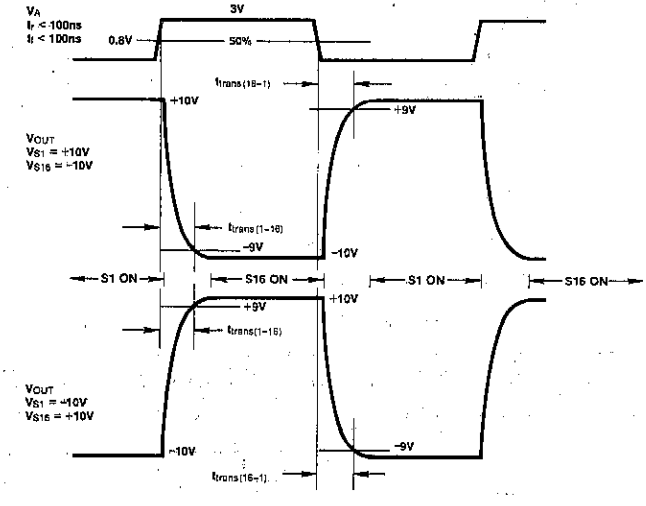


Figure 1

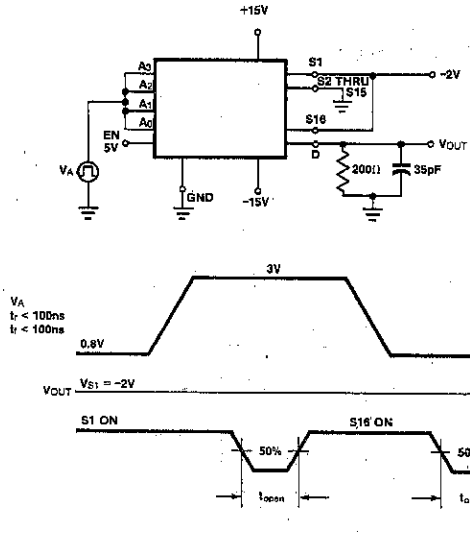


Figure 2

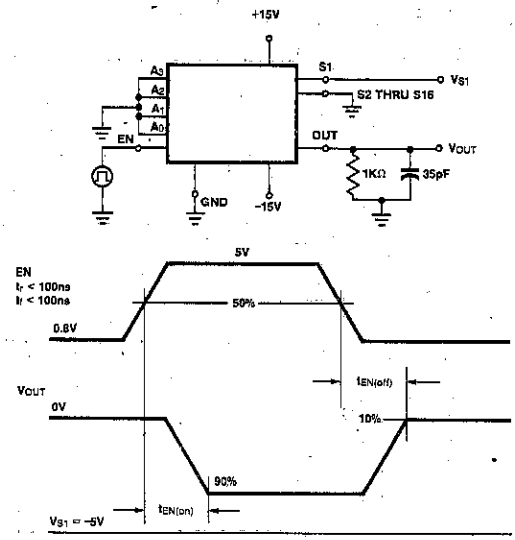
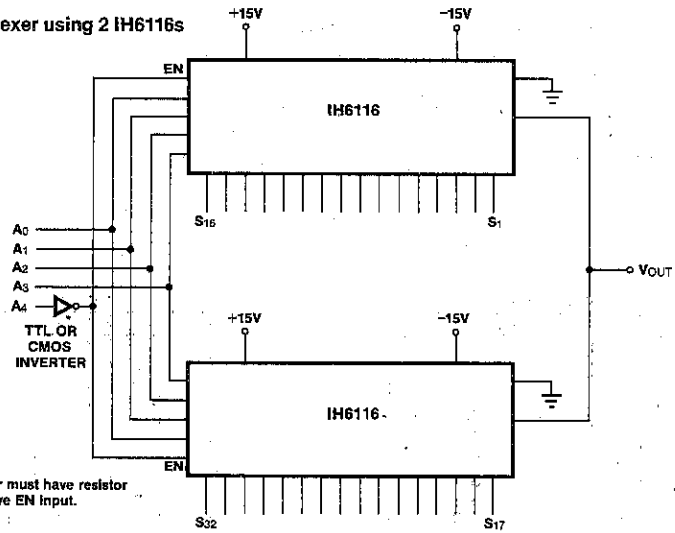


Figure 3

3

IH6116 APPLICATIONS

I. 1 out of 32 channel multiplexer using 2 IH6116s



*TTL inverter must have resistor pullup to drive EN input.

DECODE TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	ON SWITCH
0	0	0	0	0	S1
0	0	0	0	1	S2
0	0	0	1	0	S3
0	0	0	1	1	S4
0	0	1	0	0	S5
0	0	1	0	1	S6
0	0	1	1	0	S7
0	0	1	1	1	S8
0	1	0	0	0	S9
0	1	0	0	1	S10
0	1	0	1	0	S11
0	1	0	1	1	S12
0	1	1	0	0	S13
0	1	1	0	1	S14
0	1	1	1	0	S15
0	1	1	1	1	S16

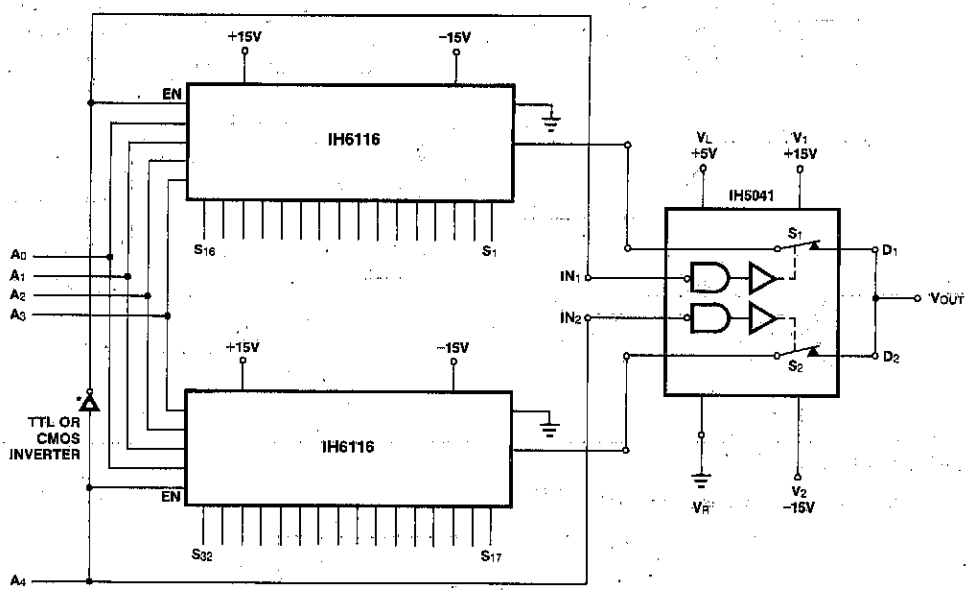
DECODE TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	ON SWITCH
1	0	0	0	0	S17
1	0	0	0	1	S18
1	0	0	1	0	S19
1	0	0	1	1	S20
1	0	1	0	0	S21
1	0	1	0	1	S22
1	0	1	1	0	S23
1	0	1	1	1	S24
1	1	0	0	0	S25
1	1	0	0	1	S26
1	1	0	1	0	S27
1	1	0	1	1	S28
1	1	1	0	0	S29
1	1	1	0	1	S30
1	1	1	1	0	S31
1	1	1	1	1	S32

Figure 4

IH6116 APPLICATIONS (Continued)

II. 1 out of 32 channel multiplexer using 2 IH6116s; using an IH5041 for submultiplexing



*TTL gate must have pullup resistor to +5V to drive EN inputs

DECODE TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	ON SWITCH
0	0	0	0	0	S1
0	0	0	0	1	S2
0	0	0	1	0	S3
0	0	0	1	1	S4
0	0	1	0	0	S5
0	0	1	0	1	S6
0	0	1	1	0	S7
0	0	1	1	1	S8
0	1	0	0	0	S9
0	1	0	0	1	S10
0	1	0	1	0	S11
0	1	0	1	1	S12
0	1	1	0	0	S13
0	1	1	0	1	S14
0	1	1	1	0	S15
0	1	1	1	1	S16

DECODE TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	ON SWITCH
1	0	0	0	0	S17
1	0	0	0	1	S18
1	0	0	1	0	S19
1	0	0	1	1	S20
1	0	1	0	0	S21
1	0	1	0	1	S22
1	0	1	1	0	S23
1	0	1	1	1	S24
1	1	0	0	0	S25
1	1	0	0	1	S26
1	1	0	1	0	S27
1	1	0	1	1	S28
1	1	1	0	0	S29
1	1	1	0	1	S30
1	1	1	1	0	S31
1	1	1	1	1	S32

Figure 5

IH6116 APPLICATIONS (Continued)

III. 1 out of 64 multiplexer using 4 1/16s and IH5053 as submultiplexer

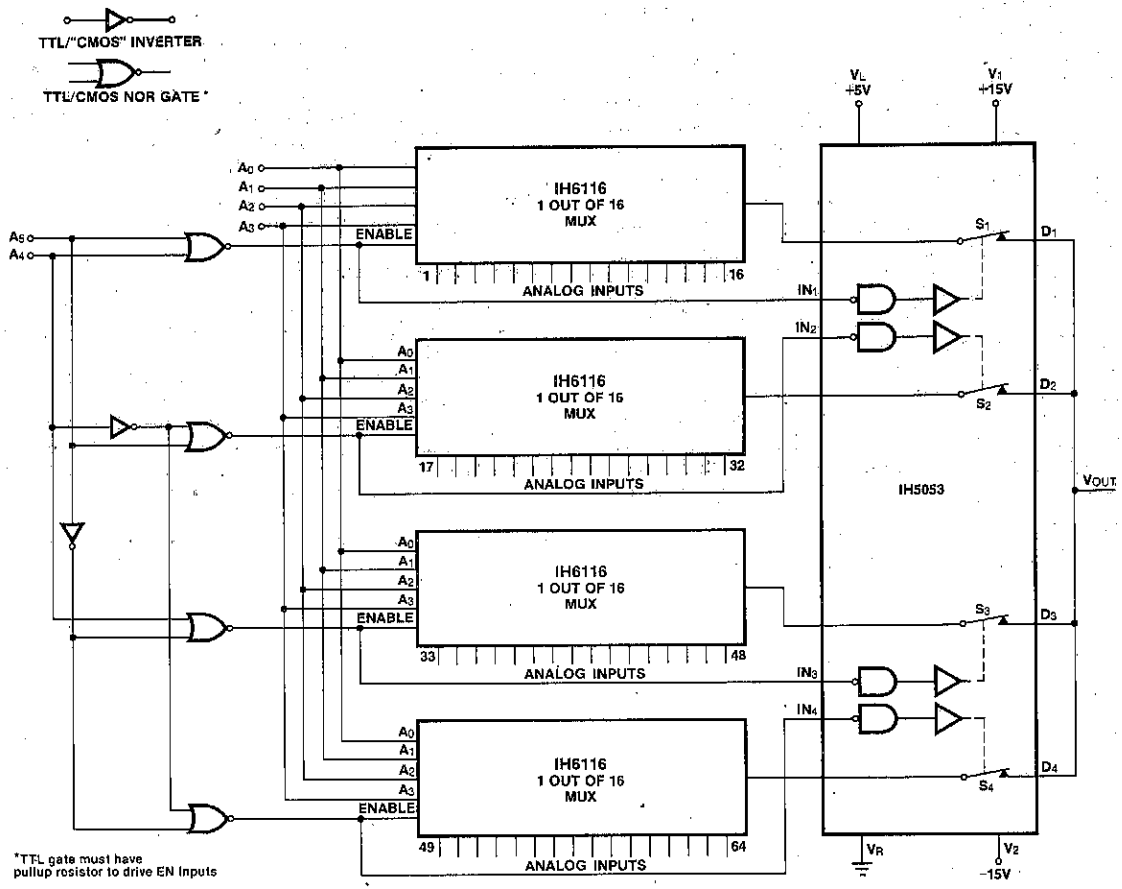


Figure 6

IV. General note on expandability of IH6116

The IH6116 is a two tier multiplexer, where sixteen input channels are routed to a common output in blocks of 4. Each block of 4 input channels is routed to one common output channel, and thus the submultiplexed system looks like 4 blocks of 4 inputs routed to 4 different outputs with the 4 outputs tied together. Thus 20 switches are needed to handle the 16 channels of information. The advantage of this is lower output capacity and leakage that would be possible using a system with all 16 channels tied to one common output. Also the expandability into 32, 64, 128, etc. is facilitated. Figures 4, 5, and 6 show how the IH6116 is expanded.

Figure 4 shows a 1 of 32 multiplexer, using 2 IH6116s. Since the 6116 is itself a 2 tier MUX, the system as shown is basically a 2 tier system. The four output channels of each 6116 are tied together so that 8 channels are tied to the V_{OUT} common point. Since only one channel of information is on at a time, the common output will consist of 7 OFF channels and 1 ON channel. Thus the output leakage will correspond to 7 $I_{D(offs)}$ and 1 $I_{D(on)}$, or about 1.0 nA of typical leakage at room temperature. Thruput speed will be typically 0.8μs for t_{on} and 0.3μs for t_{off}. Thruput channel resistance will be in the 500Ω area.

Figure 5 shows the 1 of 32 MUX of Figure 4, with a third tier of submultiplexing added to further reduce leakage and output capacity. The IH5041 has typical ON resistances of 50Ω (max. is 75Ω) so it only increases thruput channel resistance from the 500 ohms of Figure 4 to about 550 ohms for Figure 5. Thruput channel speed is a little slower by about 0.5μs for both ON and OFF time, and output leakage is about 0.2 nA.

3

Figure 6 shows a 1 of 64 MUX using 3 tier MUXing (similar to Figure 5). The Intersil IH5053 is used to get the third tier of MUXing. The V_{OUT} point will see 3 OFF channels and 1 ON channel at any one time, so that the typical leakages will be about 0.4 nA. Thruput channel resistance will be in the 550 ohm area with thruput switching speeds about 1.3μs for ON time and 0.8μs for OFF time.

The IH5053 was chosen as the third tier of the MUX because it will switch the same AC signals as the IH6116 (typically plus and minus 15V) and uses break before make switching. Also power supply quiescent currents are on the order of 1-2μA so that no excessive system power is generated. Note that the logic of the 5053 is such that it can be tied directly to the ENable input (as shown in the figures) with no extra logic being required.

V. Enable input strobing levels

The enable input (EN) acts as an enabling or disabling pin for the IH6116 when used as a 16 channel MUX. However, when expanding the MUX to more than 16 channels, the EN pin acts as another address input. Figures 4 and 5 show the EN pin used as the A4 input.

For the system to function properly the EN input (pin 18) must go to 5V±5% for the high state and less than 0.8V for the low state. When using TTL logic, a pull-up resistor of 1kΩ or less should be used to pull the output voltage up to 5V. When using CMOS logic, the high state goes to the power supply so no pull-up is required.

If used on high voltage logic supplies, EN should be at least 0.7V below V+ at all times. See IH6108 data sheet for details.

APPLICATION NOTES

Further information may be found in:

A003 "Understanding and Applying the Analog Switch," by Dave Fullagar

A006 "A New CMOS Analog Gate Technology," by Dave Fullagar

A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing," by Ed Slieger

R009 "Reduce CMOS Multiplexer Troubles Through Proper Device Selection," by Dick Wilenken

NOTE: This multiplexer does not require external resistors and/or diodes to eliminate what is commonly known as a latch up or SCR action. Because of this fact, the $r_{DS(ON)}$ of the switch is maintained at specified values.

IH6201
Dual CMOS Driver/ Voltage Translator

FEATURES

- **Driven direct from TTL or CMOS logic**
- **Translates logic levels up to 30V levels**
- **Switches 20V_{ACPP} signals when used in conjunction with Intersil IH401A Varafet (as an analog gate)**
- **$t_{ON} \leq 300nS$ & $t_{OFF} \leq 200nS$ for 30V level shifts**
- **Quiescent supply current $\leq 100\mu a$ for any state (d.c.)**
- **Provides both normal & inverted outputs**

GENERAL DESCRIPTION

The IH6201 is a CMOS, Monolithic, Dual Voltage Translator; it takes the low level TTL or CMOS logic level and converts them to higher levels (i.e. to ±15V swings). This translator is typically used in making solid state switches, or analog gates.

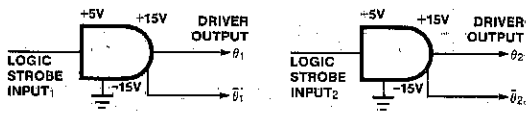
When used in conjunction with the Intersil IH401 family Varafets, the combination makes a complete solid state switch capable of switching signals up to 22Vpp and up to 20MHz in frequency. This switch is a "break-before-make" type (i.e. t_{off} time < t_{on} time). The combination has typical $t_{off} \approx 80nS$ and typ. $t_{on} \approx 200nS$ for signals up to 20Vpp in amplitude.

A TTL "1" input strobe will force the θ driver output up to V^+ level; the $\bar{\theta}$ output will be driven down to the V^- level. When the TTL input goes to "0", the θ output goes to V^- and $\bar{\theta}$ goes to V^+; thus θ and $\bar{\theta}$ are 180° out of phase with each other. These complementary outputs can be used to create a wide variety of functions such as SPDT and DPDT switches, etc.; alternatively the complementary outputs can be used to drive an N and P channel Mosfet, to make a complete Mosfet analog gate.

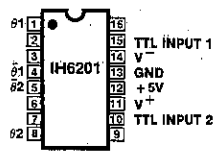
The driver typically uses +5V and ±15V power supplies; however a wide range of V^+ and V^- is possible, however $V^+ > 5V$ is necessary for the driver to work properly.

3

BLOCK DIAGRAM



PIN CONFIGURATION



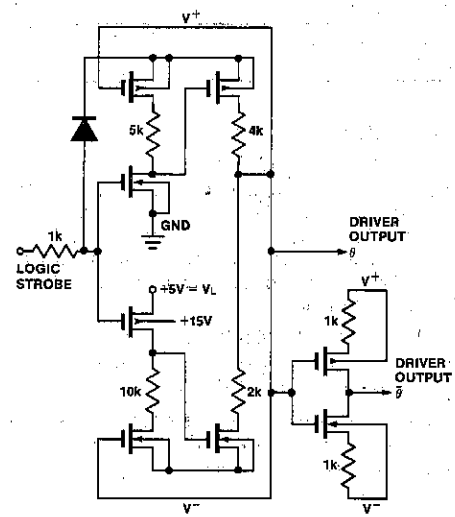
OUTLINE DWGS
DE, JE, PE

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE
*IH6201CDE	0°C to 70°C
*IH6201MDE	−55°C → +125°C
IH6201CJE	0°C to 70°C
IH6201MJE	−55°C to 125°C
IH6201CPE	0°C to 70°C

*Special Order Only

SCHEMATIC DIAGRAM (ONE CHANNEL)



ABSOLUTE MAXIMUM RATINGS

V^+ to V^- 35V
V^+ 35V
V^- 35V
V^+ to V_{IN} 40V

Operating Temperature ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL SPECIFICATIONS $V^+ = +15V$, $V^- = -15V$, $V_L = +5V$

ITEM	CONDITIONS	IH6201CDE			IH6201MDE			UNITS
		−25°C	+25°C	+85°C	−55°C	+25°C	+125°C	
θ or $\bar{\theta}$ driver output swing	V_{IN}=0V ⌐ +3V ¬ fig. 2B	28	28	28	28	28	28	Vpp
V_{IN} strobe level ("1") for proper translation	$\theta \geq 14V$ $\bar{\theta} \geq -14V$	3.0	3.0	3.0	2.4	2.4	2.4	$V_{D.C.}$
V_{IN} strobe level ("0") for proper translation	$\theta \geq -14V$ $\bar{\theta} \geq 14V$	0.4	0.4	0.4	0.8	0.8	0.8	$V_{D.C.}$
I_{IN} input strobe current draw (for 0V − 5V range)	V_{IN} = 0V or +5V	1	1	1	1	1	1	μA
t_{on} time	V_{IN}=0V ⌐ 3V / 4μS ¬ C_L = 30pf switching turn-on time fig. 2B	400	400	400	300	300	300	nS
t_{off} time	V_{IN}=0V ⌐ +3V / 4μS ¬ C_L = 30pf switching turn-off time fig. 2B	300	300	300	200	200	200	nS
I^+ (V^+) power supply quiescent current	V_{IN} = 0V or +5V	100	100	100	100	100	100	μA
I^- (V^-) power supply quiescent current	V_{IN} = 0V or +5V	100	100	100	100	100	100	μA
I_L (V_L) power supply quiescent current	V_{IN} = 0V or +5V	100	100	100	100	100	100	μA

APPLICATIONS

I. INPUT DRIVE CAPABILITY

The strobe input lines are designed to be driven from TTL logic levels; this means 0.8V − 2.4V levels max. and min. respectively. For those users who require 0.8V to 2.0V operation, a pull-up resistor is recommended from the TTL output to +5V line. This resistor is not critical and can be in the 1kΩ to 10kΩ range.

When using 4000 series CMOS logic, the input strobe is connected direct to the 4000 series gate output and no pull up resistors, or any other interface, is necessary.

When the input strobe voltage level goes below Gnd (i.e. to −15V) circuit is unaffected as long as V^+ to V_{IN} does not exceed absolute maximum rating.

II. OUTPUT DRIVE CAPABILITY

The translator output is designed to drive the Intersil IH401 family of Varafets; these are N-channel J-FETS with built-in driver diodes. Driver diodes are necessary to isolate the signal source from the driver/translator output; this prevents forward biasing between the signal input and the +Vcc supply. The IH6201 will drive any J-FET provided some sort of isolation is added i.e.

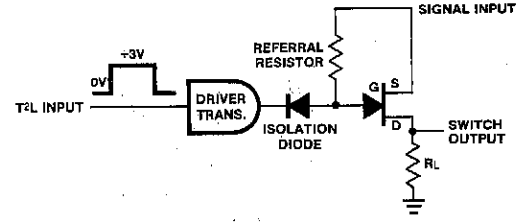


Figure 1

You will notice in Figure 1 that a "referral" resistor has been added from 2N4391 gate to its source. This resistor is needed to compensate for inadequate charge area curve for isolation diode (i.e. if C vs. V plot for diode ≤ 2 [C vs. V plot for output J-FET] switch won't function; then adding this resistor overcomes this condition. The "referral" resistor is normally in the 100kΩ to 1MΩ range and is not too critical.

III. MAKING A COMPLETE SOLID STATE SWITCH THAT CAN HANDLE 20Vpp SIGNALS

The limitation on signal handling capability comes from the output gating device. When a J-FET is used, it's the pinch-off of the J-FET acting with the V^- supply that does the

APPLICATIONS, CONTINUED

limiting. In fact max. signal handling capability = 2 (Vp + (V⁻)) Vpp where Vp = pinch-off voltage of J-FET chosen. i.e. Vp = 7V, V⁻ = −15V ∴ max. signal handling = 2 (7V + (−15V)) Vpp = 2(7V−15)pp=2(−8Vpp)=16Vpp. Obviously to get ≥ 20Vpp, Vp ≥ 5V with V⁻ = −15V. Another simple way to get 20Vpp with Vp = 7V, is to increase V⁻ to −17V. In fact using V⁺ = +12V or +15V and setting V⁻ = −18V allows one to switch 20Vpp with any member of IH401 family. The advantage of using the Vp = 7V pinch-off (along with unsymmetrical supplies) over the Vp = 5V pinch-off (and ±15V supplies) is that you will have a much lower $R_{DS(ON)}$ resistance for the Vp = 7V fet.(i.e. for the 2N4391 fet

$r_{DS(ON)} \approx 22\Omega$, $r_{DS(ON)} \approx 35\Omega$)
$V_p = 7V$ $V_p = 5V$

The IH6201 is a dual translator, each containing 4 CMOS FETs. The schematic of one-half IH6201, driving one-fourth of an IH401, is shown in Figure 2A.

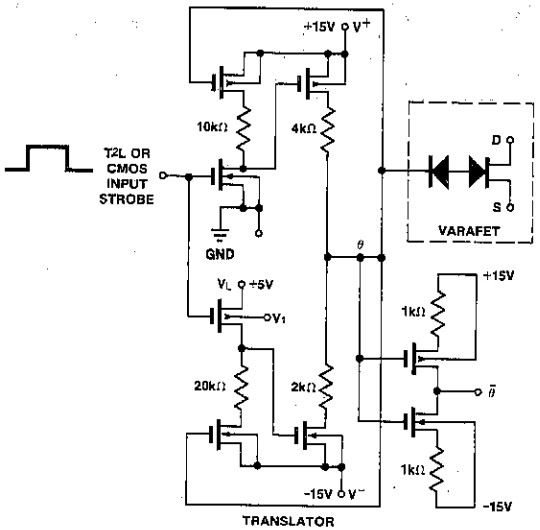
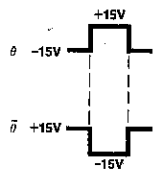


Figure 2A



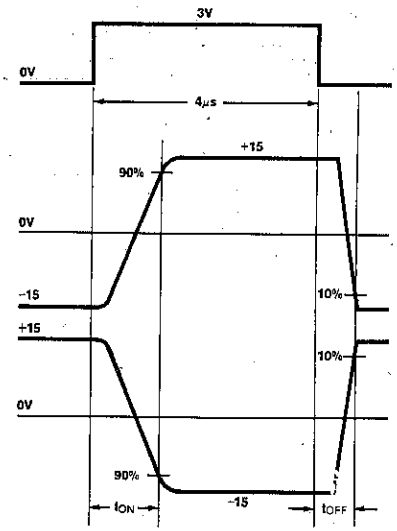
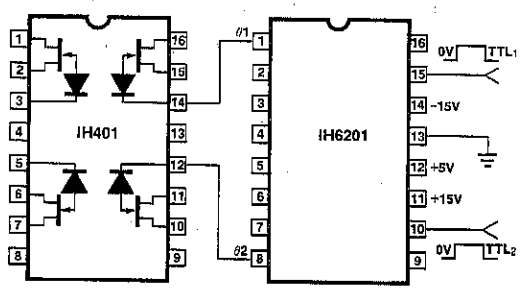


Figure 2B

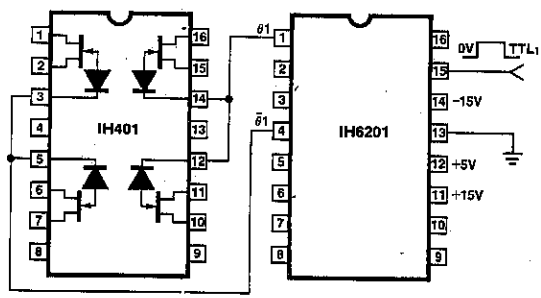
NOTE: Each translator output has a θ and $\bar{\theta}$ output. θ is just the inverse of $\bar{\theta}$.

A very useful feature of this system is that one-half of an IH6201 and one-half of an IH401 can combine to make a SPDT switch, or an IH6201 plus an IH401 can make a dual SPDT analog switch. (See III.)

I. Dual SPST Analog Switch



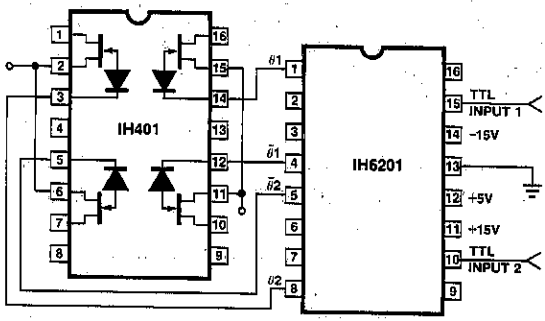
II. DPDT Analog Switch



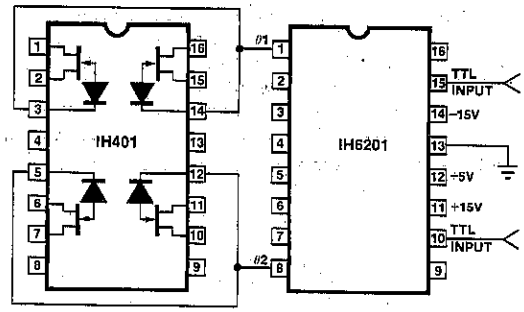
NOTE: Either switch is turned on when strobe input goes high.

APPLICATIONS, CONTINUED

III. Dual SPDT



IV. Dual DPST



3

IH6208

4-Channel Differential CMOS Analog Multiplexer

FEATURES

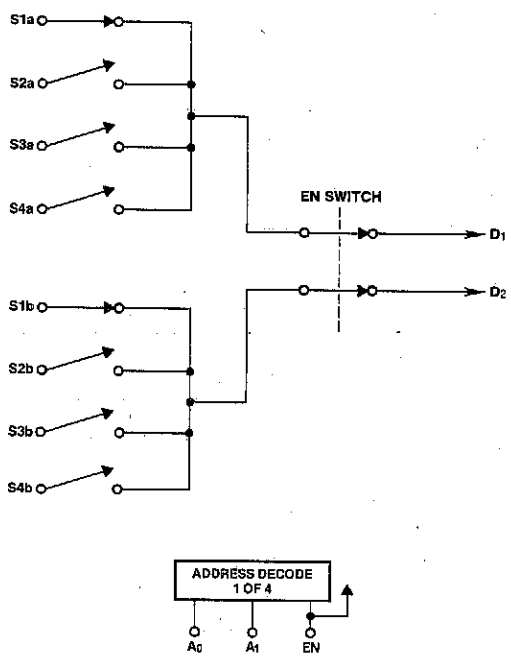
- **Ultra low leakage — $I_{D(off)} \leq 100pA$**
- **$r_{DS(on)} < 400$ ohms over full signal and temperature range**
- **Power supply quiescent current less than 100μA**
- **$\pm$14V analog signal range**
- **No SCR latch up**
- **Break-before-make switching**
- **Binary Address control (2 Address inputs control 2 out of 8 channels)**
- **TTL and CMOS compatible Address control**
- **Pin compatible with HI509, DG509 & AD7509**

GENERAL DESCRIPTION

The IH6208 is a monolithic 2 of 8 CMOS multiplexer. The part is a plug-in replacement for the DG509. Two line binary decoding is used so that the 8 channels can be controlled in pairs by the binary inputs; additionally a third input is provided to use as a system enable. When the ENable input is high (5V) the channels are sequenced by the 2 line binary inputs, and when low (0V) all channels are off. The 2 Address inputs are controlled by TTL logic or CMOS logic elements with a "0" corresponding to any voltage less than 0.8V and a "1" corresponding to any voltage greater than 2.4V. Note that the ENable input must be taken to 5V to enable the system, and less than 0.8V to disable the system.

3

FUNCTIONAL DIAGRAM



2 LINE BINARY ADDRESS INPUTS
(0 0) AND EN = 5V (EN = "1" FOR +5V, "0" FOR 0V)
ABOVE EXAMPLE SHOWS CHANNELS 1a & 1b ON.

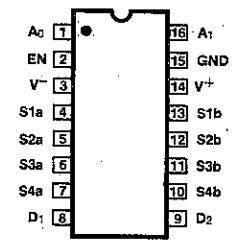
DECODE TRUTH TABLE

A_1	A_0	EN	ON SWITCH PAIR
X	X	0	NONE
0	0	1	1a, 1b
0	1	1	2a, 2b
1	0	1	3a, 3b
1	1	1	4a, 4b

A_0, A_1

LOGIC "1" = $V_{AH} \geq 2.4V$ $V_{ENH} \geq 4.5V$
LOGIC "0" = $V_{AL} \leq 0.8V$

PIN CONFIGURATION



ORDERING INFORMATION

Ceramic package available as special order only (IH6208MDE/CDE)

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH6208MJE	−55°C to +125°C	16 pin CERDIP
IH6208CJE	0°C to 70°C	16 pin CERDIP
IH6208CPE	0°C to 70°C	16 pin Plastic DIP

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground ..... −15V, V_1
V_S or V_D to V^+ ..... 0, −32V
V_S or V_D to V^- 0, 32V
V^+ to Ground 16V
V^- to Ground ..... −16V
Current (Any Terminal) ..... 30 mA
Current (Analog Source or Drain) ..... 20 mA
Operating Temperature ..... −55 to 125°C
Storage Temperature ..... −65 to 150°C
Lead Temp (Soldering, 10 sec) ..... 300°C
Power Dissipation (Package)* ..... 1200 mW

*All leads soldered or welded to PC board. Derate 10 mW/°C above 70°C.

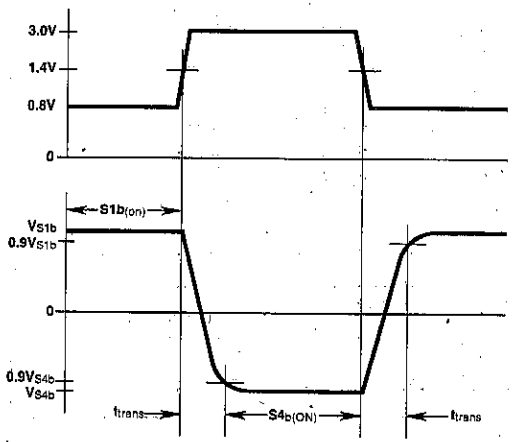
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS $V^+ = 15V$, $V^- = -15V$, $V_{EN} = +5V$ (Note 1), Ground = 0V, unless otherwise specified.

	CHARACTERISTIC		MEASURED TERMINAL	NO TESTS PER TEMP	TYP 25°C	MAX LIMITS M SUFFIX −55°C	M SUFFIX 25°C	M SUFFIX 125°C	C SUFFIX 0°C	C SUFFIX 25°C	C SUFFIX 70°C	UNIT	TEST CONDITIONS	
SWITCH	$r_{DS(ON)}$		S to D	8	180	300	300	400	350	350	450	Ω	$V_D = 10V$, $I_S = -1.0$ mA	Sequence each switch on
				8	150	300	300	400	350	350	450		$V_D = -10V$, $I_S = -1.0$ mA	$V_{AL} = 0.8V$, $V_{AH} = 2.4V$
	$\Delta r_{DS(ON)}$				20							%	$\Delta r_{DS(on)} = \frac{r_{DS(on)max} - r_{DS(on)min}}{r_{DS(on)avg.}}$	$V_S = \pm 10V$
	$I_{S(OFF)}$		S	8	0.002		0.05	50		0.1	50	nA	$V_S = 10V$, $V_D = -10V$	$V_{EN} = 0$
				8	0.002		0.05	50		0.1	50		$V_S = -10V$, $V_D = 10V$	
	$I_{D(OFF)}$		D	2	0.03		0.1	50		0.2	100		$V_D = 10V$, $V_S = -10V$	
				2	0.03		0.1	50		0.2	100		$V_D = -10V$, $V_S = 10V$	
	$I_{D(ON)}$		D	8	0.1		0.2	50		0.4	100		$V_{S(All)} = V_D = 10V$	Sequence each switch on
				8	0.1		0.2	50		0.4	100		$V_{S(All)} = V_D = -10V$	$V_{AL} = 0.8V$, $V_{AH} = 2.4V$
INPUT	$I_{A(on)}$			2	.01		−10	−30		−10	−30	μA	$V_A = 2.4V$ or 0V	
	$I_{A(off)}$			2	.01		10	30		10	30		$V_A = 15V$ or 0V	
	I_A		A0, A1	2			−10	−30		−10	−30		$V_{EN} = 5V$	All $V_A = 0$
			EN	1			−10	−30		−10	−30		$V_{EN} = 0$	(Address Pins)
DYNAMIC	t_{trans}		D		0.3		1					μs	See Fig. 1	
	t_{open}		D		0.2								See Fig. 2	
	$t_{EN(on)}$		D		0.6		1.5						See Fig. 3	
	$t_{EN(off)}$		D		0.4		1							
	"OFF" Isolation		D		60							dB	$V_{EN} = 0$, $R_L = 200\Omega$, $C_L = 3$ pF, $V_S = 3$ VRMS, f = 500 kHz	
	$C_{S(off)}$		S		5							pF	$V_S = 0$	$V_{EN} = 0$, f = 140 kHz to 1 MHz
	$C_{D(off)}$		D		12								$V_D = 0$	
	$C_{DS(off)}$		D to S		1								$V_S = 0$, $V_D = 0$	
SUPPLY	Supply Current	+	V^+	1	40		200			1000		μA	$V_{EN} = 5V$	All $V_A = 0$ or 5V
		−	V^-	1	2		100			1000				
	Standby Current	+	V^+	1	1		100			1000			$V_{EN} = 0$	
		−	V^-	1	1		100			1000				

NOTE 1: See Section I Enable Input Strobing Levels.

SWITCHING INFORMATION



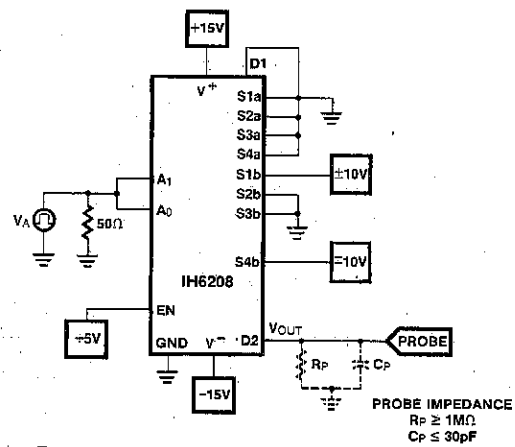


Figure 1. t_{trans} Switching Test

SWITCHING INFORMATION (Continued)

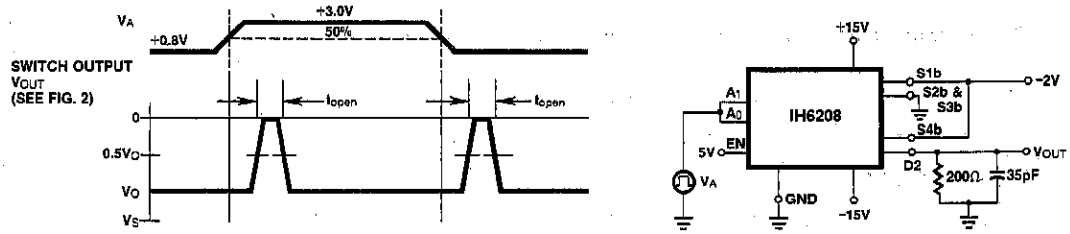


Figure 2. t_{open} (Break-Before-Make) Switching Test

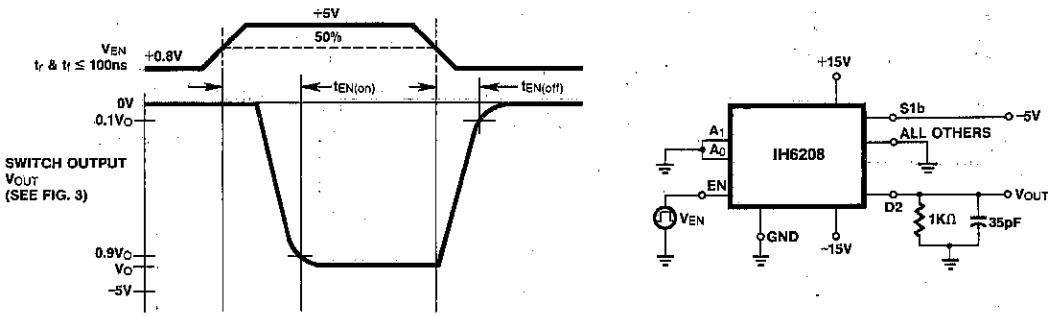


Figure 3. t_{on} and t_{off} Switching Test

IH6208 APPLICATION INFORMATION

I. ENable Input Strobing Levels

The ENable input on the IH6208 requires a minimum of +4.5V to trigger it into the "1" state and a maximum of +0.8V to trigger it into the "0" state. If the ENable input is being driven from TTL logic, a pull-up resistor of 1k to 3kΩ is required from the gate output to +5V supply. (See Figure 4).

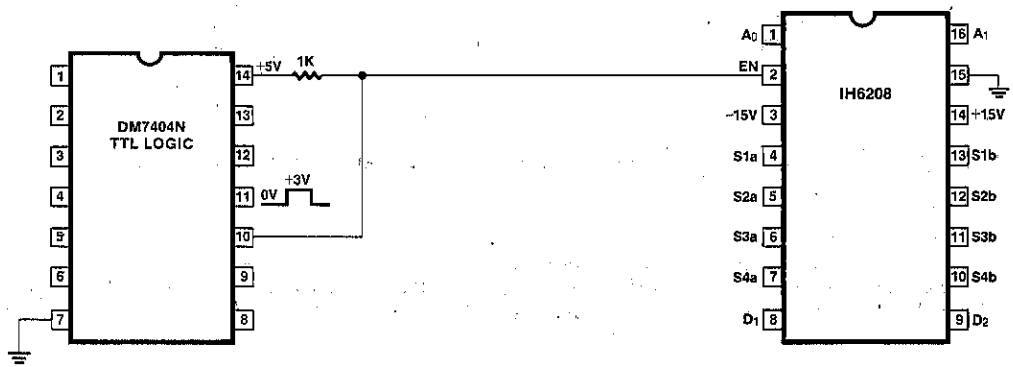


Figure 4. ENable Input Strobing from TTL Logic

IH6208 APPLICATION INFORMATION (Continued)

When the EN input is driven from CMOS logic, no pullup is necessary. (See Fig. 5)

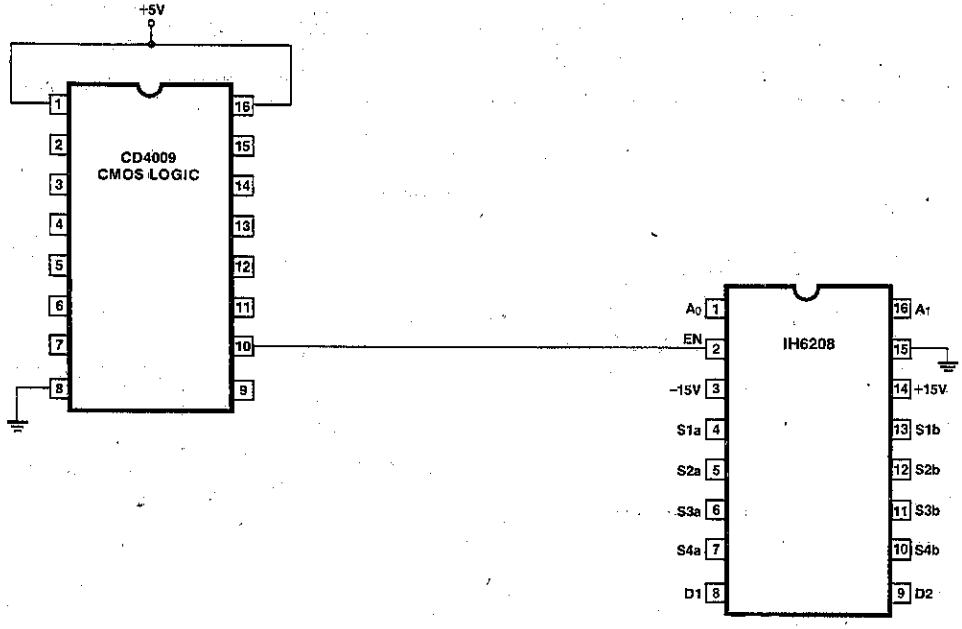


Figure 5. CMOS Logic Driving ENable Pin.

The supply voltage of the CD4009 affects the switching speed of the IH6208; the same is true for TTL supply voltage levels. The chart below shows the effect on t_{trans} for a supply varying from +4.5V to +5.5V.

CMOS OR TTL SUPPLY	TYPICAL t_{trans} @ 25°C
+4.5V	400ns
+4.75V	300ns
+5.0V	250ns
+5.25V	200ns
+5.50V	175ns

The throughput rate can therefore be maximized by using a +5V to +5.5V supply for the ENable Strobe Logic.

The examples shown in Figures 4 and 5 deal with ENable strobing when expansion to more than four differential channels is required; in these cases the EN terminal acts as a third address input. If four channel pairs or less are being multiplexed, the EN terminal can be directly connected to +5V to enable the IH6208 at all times.

II. Using the IH6208 with supplies other than ±15V

The IH6208 can be used with power supplies ranging from ±6V to ±16V. The switch $r_{DS(on)}$ will increase as the supply voltages decrease, however the multiplexer error term (the product of leakage times $r_{DS(on)}$) will remain approximately constant since leakage decreases as the supply voltages are reduced.

Caution must be taken to ensure that the enable (EN) voltage is at least 0.7V below V^+ at all times. If this is not done the Address input strobing levels will not function properly. This may be achieved quite simply by connecting EN (pin 2) to V^+ (pin 14) via a silicon diode as shown in Figure 6. A further requirement must be met when using this type of configuration; the strobe levels at A0 and A1 must be within 2.5V of the EN voltage in order to define a binary "1" state. For the case shown in Figure 6 the EN voltage is 11.3V, which means that logic high at A0 and A1 is = +8.8V (logic low continues to be = 0.8V). In this configuration the IH6208 cannot be driven by TTL (+5V) or CMOS (+5V) logic. It can be driven by TTL open collector logic or CMOS logic with +12V supplies.

If the logic and the IH6208 have common supplies, the EN pin should again be connected to the supply through a silicon diode. In this case, tying EN to the logic supply directly will not work since it violates the 0.7V differential voltage required between V^+ and EN (See Figure 7). A 1μF capacitor can be placed across the diode to minimize switching glitches.

3

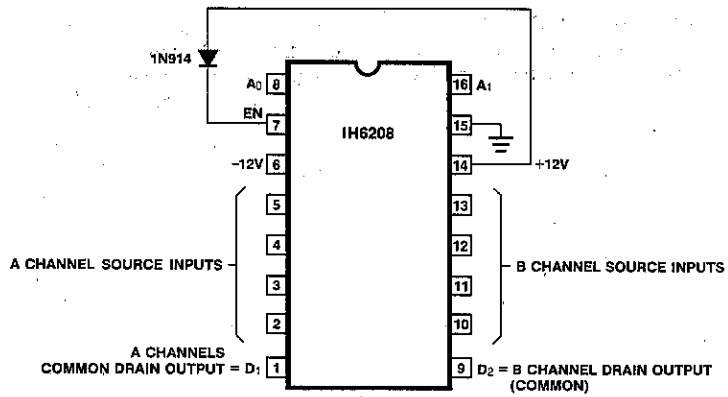


Figure 6. IH6208 Connection Diagram for less than ±15V Supply Operation.

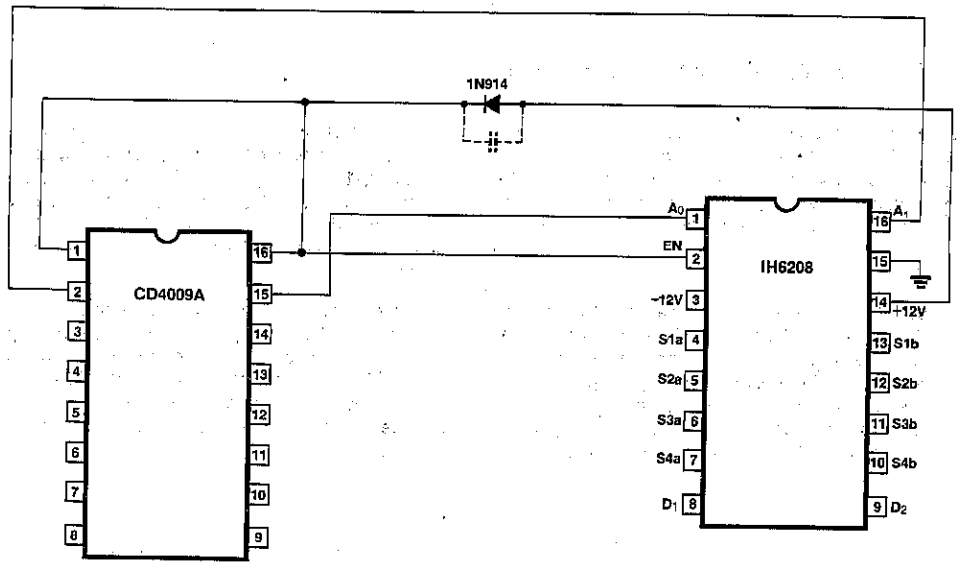


Figure 7. IH6208 Connection Diagram with ENable Input Strobing for less than ±15V Supply Operation.

III. Peak-to-Peak Signal Handling Capability

The IH6208 can handle input signals up to ±14V (actually −15V to +14.3V because of the input protection diode) when using ±15V supplies.

The electrical specifications of the IH6208 are guaranteed for ±10V signals, but the specifications have very minor changes for ±14V signals. The notable changes are slightly lower $r_{DS(on)}$ and slightly higher leakages.

IH6216

8-Channel Differential CMOS Analog Multiplexer

FEATURES

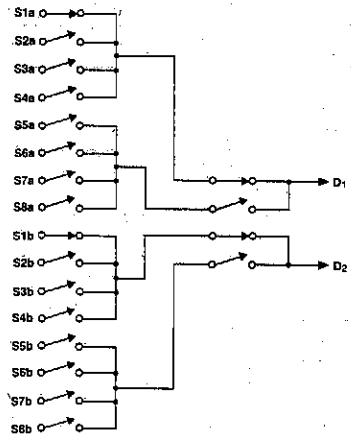
- **Pin compatible with HI507, DG507 & AD7507**
- **±11V analog signal range**
- **$r_{DS(on)}$ < 700 ohms over full signal and temperature range**
- **Break-before-make switching**
- **TTL and CMOS compatible Address control**
- **Binary Address control (3 Address inputs control 2 out of 16 channels)**
- **Two tier submultiplexing to facilitate expandability**
- **Power supply quiescent current less than 100μA**
- **No SCR latch up**
- **Very low leakage $I_{D(off)} \leq$ 100pA**

GENERAL DESCRIPTION

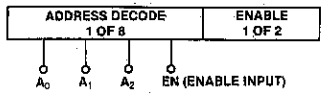
The IH6216 is a CMOS monolithic 2 of 16 multiplexer. The part is a plug-in replacement for the DG507. Three line binary decoding is used so that the 16 channels can be controlled in pairs by the binary inputs; additionally a fourth input is provided to use as a system enable. When the ENable input is high (5V) the channels are sequenced by the 3 line binary inputs, and when low (0V) all channels are off. The 3 Address inputs are controlled by TTL logic or CMOS logic elements with a "0" corresponding to any voltage less than 0.8V and a "1" corresponding to any voltage greater than 3.0V. Note that the ENable input must be taken to 5V to enable the system and less than 0.8V to disable the system.

3

FUNCTIONAL DIAGRAM



TO DECODE LOGIC CONTROLLING BOTH TIERS OF MUXING



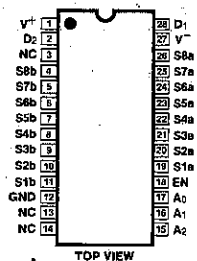
3 LINE BINARY ADDRESS INPUTS (0 0 0) AND EN = 5V ABOVE EXAMPLE SHOWS CHANNELS 1a & 1b ON.

DECODE TRUTH TABLE

A_2	A_1	A_0	EN	ON SWITCH PAIR
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

LOGIC "1" = V_{AH} > 3V V_{ENH} > 4.5V
LOGIC "0" = V_{AL} < 0.8V

PIN CONFIGURATION



TOP VIEW
V^+ COMMON TO SUBSTRATE

ORDERING INFORMATION

Ceramic package available as special order only (IH6216MDI/CDI)

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH6216MJI	−55°C to +125°C	28 pin CERDIP
IH6216CJI	0°C to 70°C	28 pin CERDIP
IH6216CPI	0°C to 70°C	28 pin Plastic DIP

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground ..... −15V, V_1
V_S or V_D to V^+ ..... 0, −32V
V_S or V_D to V^- 0, 32V
V^+ to Ground 16V
V^- to Ground ..... −16V
Current (Any Terminal) ..... 30 mA
Current (Analog Source or Drain) ..... 20 mA

Operating Temperature ..... −55 to 125° C
Storage Temperature ..... −65 to 150° C
Power Dissipation (Package)* 1200mW
Lead Temperature (Soldering 10 sec) ..... 300 °C

*All leads soldered or welded to PC board. Derate 10 mW/° C above 70° C

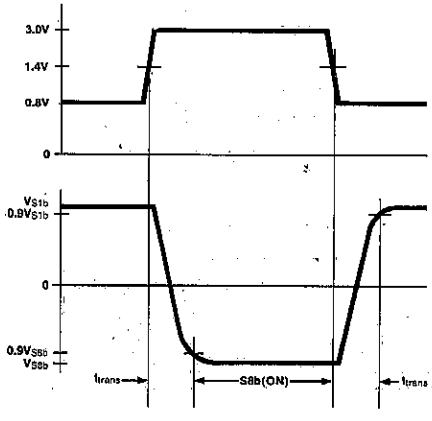
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

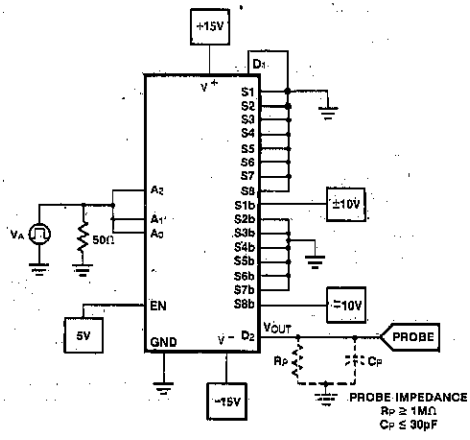
ELECTRICAL CHARACTERISTICS $V^+ = 15V$, $V^- = -15V$, $V_{EN} = +5V$ (Note 1), Ground = 0V, unless otherwise specified.

	CHARACTERISTIC		MEASURED TERMINAL	NO TESTS PER TEMP	TYP 25°C	MAX LIMITS M SUFFIX −55°C	M SUFFIX 25°C	M SUFFIX 125°C	C SUFFIX 0°C	C SUFFIX 25°C	C SUFFIX 70°C	UNIT	TEST CONDITIONS	
SWITCH	$r_{DS(ON)}$		S to D	16	480	600	600	700	650	650	750	Ω	$V_D = 10V$, $I_S = -10mA$	Sequence each switch on
				16	300	600	600	700	650	650	750		$V_D = -10V$, $I_S = 10mA$	$V_{AL} = 0.8V$, $V_{AH} = 3V$
	$\Delta r_{DS(ON)}$				20							%	$\Delta r_{DS(on)} = \frac{r_{DS(on)max} - r_{DS(on)min}}{r_{DS(on)avg.}}$ $V_S = \pm 10V$	
	$I_{S(OFF)}$		S	16	0.01		0.1	50		0.2	50	nA	$V_S = 10V$, $V_D = -10V$	$V_{EN} = 0$
				16	0.01		0.1	50		0.2	50		$V_S = -10V$, $V_D = 10V$	
	$I_{D(OFF)}$		D	2	0.1		0.2	100		0.4	100		$V_D = 10V$, $V_S = -10V$	
				2	0.1		0.2	100		0.4	100		$V_D = -10V$, $V_S = 10V$	
	$I_{D(ON)}$		D	16	0.1		0.2	100		0.4	100		$V_{S(All)} = V_D = 10V$	Sequence each switch on
				16	0.1		0.2	100		0.4	100		$V_{S(All)} = V_D = -10V$	$V_{AL} = 0.8V$, $V_{AH} = 3V$
INPUT	$I_{A(on)}$ or $I_{A(off)}$			3	.01		−10	−30		−10	−30	μA	$V_A = 3.0V$	
				3	.01		10	30		10	30		$V_A = 15V$	
	I_A		A_0 A_1 A_2 A_3	3			−10	−30		−10	−30		$V_{EN} = 5V$	All $V_A = 0$
			EN	1			−10	−30		−10	−30		$V_{EN} = 0$	
DYNAMIC	t_{trans}		D		0.6		1					μs	See Fig. 1	
	t_{open}		D		0.2								See Fig. 2	
	$t_{on(EN)}$		D		0.8		1.5						See Fig. 3	
	$t_{off(EN)}$		D		0.3		1							
	"OFF" Isolation		D		60							dB	$V_{EN} = 0$, $R_L = 200\Omega$, $C_L = 3$ pF, $V_S = 3$ VRMS, f = 500 kHz	
	C_S		S		5							pF	$V_S = 0$	$V_{EN} = 0$, f = 140 kHz to 1 MHz
	$C_{d(off)}$		D		20								$V_D = 0$	
	C_{ds}		D to S		1								$V_S = 0$, $V_D = 0$	
SUPPLY	Supply Current	+	V^+	1	55		200			1000		μA	$V_{EN} = 5V$	All $V_A = 0$ or 3V
		−	V^-	1	2		100			1000				
	Standby Current	+	V^+	1	1		100			1000			$V_{EN} = 0$	
		−	V^-	1	1		100			1000				

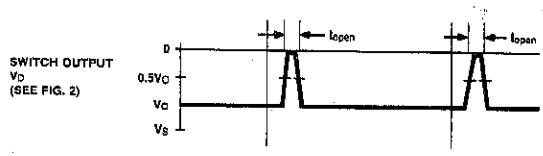
NOTE 1: See Section V. Enable Input Strobing Levels.

SWITCHING INFORMATION





SWITCHING INFORMATION (Continued)



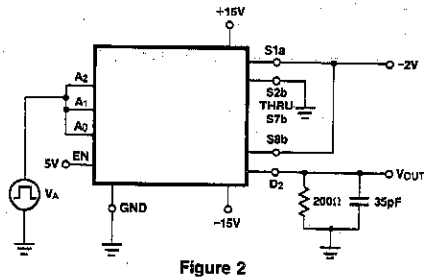
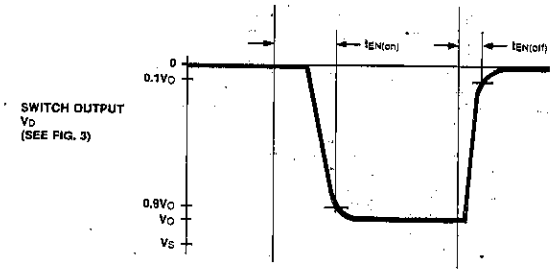


Figure 2



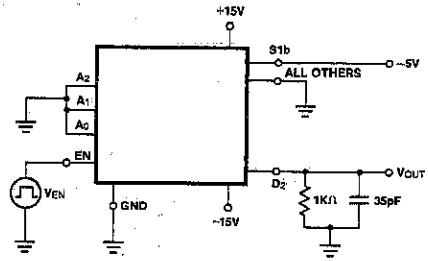
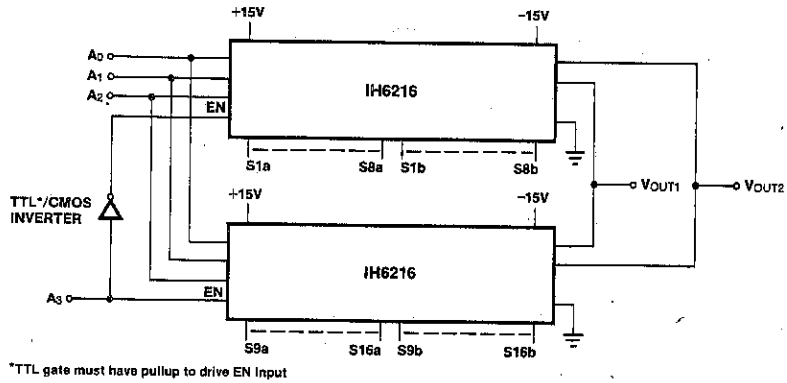


Figure 3

IH6216 APPLICATIONS

1. 2 out of 32 channel multiplexer using 2 IH6216s



*TTL gate must have pullup to drive EN input

Figure 4

DECODE TRUTH TABLE

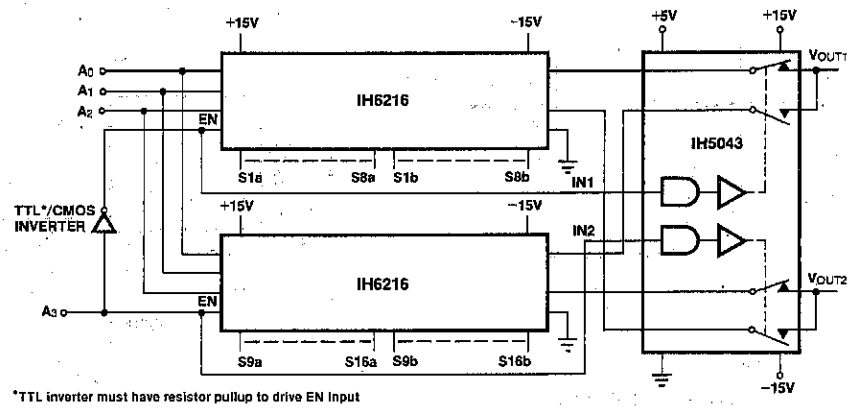
A3	A2	A1	A0	ON SWITCH	
0	0	0	0	S1a	
0	0	0	1	S2a	
0	0	1	0	S3a	
0	0	1	1	S4a	
0	1	0	0	S5a	
0	1	0	1	S6a	
0	1	1	0	S7a	
0	1	1	1	S8a	VOUT1
1	0	0	0	S9a	
1	0	0	1	S10a	
1	0	1	0	S11a	
1	0	1	1	S12a	
1	1	0	0	S13a	
1	1	0	1	S14a	
1	1	1	0	S15a	
1	1	1	1	S16a	

DECODE TRUTH TABLE

A3	A2	A1	A0	ON SWITCH	
0	0	0	0	S1b	
0	0	0	1	S2b	
0	0	1	0	S3b	
0	0	1	1	S4b	
0	1	0	0	S5b	
0	1	0	1	S6b	
0	1	1	0	S7b	
0	1	1	1	S8b	VOUT2
1	0	0	0	S9b	
1	0	0	1	S10b	
1	0	1	0	S11b	
1	0	1	1	S12b	
1	1	0	0	S13b	
1	1	0	1	S14b	
1	1	1	0	S15b	
1	1	1	1	S16b	

IH6216 APPLICATIONS (Continued)

II. 2 out of 32 channel multiplexer using 2 IH6216s; with an IH5043 for submultiplexing



*TTL inverter must have resistor pullup to drive EN input

Figure 5

DECODE TRUTH TABLE

A_3	A_2	A_1	A_0	ON SWITCH	
0	0	0	0	S1a	
0	0	0	1	S2a	
0	0	1	0	S3a	
0	0	1	1	S4a	
0	1	0	0	S5a	
0	1	0	1	S6a	
0	1	1	0	S7a	
0	1	1	1	S8a	V_{OUT1}
1	0	0	0	S9a	
1	0	0	1	S10a	
1	0	1	0	S11a	
1	0	1	1	S12a	
1	1	0	0	S13a	
1	1	0	1	S14a	
1	1	1	0	S15a	
1	1	1	1	S16a	

DECODE TRUTH TABLE

A_3	A_2	A_1	A_0	ON SWITCH	
0	0	0	0	S1b	
0	0	0	1	S2b	
0	0	1	0	S3b	
0	0	1	1	S4b	
0	1	0	0	S5b	
0	1	0	1	S6b	
0	1	1	0	S7b	
0	1	1	1	S8b	V_{OUT2}
1	0	0	0	S9b	
1	0	0	1	S10b	
1	0	1	0	S11b	
1	0	1	1	S12b	
1	1	0	0	S13b	
1	1	0	1	S14b	
1	1	1	0	S15b	
1	1	1	1	S16b	

IH6216 APPLICATIONS

III. 2 out of 64 multiplexer using 4 IH6216s and 2 IH5043s as submultiplexers

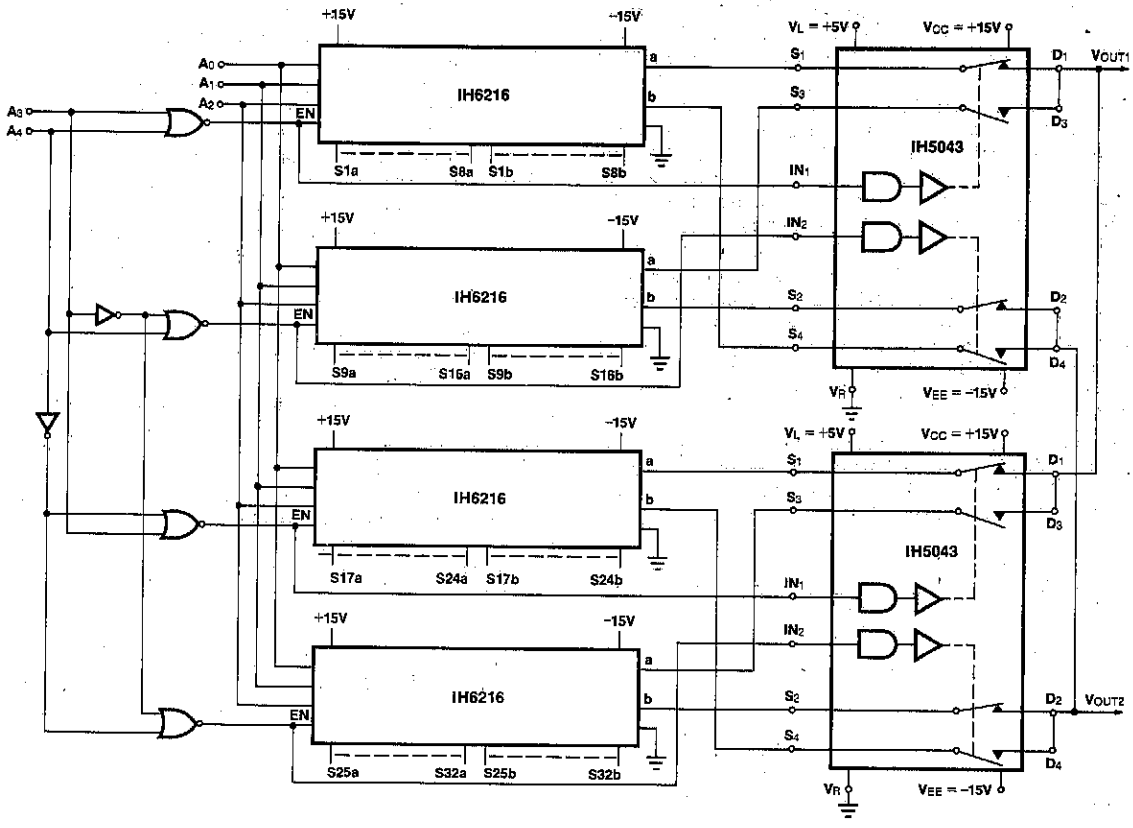


Figure 6

General note on expandability of IH6216

The IH6216 is a two tier multiplexer where 8 pairs of input channels are routed to a pair of outputs in blocks of 4. Each block of 4 input channels is routed to one common output channel, and thus the submultiplexed system looks like 4 blocks of 4 inputs routed to 4 different outputs with the 4 outputs tied in pairs. Thus 20 switches are needed to handle the 16 channels of information. The advantages of this are lower output capacity and leakage than would be possible using a system with all 8 channels tied to one common output. Also the expandability into 2 out of 32, 64, 128, etc. is facilitated. Figures 4, 5, and 6 show how the IH6216 is expanded.

Figure 4 shows a 2 of 32 multiplexer using 2 IH6216s. Since the 6216 is itself a 2 tier MUX, the system as shown is basically a 2 tier system. Corresponding output points of each of the 6216 are connected together, and the ENable input strobe is used as the A_3 input. Since each output (pins 2 and 28) corresponds to an "ON" FET and an "OFF" FET, the overall system looks like 1 "ON" FET and 3 "OFF" FETs for each of the V_{out1} and V_{out2} outputs. Thus the output leakage will be 1 $I_{D(on)}$ plus 3 $I_{D(off)}$s or about 0.4 nA at room temperature. Thruput speed will be typically 0.8μs for t_{on} and 0.3μs for t_{off}, with thruput channel resistance in the 500Ω area.

Figure 5 shows the 2 of 32 MUX of Figure 4, with a third tier of submultiplexing added to further reduce leakage and output capacity. The IH5043 has typical ON resistance of 50Ω (max. is 75Ω) so it only increases thruput channel resistance from the 500 ohms of Figure 4 to about 550 ohms for Figure 5. Thruput channel speed is a little slower by about 0.5μs for both ON and OFF time, and output leakage is about 0.2 nA.

Figure 6 shows a 2 of 64 MUX using 3 tier MUXing (similar to Figure 5). The Intersil IH5043 is used for the third tier of MUXing. Each V_{out} point will see 3 OFF channels and 1 ON channel at any time, so that the typical leakages will be about 0.4 nA. Thruput channel resistance will be in the 550Ω area and thruput switching speeds will be about 1.3μs for ON time and 0.8μs for OFF time.

The IH5043 was chosen as the third tier of the MUX because it will switch the same AC signals as the IH6216 (typically plus and minus 15V) and uses break before make switching. Also power supply quiescent currents are typically 1–2μA so that no excessive system power is generated. Note that the logic of the 5043 is such that it can be tied directly to the ENable input (as shown in the figures) with no extra logic being required.

V. Enable input strobing levels

The ENable input acts as an enabling or disabling pin for the IH6216 when used as a 2 out of 16 channel MUX, however when expanding the MUX to more than 16 channels, the EN pin acts as another address input. Figures 4 and 5 show the EN pin used as the A_3 input.

For the system to function properly the EN input (pin 18) must go to 5V ±5% for the high state and less than 0.8V for the low state. When using TTL logic, a pull-up of 1kΩ or less resistor should be used to pull the output voltage up to 5V. When using CMOS logic, the high state goes up to the power supply so no pull-up is required.

If used on high voltage logic supplies, EN should be at least 0.7V below V^+ at all times. See IH6208 data sheet for details.

APPLICATION NOTES

Further information may be found in:

A003 "Understanding and Applying the Analog Switch," by Dave Fullagar

A006 "A New CMOS Analog Gate Technology," by Dave Fullagar

A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing," by Ed Slieger

R009 "Reduce CMOS Multiplexer Troubles Through Proper Device Selection," by Dick Wilenken

NOTE: This multiplexer does not require external resistors and/or diodes to eliminate what is commonly known as a latch up or SCR action. Because of this fact, the $r_{DS(ON)}$ of the switch is maintained at specified values.