Low-Voltage, Low R_{ON}, Dual DPDT Analog Switch

DESCRIPTION

The DG2015 is a dual double-pole/double-throw monolithic CMOS analog switch designed for high performance switching of analog signals. Combining low power, high speed, low on-resistance and small physical size, the DG2015 is ideal for portable and battery powered applications requiring high performance and efficient use of board space.

The DG2015 is built on Vishay Siliconix's low voltage JI2 process. An epitaxial layer prevents latchup. Break-before-make is guaranteed.

The switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

FEATURES

- **Halogen-free according to IEC 61249-2-21 Definition**
- Low Voltage Operation (2.7 V to 3.3 V)
- Low On-Resistance - R_{ON}: 0.85 Ω
- 3 dB Loss at 100 MHz
- Fast Switching: t_{ON} = 40 ns, t_{OFF} = 35 ns
- QFN-16 Package
- **Compliant to RoHS Directive 2002/95/EC**

Pb-free
RoHS COMPLIANT
HALOGEN FREE

BENEFITS

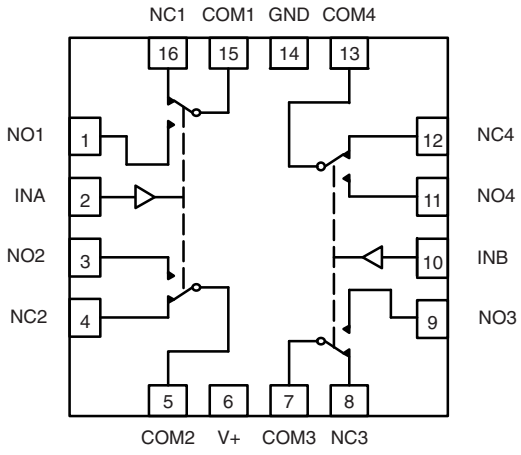
- Reduced Power Consumption
- High Accuracy
- Reduced Board Space
- Reduce Board Space
- TTL/1.8 V Logic Compatible

APPLICATIONS

- Cellular Phones
- Speaker Headset Switching
- Audio and Video Signal Routing
- PCMCIA Cards
- Battery Operated Systems

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG2015
QFN-16 (4 x 4)



Top View

TRUTH TABLE

Logic	NC1, 2, 3 and 4	NO1, 2, 3 and 4
0	ON	OFF
1	OFF	ON

ORDERING INFORMATION

Temp Range	Package	Part Number
- 40 °C to 85 °C	16-pin QFN (4 mm x 4 mm)	DG2015DN-T1-E4

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ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)			
Parameter		**Limit**	**Unit**
Reference V+ to GND		- 0.3 to + 6	V
IN, COM, NC, NO[a]		- 0.3 to (V+ + 0.3)	
Current (Any terminal except NO, NC or COM)		30	mA
Continuous Current (NO, NC, or COM)		± 150	
Peak Current (Pulsed at 1 ms, 10 % duty cycle)		± 200	
Storage Temperature (D Suffix)		- 65 to 150	°C
Package Solder Reflow Conditions[d]	16-pin QFN (4 mm x 4 mm)	240	
Power Dissipation (Packages)[b]	QFN-16[c]	1880	mW

Notes:
a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 23.5 mW/°C above 70 °C.
d. Manual soldering with iron is not recommended for leadless components. The QFN is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper lip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

SPECIFICATIONS (V+ = 3 V)

Parameter	**Symbol**	**Test Conditions Otherwise Unless Specified** V+ = 3 V, ± 10 %, V_{IN} = 0.4 V or 2 V[e]	**Temp.[a]**	**Limits - 40 °C to 85 °C** **Min.[b]**	**Typ.[c]**	**Max.[b]**	**Unit**
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC} V_{COM}		Full	0		V+	V
On-Resistance	R_{ON}	V+ = 2.7 V, V_{COM} = 0.2 V/1.5 V, I_{NO}, I_{NC} = 100 mA	Room Full		0.85	1.6 1.7	Ω
R_{ON} Flatness	R_{ON} Flatness	V+ = 2.7 V, V_{COM} = 0 V to V+, I_{NO}, I_{NC} = 100 mA	Room		0.16		
R_{ON} Match	ΔR_{ON}		Room		0.15		
Switch Off Leakage Current	$I_{NO(off)}$ $I_{NC(off)}$	V+ = 3.3 V V_{NO}, V_{NC} = 1 V/3 V, V_{COM} = 3 V/1 V	Room Full	- 1 - 10		1 10	nA
	$I_{COM(off)}$		Room Full	- 1 - 10		1 10	
Channel-On Leakage Current	$I_{COM(on)}$	V+ = 3.3 V, V_{NO}, V_{NC} = V_{COM} = 1 V/3 V	Room Full	- 1 - 10		1 10	
Digital Control							
Input High Voltage	V_{INH}		Full	2			V
Input Low Voltage	V_{INL}		Full			0.4	
Input Capacitance	C_{in}		Full		4		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 V or V+	Full	- 1		1	µA
Dynamic Characteristics							
Turn-On Time	t_{ON}	V_{NO} or V_{NC} = 2 V, R_L = 300 Ω, C_L = 35 pF	Room Full		40	65 67	ns
Turn-Off Time	t_{OFF}		Room Full		35	60 62	
Break-Before-Make Time	t_d		Full	1	3		
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω	Room		7		pC
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room		- 67		dB
Crosstalk[d]	X_{TALK}		Room		- 70		
N_O, N_C Off Capacitance[d]	$C_{NO(off)}$	V_{IN} = 0 V or V+, f = 1 MHz	Room		63		pF
	$C_{NC(off)}$		Room		67		
Channel-On Capacitance[d]	$C_{NO(on)}$		Room		200		
	$C_{NC(on}$		Room		196		

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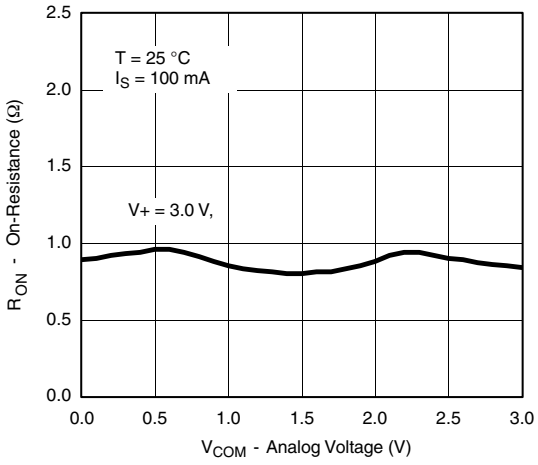
SPECIFICATIONS (V+ = 3 V)							
Parameter	**Symbol**	**Test Conditions Otherwise Unless Specified** V+ = 3 V, ± 10 %, V_{IN} = 0.4 V or 2 V[e]	**Temp.[a]**	**Limits - 40 °C to 85 °C** **Min.[b]**	**Typ.[c]**	**Max.[b]**	**Unit**
Power Supply							
Power Supply Range	V+			2.7		3.3	V
Power Supply Current	I+	V_{IN} = 0 V or V+	Full			1	µA
Power Consumption	P_C		Full			3.3	µW

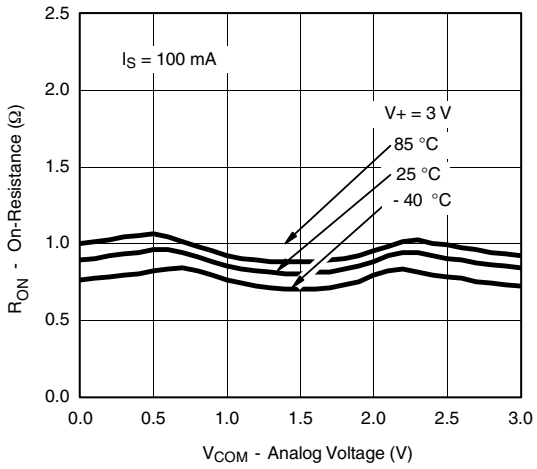
Notes:
a. Room = 25 °C, full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Guaranteed by 5 V leakage testing, not production tested.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

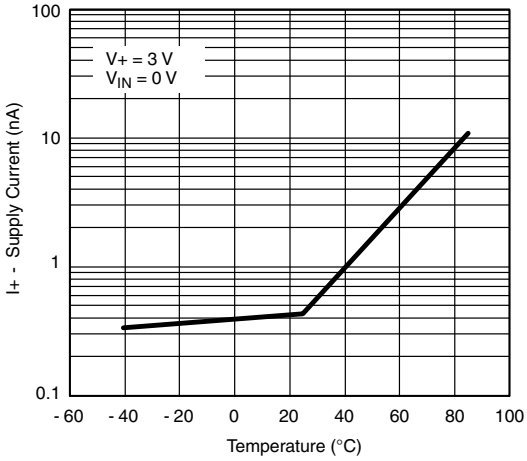
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



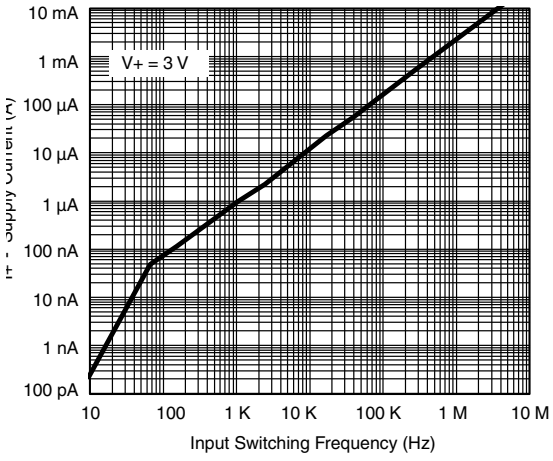
R_{ON} vs. V_{COM} and Supply Voltage



R_{ON} vs. Analog Voltage and Temperature



Supply Current vs. Temperature



Supply Current vs. Input Switching Frequency

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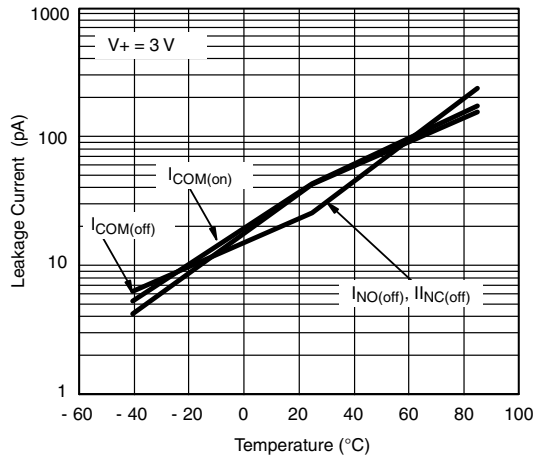
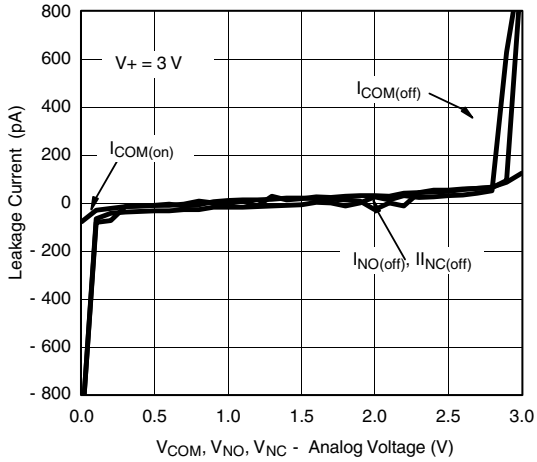
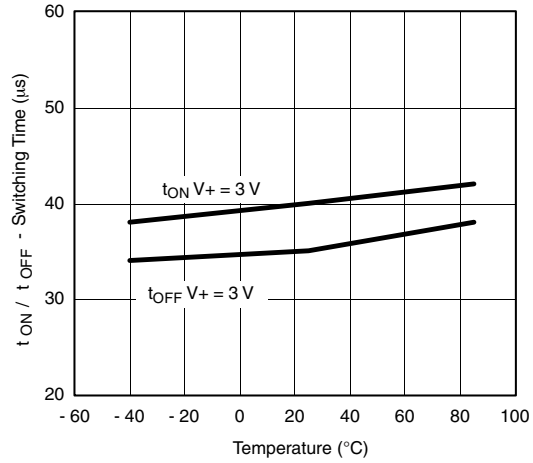
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



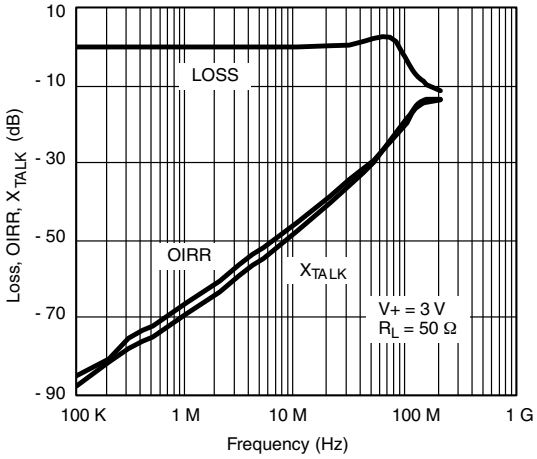
Leakage Current vs. Temperature



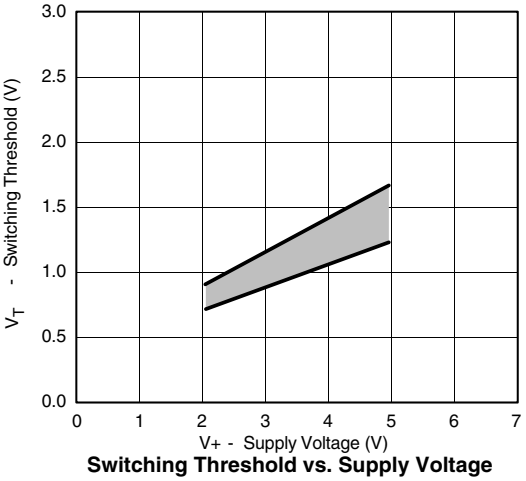
Leakage vs. Analog Voltage



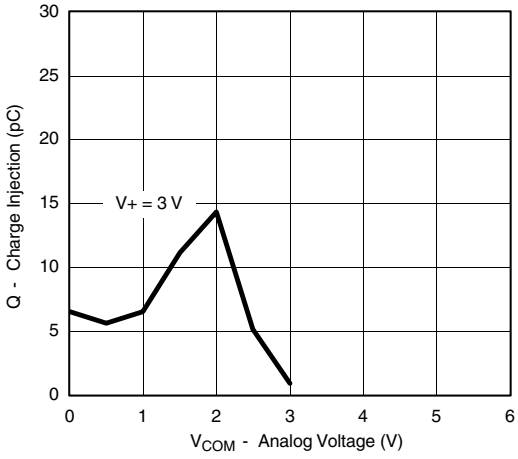
Switching Time vs. Temperature



Insertion Loss, Off-Isolation Crosstalk vs. Frequency



Switching Threshold vs. Supply Voltage



Charge Injection vs. Analog Voltage

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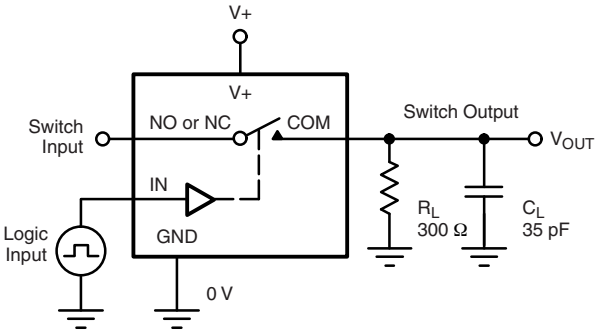
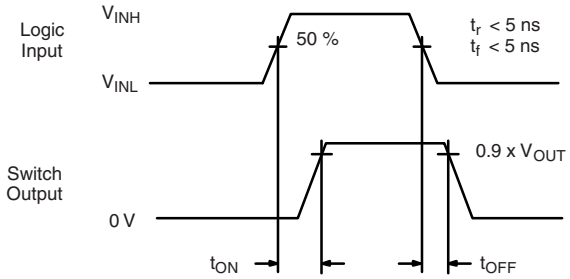
TEST CIRCUITS



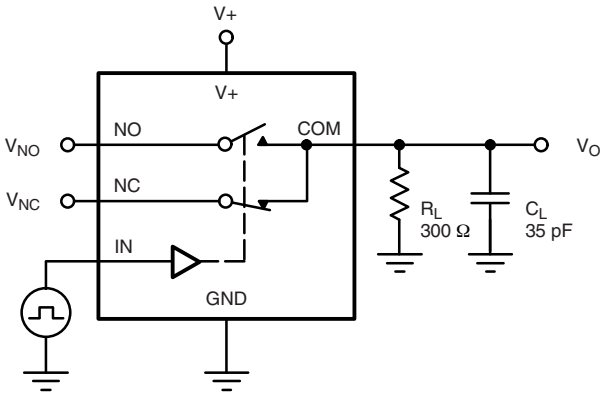
C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1. Switching Time



C_L (includes fixture and stray capacitance)

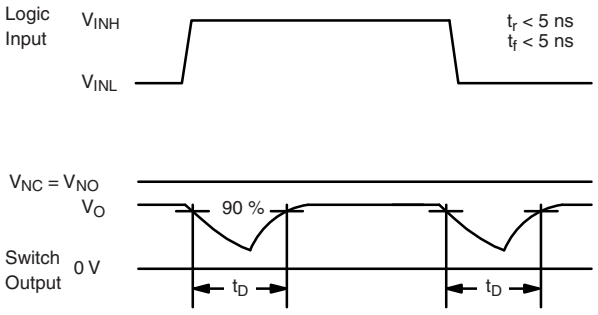
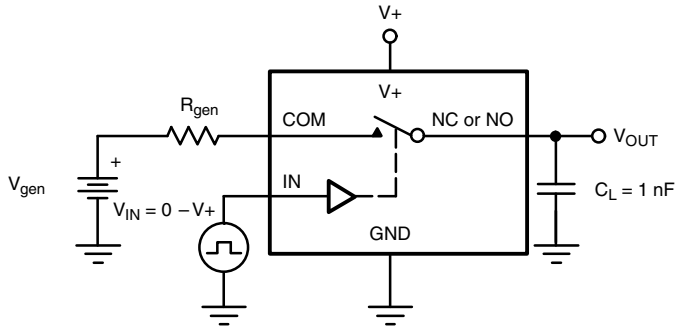
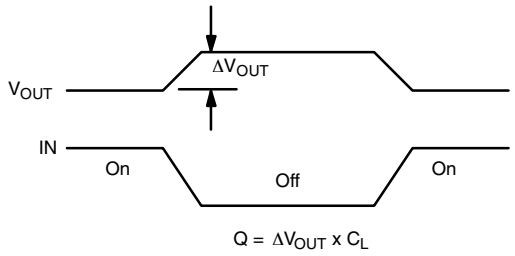


Figure 2. Break-Before-Make Interval





$Q = \Delta V_{OUT} \times C_L$

IN depends on switch configuration: input polarity determined by sense of switch.

Figure 3. Charge Injection

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TEST CIRCUITS

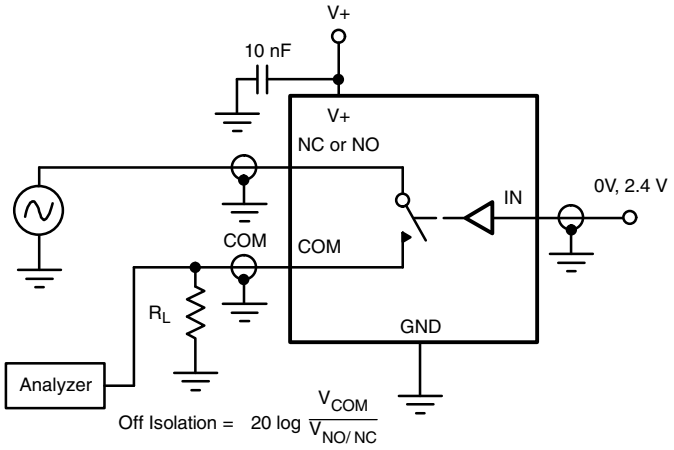

Figure 4. Off-Isolation

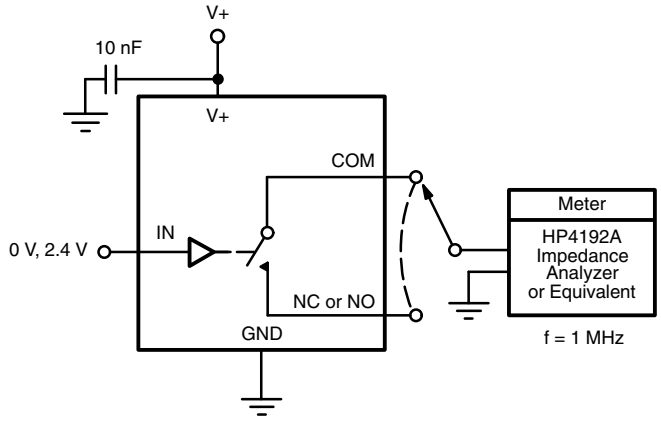

Figure 5. Channel Off/On Capacitance

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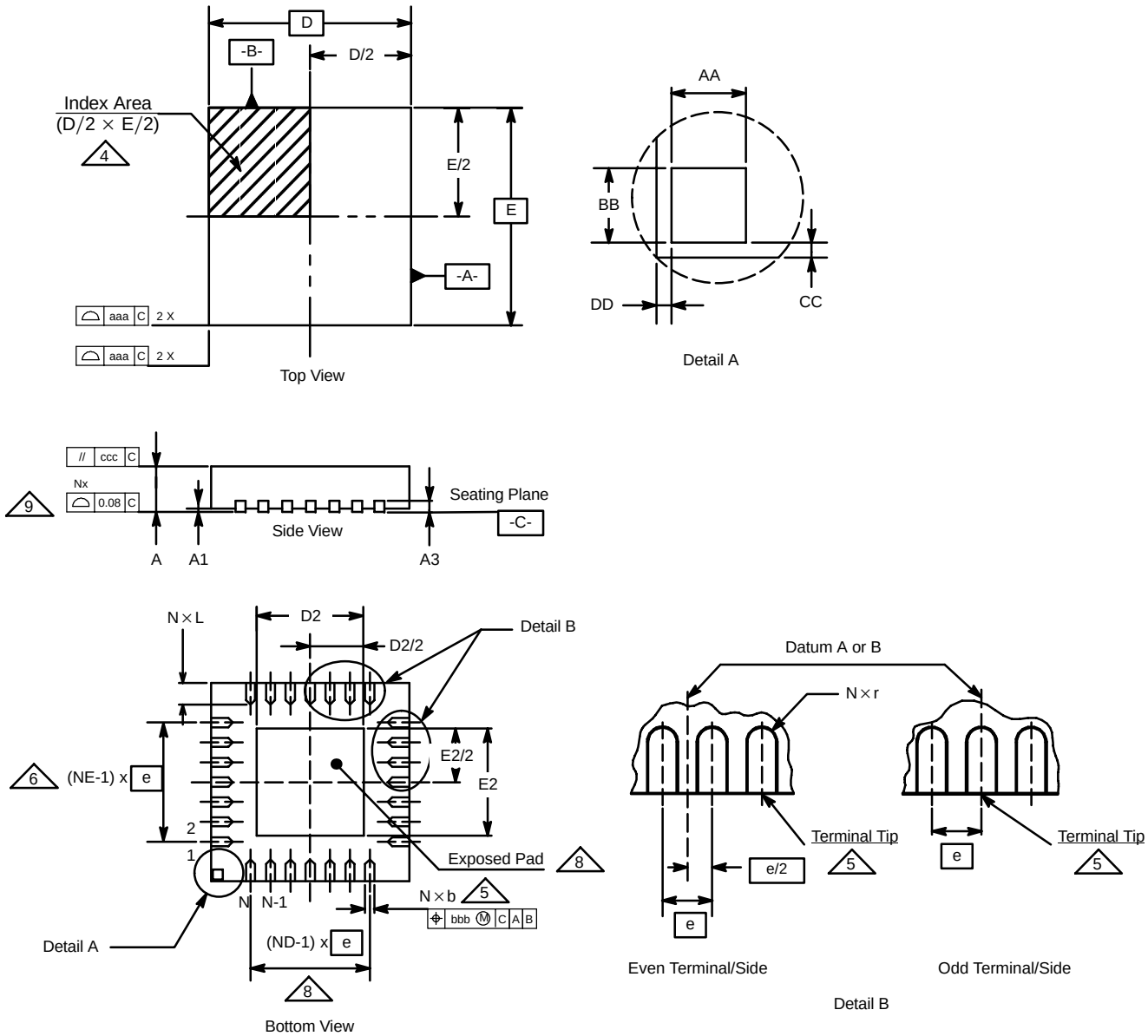
QFN-16 (4 × 4 mm)

JEDEC Part Number: MO-220



QFN-16 (4 × 4 mm)
JEDEC Part Number: MO-220

Dim	MILLIMETERS*			INCHES			Notes
	Min	Nom	Max	Min	Nom	Max	
A	0.80	0.90	1.00	0.0315	0.0354	0.0394	
A1	0	0.02	0.05	0	0.0008	0.0020	
A3	-	0.20 Ref	-	-	0.0079	-	
AA	-	0.345	-	-	0.0136	-	
aaa	-	0.25	-	-	0.0098	-	
BB	-	0.345	-	-	0.0136	-	
b	0.23	0.30	0.38	0.0091	0.0118	0.0150	5
bbb	-	0.10	-	-	0.0039	-	
CC	-	0.18	-	-	0.0071	-	
ccc	-	0.10	-	-	0.0039	-	
D		4.00 BSC			0.1575 BSC		
D2	2.00	2.15	2.25	0.0787	0.0846	0.0886	
DD	-	0.18	-	-	0.0071	-	
E		4.00 BSC			0.1575 BSC		
E2	2.00	2.15	2.25	0.0787	0.0846	0.0886	
e		0.65 BSC			0.0256 BSC		
L	0.45	0.55	0.65	0.0177	0.0217	0.0256	
N		16			16		3, 7
ND	-	4	-	-	4	-	6
NE	-	4	-	-	4	-	6
r	b(min)/2	-	-	b(min)/2	-	-	

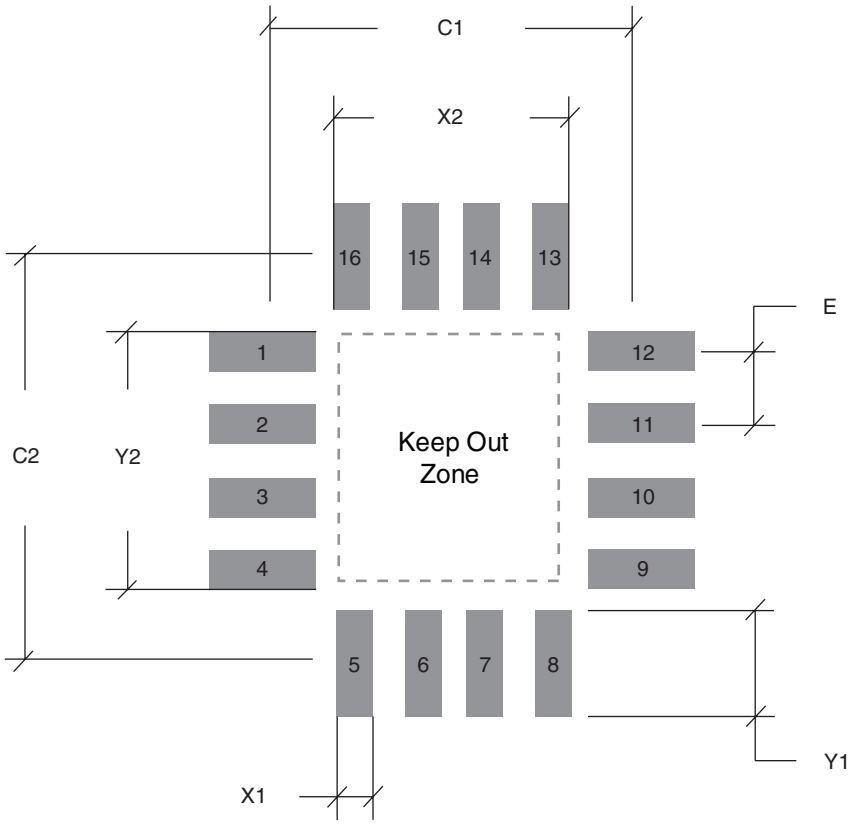
* Use millimeters as the primary measurement.

ECN: S-21437—Rev. A, 19-Aug-02
DWG: 5890

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters. All angels are in degrees.
3. N is the total number of terminals.
4. The terminal #1 identifier and terminal numbering convention shall conform to JESD 95-1 SPP-012. Details of terminal #1 identifier are optional, but must be located within the zone indicated. The terminal #1 identifier may be either a molded or marked feature. The X and Y dimension will vary according to lead counts.
5. Dimension b applies to metallized terminal and is measured between 0.25 mm and 0.30 mm from the terminal tip.
6. ND and NE refer to the number of terminals on the D and E side respectively.
7. Depopulation is possible in a symmetrical fashion.
8. Variation HHD is shown for illustration only.
9. Coplanarity applies to the exposed heat sink slug as well as the terminals.

RECOMMENDED MINIMUM PADS FOR QFN-16 (4 x 4 MM BODY)



	Inches	Millimeters
C1	0.142	3.60
C2	0.142	3.60
E	0.026	0.65
X1	0.014	0.35
X2	0.089	2.25
Y1	0.037	0.95
Y2	0.089	2.25

Note:
QFN-16 (4 x 4) has an exposed center pad that must not come into contact with any metalized structure on the PCB. This area is considered a Keep Out Zone.

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