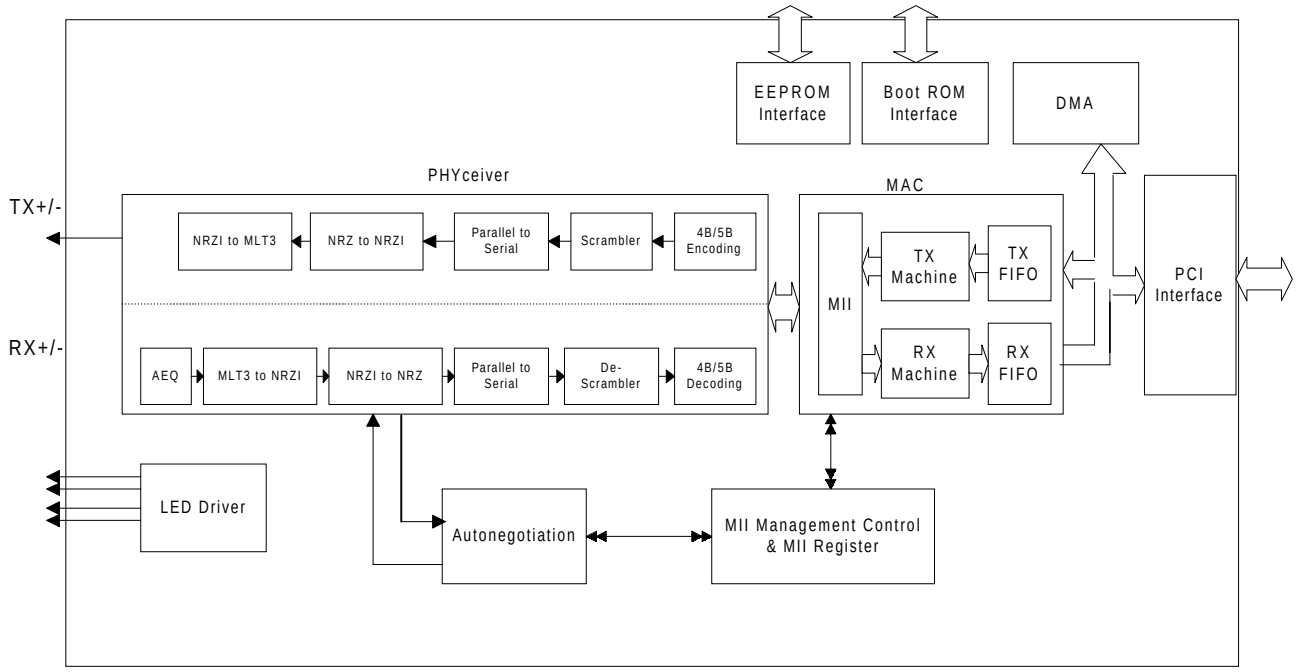
General Description

The DAVICOM's DM9102 is a highly integrated single-chip Fast Ethernet controller. It fully integrated 100BASE-TX/10Base-T Fast Ethernet MAC, PHY and PMD. It is fully compliant with PCI Spec. 2.1 and IEEE802.3u. The DM9102 provides a direct interface to the PCI local bus and direct connection to the network wire. As a controller, it provides the bus master capability. The DM9102 also supports auto-negotiation function that enables it to detect speed and duplex automatically. Due to the well-controlled rising/falling time, it requires no external filter to transmit signal to the media.

Block Diagram



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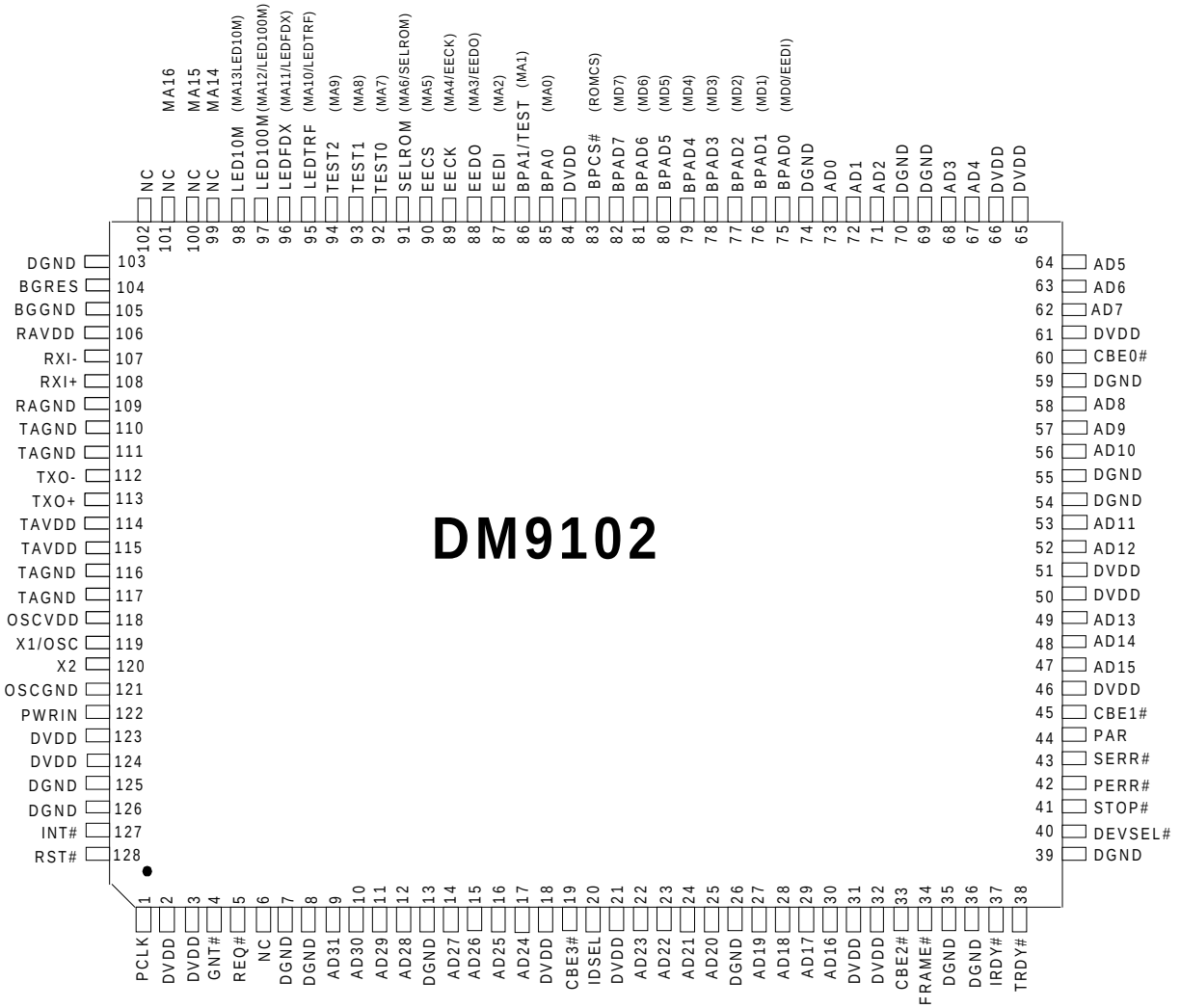
Features

- Single chip LAN controller integrated Fast Ethernet MAC, PHY and transceiver
- Compliant with IEEE 802.3u 100BASE-TX, IEEE 802.3 10BASE-T and ANSI X3T12 TP-PMD standard
- Direct interface to the PCI bus & fully compliant with PCI specification 2.1
- PCI bus master architecture
- Support PCI bus burst mode data transfer with programmable burst size
- EEPROM 93C46 interface to store configuration information and user defined message
- Support up to 256K bytes Boot ROM interface
- Two large independent receive FIFO (4K) & transmit FIFO (2K) with programmable FIFO threshold and full packet burst processing
- Support automatic packet deletion for runt packets and packet re-transmission with no FIFO reload
- Support Full/Half Duplex operation
- Physical, broadcast address recognition and 512-bit hash table algorithm for multicast address filtering
- Compliant with IEEE802.3u Auto-negotiation protocol for automatic link type selection
- High performance 100Mbps clock generator and data recovery circuit
- Digital clock recovery circuit using advanced digital algorithm to reduce jitter
- Adaptive equalization circuit and Baseline wandering restoration circuit for 100Mbps receiver
- Provides Loopback mode for easy system diagnostics
- 128 pin QFP with CMOS process

Pin Configuration



■ Pin Description

I = Input, O = Output, I/O = Input/Output, O/D = Open Drain, P = Power
LI = reset Latch Input, # = all pin name with # are asserted Low

PCI Bus Interface

Pin No.	Pin Name	I/O	Description
1	PCLK	I	PCI system clock PCI bus clock that provides timing for DM9102 related to PCI bus transactions. The clock frequency range is up to 33MHz.
4	GNT#	I	Bus Grant This signal is asserted low to indicate that DM9102 has been granted ownership of the bus by the central arbiter.
5	REQ#	O	Bus Request The DM9102 will assert this signal low to request the ownership of the bus.
6	NC		No Connection
20	IDSEL	I	Initialization Device Select This signal is asserted high during Configuration Space read and write access.
34	FRAME#	I/O	Cycle Frame This signal is driven low by the DM9102 master mode to indicate the beginning and duration of a bus transaction.
37	IRDY#	I/O	Initiator Ready This signal is driven low when the master is ready to complete the current data phase of the transaction. A data phase is completed on any clock both IRDY# and TRDY# are sampled asserted.
38	TRDY#	I/O	Target Ready This signal is driven low when the target is ready to complete the current data phase of the transaction. During a read, it indicates that valid data is asserted. During a write, it indicates the target is prepared to accept data.
40	DEVSEL#	I/O	Device Select The DM9102 asserts the signal low when it recognizes its target address after FRAME# is asserted. As a bus master, the DM9102 will sample this signal to insure that the destination address for the data transfer is recognized by a target.
41	STOP#	I/O	Stop This signal is asserted low by the target device to request the master device to stop the current transaction.
42	PERR#	I/O	Parity Error The DM9102 as a master or slave will assert this signal low to indicate a parity error on any incoming data.
43	SERR#	I/O	System Error This signal is asserted low when an address parity is detected with PCICS bit31 (detected parity error) Is

			enabled. The system error asserts two clock cycles after the falling address if an address parity error is detected.
44	PAR	I/O	Parity This signal indicates even parity across AD0~AD31 and C/BE0#~C/BE3# including the PAR pin. This signal is an output for the master and an input for the slave device. It is stable and valid one clock after the address phase.
19 33 45 60	C/BE3# C/BE2# C/BE1# C/BE0#	I/O	Bus Command/Byte Enable During the address phase, these signals define the bus command or the type of bus transaction that will take place. During the data phase these pins indicate which byte lanes contain valid data. C/BE0# applies to bit7-0 and C/BE3# applies to bit31-24.
9~12, 14~17, 22~25,27~30,47,48, 49,52,53,56,57,58,62, 63,64,67,68,71,72,73	AD31~AD0	I/O	Address & Data These are multiplexed address and data bus signals. As a bus master, the DM9102 will drive address during the first bus phase. During subsequent phases, the DM9102 will either read or write data expecting the target to increment its address pointer. As a target, the DM9102 will decode each address on the bus and respond if it is the target being addressed.
127	INT#	O/D	Interrupt Request This signal will be asserted low when an interrupt condition as defined in CR5 is set, and the corresponding mask bit in CR7 is not set.
128	RST#	I	System Reset When this signal is asserted low, DM9102 performs the internal system reset to its initial state.

Boot ROM and EEPROM Interface (Including Multiplex Mode or Direct Mode):
Multiplex Mode:

Pin No.	Pin Name	I/O	Description
75~82	BPAD0~BPAD7	I/O	Boot ROM Address and Data bus Boot ROM address and Data multiplexed lines bits 0~7. In two consecutive address cycles, these lines contain the boot ROM address pins 7~2, out_enable and write_enable of boot ROM in the first cycle; and these lines contain address pins 15~8 in second cycle. After the first two cycles, these lines contain data bit 7~0 in consective cycles.
83	BPCS#	O	Boot ROM Chip Select Boot ROM or external register chip select signal.
85	BPA0	O,LI	Boot ROM address line. Low address bit0 interfacing to Boot ROM.
86	BPA1/TEST	O	Boot ROM address line. Low address bit1 interfacing to Boot ROM. This bit is also set to enable TEST mode only in multiplex mode. (debug only)

87	EEDI	I,LI	EEPROM Data In The DM9102 will read the contents of EEPROM serially through this pin.
88	EEDO	O	EEPROM Data Out The DM9102 will use this pin to serially write op codes, addresses and data into the EEPROM.
89	EECK	O	EEPROM Serial Clock This pin provides the clock for the EEPROM data transfer.
90	EECS	O	EEPROM Chip Select This pin will enable the EEPROM during loading of the Configuration Data.
92	TEST0	I	TEST option control This pin are valid only test mode enabled. In normal operation when in multiplex mode, this pin are pulled low.
93,94	TEST1,TEST2	I	TEST option control These two pins are valid only test mode is enabled. In normal operation when in multiplex mode, these two pins are pulled low.
99~101	NC		In Multiplex mode, these three pins are not connected.

Direct Mode

Pin No.	Pin Name	I/O	Description
75	MD0/EEDI	I	Boot ROM Data Input/EEDI Data In This pin is multiplexed by EEDI and MD0. The DM9102 will read the contents of EEPROM serially through this pin.
76~82	MD1~MD7	I	Boot ROM Data Input Bus
83	ROMCS	O	Boot ROM or EEPROM chip selection.
85~87	MA0~MA2	O	Boot ROM Address Output Bus
88	MA3/EEDO	O	Boot ROM Address Output/EEPROM Data Out This pin is multiplexed with MA3 and EEDO. The DM9102 will use this pin to serially write op codes, addresses and data into the EEPROM.
89	MA4/EECK	O	Boot ROM Address Output/EEPROM Serial Clock This pin is multiplexed with MA4 and EECK. This pin provides the clock for the EEPROM data transfer.
90	MA5	O	Boot ROM Address Output Bus
91	MA6/SELROM	O/LI	Boot ROM Address Output Bus/Multiplex or Direct mode selection It is also used as multiplex or direct mode selection at power-up reset. 0 = multiplex mode, 1 = direct mode.
92~94	MA7~MA9	O	Boot ROM Address Output Bus
95~98	MA10/LEDTRF	O	Boot ROM Address Output Bus/Active LED When at the time of Boot ROM operation, the LED maybe flash few seconds. LED Active Low. When operates as LED pin, if Bit5 of PHY

			management register16 is 0, it is the Activity LED and will flash when in transmitting or receiving. If Bit5 of PHY Management register16 is 1, this pin is no use
96	MA11/LEDFDX	O	Boot ROM Address Output/Full-Duplex LED Indicates Full Duplex mode operation. Active low. When at the time of Boot ROM operation, the LED maybe flash few seconds.
97	MA12/LED100M	O	Boot ROM Address Output/100Mbps LED When at the time of Boot ROM operation, the LED maybe flash few seconds. LED Active Low. When operates as LED pin, if Bit5 of PHY management register16 is 0, it indicates good link to 100Mbps (default). If Bit5 of PHY management register16 is 1, it is link and activity LED.
98	MA13/LED10M	O	Boot ROM Address Output Bus/10Mbps LED When at the time of Boot ROM operation, the LED maybe flash few seconds. LED Active Low. When operates as LED pin, if Bit5 of PHY management register16 is 0, it indicates good link to 10Mbps (default). If Bit5 of PHY management register16 is 1, it is link and activity LED.
99~101	MA14~MA16	O	Boot ROM Address Output Bus

LED Pins

Pin No.	Pin Name	I/O	Description
95	LEDTRF	O	Active LED, Active Low If Bit5 of PHY management register16 is 0, it is the Activity LED and will flash when in transmitting or receiving. (default) If Bit5 of PHY Management register16 is 1, this pin is no use.
96	LEDFDX	O	Full-Duplex LED, Active Low Indicates Full-Duplex mode operation.
97	LED100M	O	100Mbps LED, Active Low Indicates 100Mbps mode operation. If Bit5 of PHY management register16 is 0, it indicates good link to 100Mbps. (default) If Bit5 of PHY management register16 is 1, it is link and activity LED.
98	LED10M	O	10Mbps LED, Active Low. Indicates 10Mbps mode operation. If Bit5 of PHY management register16 is 0, it indicates good link to 10Mbps. (default) If Bit5 of PHY management register16 is 1, it is link and activity LED.

Network Interface

Pin No.	Pin Name	I/O	Description
107 108	RXI- RX+	I	100M/10Mbps Differential Input Pair. These two pins are differential receive input pair for 100BASE-TX and 10BASE-T. They are capable of receiving 100BASE-TX MLT-3 or 10BASE-T Manchester encoded data.
112 113	TXO- TXO+	O	100M/10Mbps Differential Output Pair. These two pins are differential output pair for 100BASE-TX and 10BASE-T. This output pair provides controlled rise and fall times designed to filter the transmitter output.

Clock Pins

Pin No.	Pin Name	I/O	Description
118	OSCVDD	P	Analog Power
119	X1/OSC	I	Crystal or Oscillator Input. (25MHZ± 50ppm)
120	X2	O	Crystal feedback output pin used for crystal connection only. Leave this pin open if oscillator is used.
121	OSCGND	P	Analog Ground

Miscellaneous Pins

Pin No.	Pin Name	I/O	Description
91	SELROM	LI	Multiplex mode/Direct mode Selection. This pin is “reset latch input at power up” to select Multiplex mode or direct mode. “0” = multiplex mode (default), “1” = direct mode. At direct mode, this is also a output pin which is used by MA6.
102	NC	O	No Connection
104	BGRES	I	Band-gap Voltage Reference Resistor. It connects to a 6200Ω, 1% error tolerance resistor between this pin and BGGND pin (pin 105) to provide an accurate current reference for DM9102.
105	BGGND	I	Ground for Band-gap circuit
122	PWRIN	I	VDD clamp This pin is used to identify the D3(cold) power state in a power management aware system. This pin should be connected to the PCI power, while other DVDD pins should be connected to the auxiliary power, if any. In non-power management aware systems, or there is no auxiliary power, the DVDD pins and the PWRIN pins should be connected to the PCI power

Power Pins

Pin No.	Pin Name	I/O	Description
106	RAVDD	P	Analog power for receive
109	RAGND	P	Analog ground for receive
114,115	TAVDD	P	Analog power for transmit
110,111,116,117	TAGND	P	Analog ground for transmit
7,8,13,26,35,36,39,54 ,55,59,69,70,74,103, 125,126	DGND	P	Digital ground pins
2,3,18,21,31,32,46,50 ,51,61,65,66,84,123, 124	DVDD	P	Digital power pins

■ Register Definition

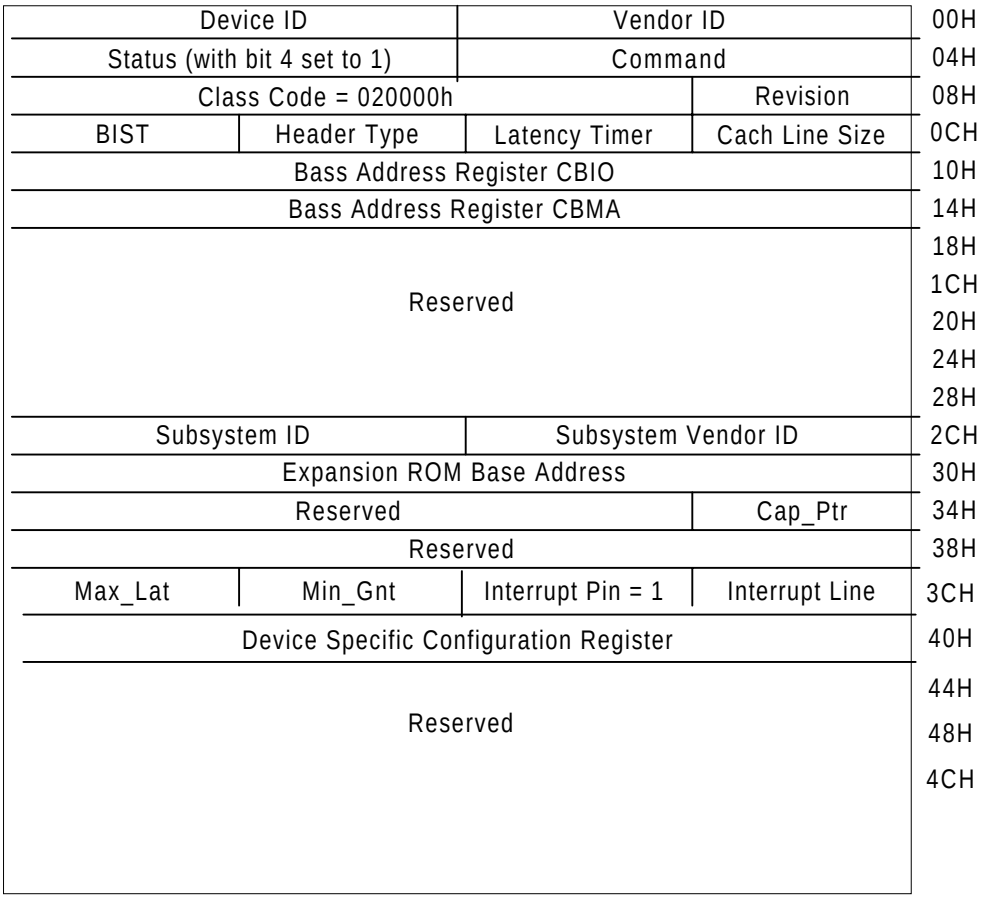
✧ PCI Configuration Registers

The definitions of PCI Configuration Registers are based on the PCI specification revision 2.1 and provides the initialization and configuration information to operate the PCI interface in the DM9102. All registers can be accessed with byte, word, or double word mode. As defined in PCI specification 2.1, read accesses to reserve or unimplemented registers will return a value of "0." These registers are to be described in the following sections.

PCI Configuration Registers Mapping :

Description	Identifier	Address Offset	Value of Reset
Identification	PCIID	00H	91021282H
Command & Status	PCICS	04H	02900007H
Revision	PCIRV	08H	02000020H
Miscellaneous	PCILT	0CH	00000000H
I/O Base Address	PCIIO	10H	undefined
Memory Base Address	PCIMEM	14H	undefined
Reserved	--------	18H - 28H	
Subsystem Identification	PCISID	2CH	load from SROM
Expansion ROM Base Address	PCIROM	30H	00000000H
Capability Pointer	CAP_PTR	34H	00000050H
Reserved	--------	38H	
Interrupt & Latency	PCIINT	3CH	281401XXH
Device Specific Configuration Register	PCIUSR	40H	00000000H

Configuration Register Structure



Key to Default

In the register description that follows, the default column takes the form <Reset Value>

Where：

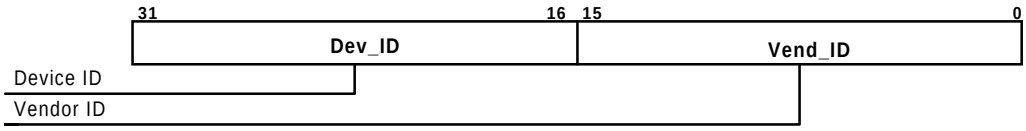
<Reset Value>:

1	Bit set to logic one
0	Bit set to logic zero
X	No default value

<Access Type>:

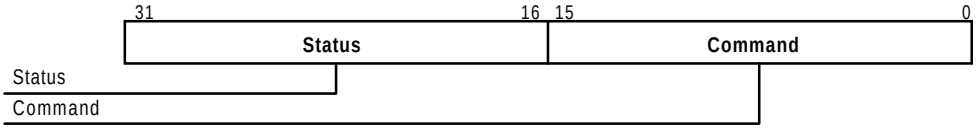
RO = Read only
RW = Read/Write
R/C : means Read / Write & Write "1" for Clear.

Identification ID (xxxxxx00 - PCIID)

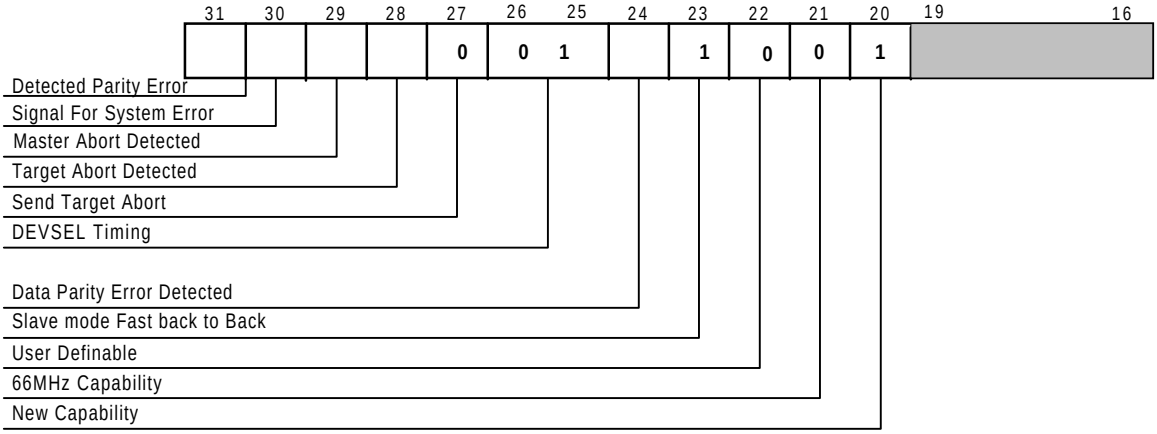


Bit	Default	Type	Description
16:31	9102h	RO	The field identifies the particular device. Unique and fixed number for the DM9102 is 9102h. It is the product number assigned by DAVICOM.
0:15	1282h	RO	This field identifies the manufacturer of the device. Unique and fixed number for Davicom is 1282h. It is a registered number from SIG.

Command & Status (xxxxxx04 - PCICS)

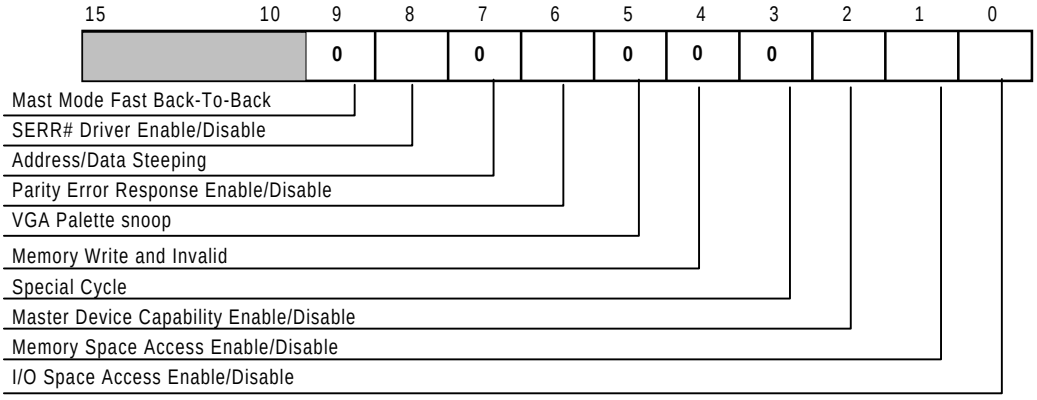


Status Register Definition:



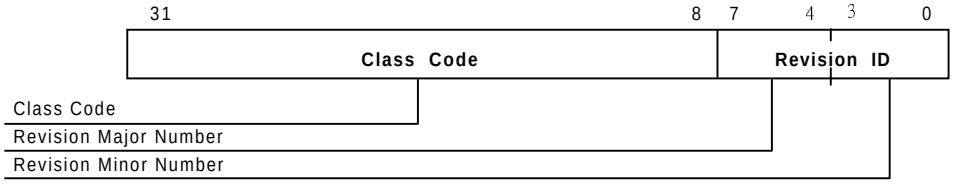
Bit	Default	Type	Description
31	0b	R/C	Detected Parity Error The DM9102 samples the AD[0:31], C/BE[0:3]#, and the PAR signal to check parity and to set parity errors. In slave mode, the parity check falls on command phase and data valid phase (IRDY# and TRDY# both active). While in master mode, the DM9102 will check during each data phase of a memory read cycle for a parity error During a memory write cycle, if an error occurs, the PERR# signal will be driven by the target. This bit is set by the DM9102 and cleared by writing "1". There is no effect by writing "0".
30	0b	R/C	Signal For System Error This bit is set when the SERR# signal is driven by the DM9102. This system error occurs when an address parity is detected under the condition that bit 8 and bit 6 in command register below are set.
29	0b	R/C	Master Abort Detected This bit is set when the DM9102 terminates a master cycle with the master-abort bus transaction.
28	0b	R/C	Target Abort Detected This bit is set when the DM9102 terminates a master cycle due to a target-abort signal from other targets.
27	0b	R/C	Send Target Abort (0 For No Implementation) The DM9102 will never assert the target-abort sequence.
26:25	01b	R/C	DEVSEL Timing (01 Select Medium Timing) Medium timing of DEVSEL# means the DM9102 will assert DEVSEL# signal two clocks after FRAME# is sample “asserted.”
24	0b	R/C	Data Parity Error Detected This bit will take effect only when operating as a master and when a Parity Error Response Bit in command configuration register is set. It is set under two conditions: (i) PERR# asserted by the DM9102 in memory data read error, (ii) PERR# sent from the target due to memory data write error.
23	1b	R/C	Slave mode Fast Back-To-Back Capable (1 For Good Capability) This bit is always reads "1" to indicate that the DM9102 is capable of accepting fast back-to-back transaction as a slave mode device.
22	0b	R/C	User-Definable-Feature Supported (0 For No Support)
21	0b	R/C	66 MHz Capable (0 For No Capability)
20	1b	R/C	New Capabilities This bit indicates whether this function implements a list of extended capabilities such as PCI power management. When set this bit indicates the presence of New Capabilities. A value of 0 means that this function does not implement New Capabilities.
19:16	0000b	RO	Reserved

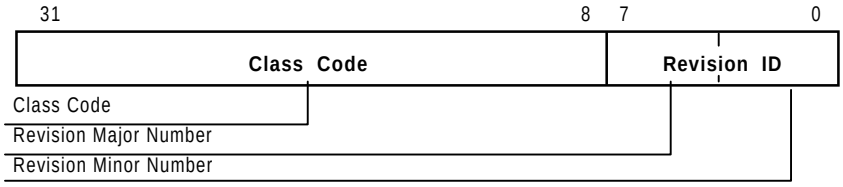
Command Register Definition:



Bit	Default	Type	Description
15:10	000000b	RO	Reserved
9	0b	RO	Master Mode Fast Back-To-Back (0 For No Support) The DM9102 does not support master mode fast back-to-back capability and will not generate fast back-to-back cycles.
8	0b	RW	SERR# Driver Enable/Disable This bit controls the assertion of SERR# signal output. The SERR# output will be asserted on detection of an address parity error and if both this bit and bit 6 are set.
7	0b	RO	Address/Data Stepping (0 For No Stepping)
6	0b	RW	Parity Error Response Enable/Disable Setting this bit will enable the DM9102 to assert PERR# on the detection of a data parity error and to assert SERR# for reporting address parity error.
5	0b	RO	VGA Palette Snooping (0 For No Support)
4	0b	RO	Memory Write and Invalid (0 For No Implementation) The DM9102 only generates Memory write cycle.
3	0b	RO	Special Cycles (0 For No Implementation)
2	1b	RW	Master Device Capability Enable/Disable When this bit is set, DM9102 has the ability of master mode operation.
1	1b	RW	Memory Space Access Enable/Disable This bit controls the ability of memory space access. The memory access includes memory mapped I/O access and Boot ROM access. As the system boots up, this bit will be enabled by BIOS for Boot ROM memory access. While in normal operation using memory mapped I/O access, this bit should be set by driver before memory access cycles.
0	1b	RW	I/O Space Access Enable/Disable This bit controls the ability of I/O space access. It will be set by BIOS after power on.

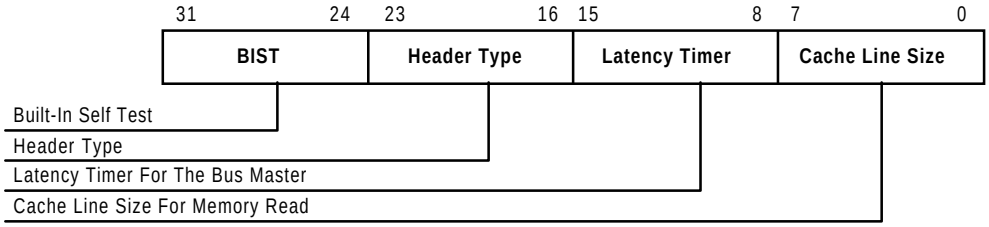
Revision ID (xxxxxx08 - PCIRV)





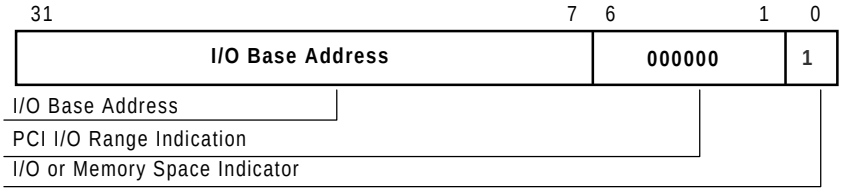
Bit	Default	Type	Description
31:8	020000h	RO	Class Code (020000h) This is the standard code for Ethernet LAN controller.
7:4	0010b	RO	Revision Major Number This is the silicon-major revision number that will increase for the subsequent versions of the DM9102.
3:0	0000b	RO	Revision Minor Number This is the silicon-minor revision number that will increase for the subsequent versions of the DM9102.

Miscellaneous Function (Xxxxxx0c - PCILT)



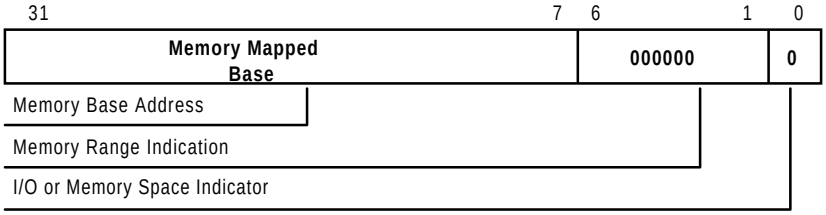
Bit	Default	Type	Description
31:24	00h	RO	Built-In-Self Test (=00h Means No Implementation)
23:16	00h	RO	Header Type (= 00h Means single function with Predefined Header Type)
15:8	00h	RW	Latency Timer For The Bus Master. The latency timer is guaranteed by the system and measured by clock cycles. When the FRAME# asserted at the beginning of a master period by the DM9102, the value will be copied into a counter and start counting down. If the FRAME# is de-asserted prior to count expiration, this value is meaningless. When the count expires before GNT# is de-asserted, the master transaction will be terminated as soon as the GNT# is removed. While GNT# signal is removed and the counter is non-ZERO, the DM9102 will continue with its data transfers until the count expires. The system host will read MIN_GNT and MAX_LAT registers to determine the latency requirement for the device and then initialize the latency timer with an appropriate value.
7:0	00h	RO	Cache-line Size For Memory Read Mode Selection (00h Means No Implementation For Use)

I/O Base Address (Xxxxxx10 - PCIIO)



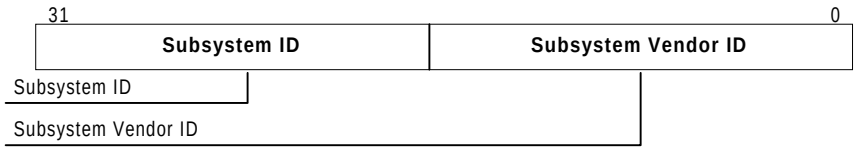
Bit	Default	Type	Description
31:7	Undefined	RW	PCI I/O Base Address This is the base address value for I/O access cycles. It will be compared to AD[31:7] in the address phase of bus command cycle for the I/O resource access.
6:1	000000b	RO	PCI I/O Range Indication It indicates that the minimum I/O resource size is 80h.
0	1b	RO	I/O Space Or Memory Space Base Indicator Determines that the register maps into the I/O space.(=1 Indicates I/O Base)

Memory Mapped Base Address (Xxxxxx14 - PCIMEM)



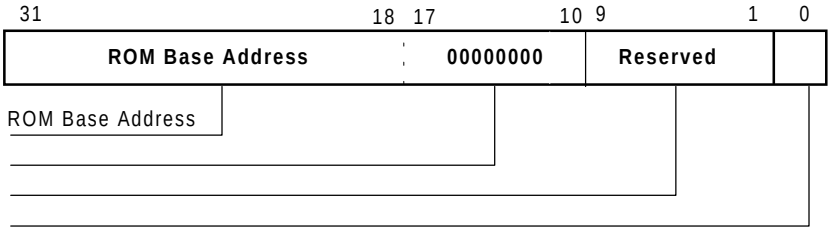
Bit	Default	Type	Description
31:7	Undefined	R/W	PCI Memory Base Address This is the base address value for Memory access cycles. It will be compared to AD[31:7] in the address phase of bus command cycle for the Memory resource access.
6:1	000000b	RO	PCI Memory Range Indication It indicates that the minimum Memory resource size is 80h.
0	0b	RO	I/O Space Or Memory Space Base Indicator Determines that the register maps into the memory space(=0 Indicates Memory Base)

Subsystem Identification (Xxxxxx2c - PCISID)



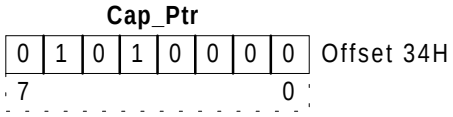
Bit	Default	Type	Description
31:16	XXXX h	RO	Subsystem ID Node number loaded from EEPROM word 1 and different from each card.
15:0	XXXX h	RO	Subsystem Vendor ID Unique number given by PCI SIG and loaded from EEPROM word 0.

Expansion ROM Base Address (Xxxxxx30 - PCIROM)



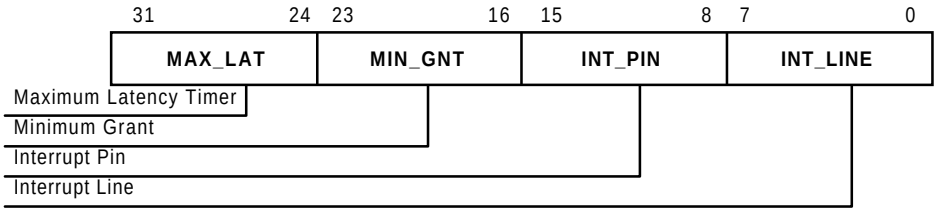
Bit	Default	Type	Description
31:10	00h	RW	ROM Base Address With 256K Boundary PCIROM bit17~10 are hardwired to 0, indicating ROM Size is up to 256K Size
9:1	000000000b	RO	Reserved Bits Read As 0
0	0b	RW	Expansion ROM Decoder Enable/Disable If this bit and the memory space access bit are both set to 1, the DM9102 will responds to its expansion ROM.

Capabilities Pointer (Xxxxxx34 - Cap _Ptr)



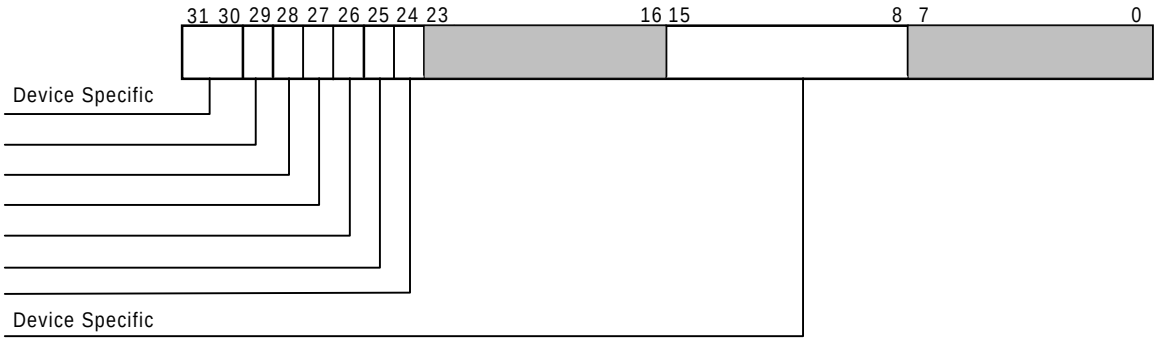
Bit	Default	Type	Description
31:8	000000h	RO	Reserved
7:0	01010000b	RO	Capability Pointer The Cap_Ptr provides an offset (default is 50h) into the function's PCI Configuration Space for the location of the first term in the Capabilities Linked List. The Cap_Ptr offset is DOUBLE WORD aligned so the two least significant bits significant bits are always "0"s

Interrupt & Latency Configuration (Xxxxxx3c - PCIINT)



Bit	Default	Type	Description
31:24	28h	RO	Maximum Latency Timer that can be sustained (Read Only and Read As 28h)
23:16	14h	RO	Minimum Grant Minimum Length of a Burst Period (Read Only and Read As 14h)
15:8	01h	RO	Interrupt Pin read as 01h to indicate INTA#
7:0	XXh	RO	Interrupt Line that Is Routed to the Interrupt Controller

Device Specific Configuration Register (Xxxxxx40 - PCIUSR)



Bit	Default	Type	Description
31	0b	RW	Device Specific Bit (sleep mode)
30	0b	RW	Device Specific Bit (snooze mode)
29	0b	RO	When set enable Link Status Change Wake-up Event
28	0b	RO	When set enable Sample Frame Wake-up Event
27	0b	RO	When set enable Magic Packet Wake-up Event
26	0b	RO	When set, indicates link change and Link Status Change Event occurred
25	0b	RO	When set, indicates the sample frame is received and Sample Frame Event occurred
24	0b	RO	When set, indicates the Magic Packet is received and Magic packet Event occurred
23:16	00h	RO	Reserved Bits Read As 0
15:8	00h	RW	Device Specific
7:0	00h	RO	Reserved Bits Read As 0

✧ Control and Status Registers (CR)

The DM9102 implement 16 control and status register, which can be accessed by the host. These CRs are double long word aligned. All CRs are set to their default values by a hardware or a software reset unless otherwise specified. All Control and Status Registers with their definitions and offset from IO or memory Base Address are shown below**:**

Register	Description	Offset from CSR Base Address	Default
CR0	System Control Register	00H	FFC00000
CR1	Transmit Descriptor Poll Demand	08H	FFFFFFFF
CR2	Receive Descriptor Poll Demand	10H	FFFFFFFF
CR3	Receive Descriptor Base Address Register	18H	00000000
CR4	Transmit Descriptor Base Address Register	20H	00000000
CR5	Network Status Report Register	28H	FC000000
CR6	Network Operation Mode Register	30H	02400040
CR7	Interrupt Mask Register	38H	FFFE0000
CR8	Statistical Counter Register	40H	00000000
CR9	External Management Access Register	48H	FFF097FF
CR10	Programming ROM Address Register	50H	Unpredictable
CR11	General Purpose Timer Register	58H	FFFE0000
CR12	PHY Status Register	60H	FFFFFFXX
CR13	Access Register	68H	XXXXXX00
CR14	Data Register	70H	Unpredictable
CR15	Watchdog And Jabber Timer Register	78H	FFFFFEC8

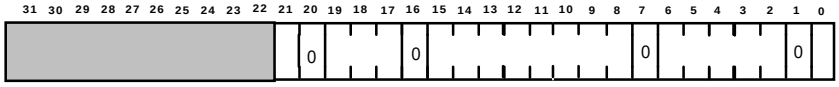
Key to Default

In the register description that follows, the default column takes the form:
<Reset Value>, <Access Type>
Where：
<Reset Value>:

1 Bit set to logic one
0 Bit set to logic zero
X No default value

<Access Type>:
RO = Read only
RW = Read/Write
WO = Write only

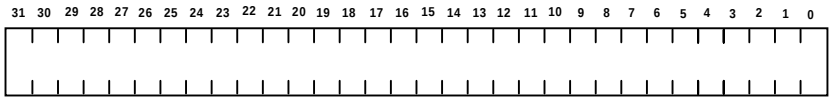
1. System Control Register (CR0)



Bit	Name	Default	Description
21	MRM	0b,RW	Memory Read Multiple When set, the DM9102 will use memory read multiple command (C/BE3~0 = 1100) when it initialize the memory read burst transaction as a master device. When reset, it will use memory read command (C/BE3 ~ 0 = 0110) for the same master operation.
20	Reserved	0b,RW	Must be Zero
19:17	TXAP	000b,RW	Transmit Automatic polling interval time When set, the DM9102 will poll the transmit descriptor automatically when it is in the suspend state due to buffer unavailable. The polling interval time is programmable based on the table shown below: Bit 19 / Bit 18 / Bit 17 / Time Interval 0 / 0 / 0 / No polling 0 / 0 / 1 / 200us 0 / 1 / 0 / 800us 0 / 1 / 1 / 1.6ms 1 / 0 / 0 / 12.8us 1 / 0 / 1 / 25.6us 1 / 1 / 0 / 51.2us 1 / 1 / 1 / 102.4us
16	Reserved	0b,RW	Must be Zero
15:14	ABA	00b,RW	Address Boundary Alignment When set, the DM9102 will execute each burst cycles to stop at the programmed address boundary. The address boundary can be programmed to be 8, 16, or 32 double-word as shown below. Bit 15 / Bit 14 / Alignment Boundary 0 / 0 / Reserved 0 / 1 / 8-double word 1 / 0 / 16-double word 1 / 1 / 32-double word
13:8	BL	000000b, RW	Burst Length When reset, the DM9102's burst length in one DMA transfer is limited by the amount of data in the receive FIFO (when receive) or the amount of free space in the transmit FIFO (when transmit). When set, the DMA's burst length is limited by the programmed value. The permissible values are 0, 1, 2, 4, 8, 16, or 32 doublewords.
7	Reserved	0,RW	Must be Zero
6:2	DGW	00000,RW	Descriptor Gap Width The value of this field defines the gap width (count in double-word) between two continuous descriptor. It is used in ring-type descriptor structure.
1	Reserved	0,RW	Must be Zero

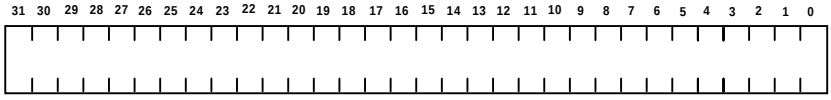
Bit	Name	Default	Description
0	SR	0,RW	Software Reset When set, the DM9102 will make a internal reset cycle. All consequent action to DM9102 should wait at least 32 PCI clock cycles to start and no necessary to reset this

2. Transmit Descriptor Poll Demand (CR1)



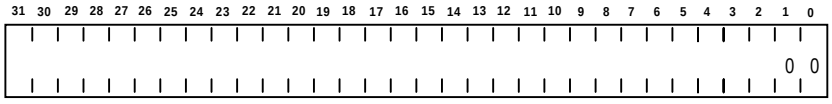
Bit	Name	Default	Description
31:0	TDP	FFFFFFFF h ,WO	Transmit Descriptor Polling Command Writing any value to this port will force DM9102 to poll the transmit descriptor. If the acting descriptor is not available, transmit process will return to suspend state. If the descriptor shows buffer available, transmit process will begin the data transfer.

3. Receive Descriptor Poll Demand (CR2)



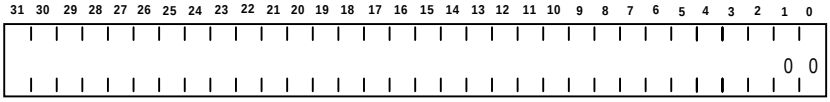
Bit	Name	Default	Description
31:0	RDP	FFFFFFFFH ,WO	Receive Descriptor Polling Command Writing any value to this port will force DM9102 to poll the receive descriptor. If the acting descriptor is not available, receive process will return to suspend state. If the descriptor shows buffer available, receive process will begin the data transfer.

4. Receive Descriptor Base Address (CR3)



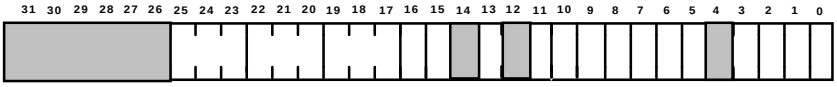
Bit	Name	Default	Description
31:0	RDBA	00000000h ,RW	Receive Descriptor Base Address This register defines base address of receive descriptor-chain (or descriptor-ring) and must be double-word aligned. The receive descriptor- polling command after CR3 is set will make DM9102 to fetch the descriptor at the Base-Address. In Ring-type structure, the descriptor pointer will go back to the Base-Address after End-descriptor of ring. Bit1,0 must be “00” for double word alignment.

5. Transmit Descriptor Base Address (CR4)



Bit	Name	Default	Description
31:0	TDBA	00000000h ,RW	Transmit Descriptor Base Address This register defines base address of transmit descriptor-chain (or descriptor-ring) and must be double-word aligned. The transmit descriptor- polling command after CR4 is set will make DM9102 to fetch the descriptor at the Base-Address. In Ring-type structure, the descriptor pointer will go back to the Base-Address after End-descriptor of ring. Bit1,0 must be "00" for double word alignment.

6. Network Status Report Register (CR5)



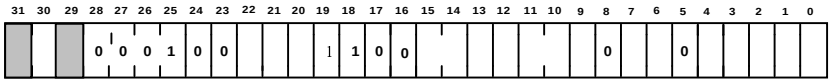
Bit	Name	Default	Description
25:23	SBEB	000,RO	System Bus Error Bits These bits are read only and used to indicate the type of system bus fetal error. Valid only when System Bus Error is set. The mapping bits are shown below. Bit25 Bit24 Bit23 Bus Error Type 0 0 0 Parity error 0 0 1 Master abort 0 1 0 Slave abort 0 1 1 Reserved 1 X X Reserved
22:20	TXPS	000,RO	Transmit Process State These bits are read only and used to indicate the state of transmit process. The mapping table is shown below. Bit22 Bit21 Bit20 Process State 0 0 0 Transmit process stopped 0 0 1 Fetch transmit descriptor 0 1 0 Move Setup Frame from the host memory 0 1 1 Move data from host memory to transmit FIFO 1 0 0 Close descriptor by clearing owner bit of descriptor 1 0 1 Waiting end of transmit 1 1 0 Transmit end and Close descriptor by writing status 1 1 1 Transmit process suspend
19:17	RXPS	000b,RO	Receive Process State These bits are read only and used to indicate the state of receive process. The mapping table is shown below. Bit19 Bit18 Bit17 Process State

			0 0 0 Receive process stopped 0 0 1 Fetch receive descriptor 0 1 0 Waiting for receive packet under buffer available 0 1 1 Move data from receive FIFO to host memory 1 0 0 Close descriptor by clearing owner bit of descriptor 1 0 1 Close descriptor by writing status 1 1 0 Receive process suspended due to buffer unavailable 1 1 1 Purge the current frame from the receive FIFO because of unavailable receive buffer
16	NIS	0b,RW	Normal Interrupt Summary Normal interrupt includes any of the three conditions : CR5<0> – TXCI : Transmit Complete Interrupt CR5<2> – TXDU : Transmit Buffer Unavailable CR5<6> – RXCI : Receive Complete Interrupt
15	AIS	0b,RW	Abnormal Interrupt Summary Abnormal interrupt includes any interrupt condition as shown below excluding Normal Interrupt conditions. They are TXPS(bit1), TXJT(bit3), TXFU(bit5), RXDU(bit7), RXPS(bit8), RXWT(bit9), TXER(bit10), GPT(bit11), SBE(bit13).
13	SBE	0b,RW	System Bus Error The PCI system bus errors will set this bit. The type of system bus error is shown in CR5<25:23> .
11	GPT	0b,RW	General-purpose Timer Expired This bit is set to indicate the general-purpose timer (described in CR11) has expired.
10	TXER	0b,RW	Transmit Early Interrupt Transmit Early Interrupt is set when the full packet data has been moved from host memory into transmit FIFO. It will inform the host to process next step before the transmission end. Transmit complete event CR5<0> will clear this bit automatically.
9	RXWT	0b,RW	Receive Watchdog Timer Expired This bit is set to indicate receive watchdog timer has expired.
8	RXPS	0b,RW	Receive Process Stopped This bit is set to indicate receive process enters the stopped state.
7	RXDU	0b,RW	Receive Buffer Unavailable This bit is set when the DM9102 fetches the next receive descriptor is still owned by the host. Receive process will be suspended until a new frame enters or the receive polling command is set.
6	RXCI	0b,RW	Receive Complete Interrupt This bit is set when a received frame is fully moved into host memory and receive status has been written to descriptor. Receive process is still running and continues to fetch next descriptor.
5	TXFU	0b,RW	Transmit FIFO Under-run This bit is set when the transmit FIFO has a under-run condition during the packet transmission. It may happen due to the heavy load on bus, receive process dominate in full-duplex, or transmit buffer unavailable before end of packet. In this case, transmit process is placed in the suspend state and under-run error TDES0<1> is set.
3	TXJT	0b,RW	Transmit Jabber Timer Expired This bit is set when the jabber timer expired with the transmitter is still active. Transmit process will be aborted and placed in the stop state. It also causes transmit jabber timeout TDES0<14> to assert.
2	TXDU	0b,RW	Transmit Buffer Unavailable This bit is set when the DM9102 fetches the next transmit descriptor that is still owned by the host. The transmit process will be suspended until the transmit

			polling command is set or auto-polling timer time-out.
1	TXPS	0b,RW	Transmit Process Stopped This bit is set to indicate transmit process enters the stopped state.
0	TXCI	0b,RW	Transmit Complete Interrupt This bit is set when a frame is fully transmitted and the transmit status has been writen to descriptor (the TDES1<31> is also asserted). The transmit process is still running and continues to fetch next descriptor.

Note: Bits 1~16 can be cleared by writing "1"

7. Network Operation Mode Register (CR6)

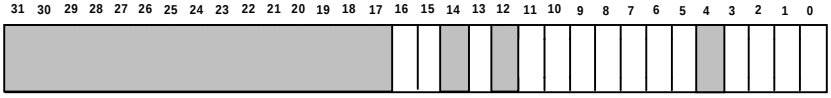


Bit	Name	Default	Description
30	RXA	0b,RW	Receive All When set, all incoming packet will be received, regardless the destination address. The address match is checked according to theCR6<7>, CR6<6>, CR6<4>, CR6<2>, CR6<0>, and RDES0<30> will show this match.
28:26	Reserved	000b,RW	Must be Zero.
25	Reserved	1b,RW	Must be One.
24:23	Reserved	00b,RW	Must be Zero.
22	TXTM	1b,RW	Transmit Threshold Mode When set, the transmit threshold mode is 10Mb/s. When reset, the threshold mode is 100Mb/s. This bit is used together with CR6<15:14> to decide the exact threshold level.
21	SFT	0b,RW	Store and Forward Transmit When set, the packet transmission from MAC will be started after a full frame has been moved from the host memory to transmit FIFO. When reset, the packet transmission's start will depend on the threshold value specified in CR6<15:14>
20	STI	0b,RW	Start Transmission Immediately When this bit is set, the packet transmission from MAC will be started immediately after transmit FIFO's threshold level reaches 16 bytes, regardless of the setting in CR6<22> and CR6<15:14>. This mode will make transmit FIFO underrun condition to happen more easily.
18:19	MBO	00b,RW	Must always write "11" to these two bits.
17	Reserved	0b,RW	Must be Zero.
16	Reserved	0b,RW	Must be Zero.

15:14	TSB	00b,RW	Threshold Bits These bits are set together with CR6<22> (chose 10Mb or 100Mb) and will decide the exact FIFO threshold level. The packet transmission will start after the data level exceeds the threshold value. Bit15 Bit14 Threshold(100M) Threshold(10M) 0 0 128 72 0 1 256 96 1 0 512 128 1 1 Reserved Reserved
13	TXSC	0b,RW	Transmit Start/stop Command When set, the transmit process will begin by fetching the transmit descriptor for available packet data to be transmitted (running state). If the fetched descriptor is owned by the host, the transmit process will enter the suspend state and transmit buffer unavailable (CR5<2>) is set. Otherwise it will begin to move data from host to FIFO and transmit out after reaching threshold level. When reset, the transmit process is placed in the stopped state after completing the transmission of the current frame.
12	FCM	0b,RW	Force Collision Mode When set, the transmission process is forced to be the collision status. Meaningful only in the internalloopback mode.
11:10	LBM	00b,RW	Loopback Mode These bits decide two loopback modes besides normal operation. External loopback mode expects transmitted data back to receive path and makes no collision detection. Bit11 Bit10 Loopback Mode 0 0 normal 0 1 internal loopback 1 x external loopback
9	FDM	0b,RW	Full-duplex Mode When auto-negotiation is disabled, this bit is set to make DM9102 operate in the full-duplex mode. Transmit and receive processes can work simultaneously. There is no collision detection needed during this mode operation.
7	PAM	0b,RW	Pass All Multicast When set, any packet with a multicast destination address is received by DM9102. The packet with a physical address will also be filtered based on the CR6<0> filter mode setting.
6	PM	1b,RW	Promiscuous mode When set, any incoming valid frame is received byDM9102, and no matter what the destination address. The DM9102 is initialized to this mode after reset operation.
5	Reserved	0b,RW	Must be Zero.
4	IAFM	0b,RO	Inverse Address Filtering Mode It is set to indicate the DM9102 operate in a Inverse Filtering Mode. This is a read only bit and mapped from the setup frame together with CR6<2>, CR6<0> setting. That is it is valid only during perfect filtering mode.
3	PBF	0b,RW	Pass Bad Frame When set, the DM9102 is indicated to receive the bad frames including runt packets, truncated frames caused by the FIFO overflow. The bad frame also has to pass the address filtering if the DM9102 is not set in promiscuous mode.

2	HOFM	0b,RO	Hash-only Filter Mode This is a read-only bit and mapped from the set-up frame together with bit4,0 of CR6. It is set to indicate the DM9102 operate in a Hash-only Filtering Mode.
1	RXRC	0b,RW	Receive Start/Stop Command When set, the receive process will begin by fetching the receive descriptor for available buffer to store the new-coming packet (placed in the running state). If the fetched descriptor is owned by the host (no descriptor is owned by the DM9102), the receive process will enter the suspend state and receive buffer unavailable CR5<7> sets. Otherwise it runs to wait for the packet's income. When reset, the receive process is placed in the stopped state after completing the reception of the current frame.
0	HPFM	0b,RO	Hash/Perfect Filter Mode This is a read only bit and mapped from the setup frame together with CR6<4>, CR6<2>. When reset, the DM9102 does a perfect address filter of incoming frames according to the addresses specified in the setup frame. When set, the DM9102 does a imperfect address filtering for the incoming frame with a multicast address according to the hash table specified in the setup frame. The filtering mode (perfect/imperfect) for the frame with a physical address will depend on CR6<2>.

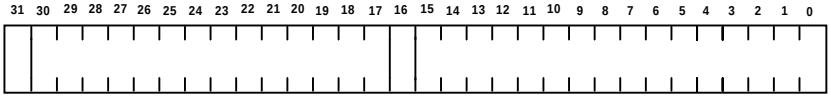
8. Interrupt Mask Register (CR7)



Bit	Name	Default	Description
16	NISE	0b,RW	Normal Interrupt Summary Enable This bit is set to enable the interrupt for Normal Interrupt Summary. Normal interrupt includes three conditions : CR5<0> – TXCI : Transmit Complete Interrupt CR5<2> – TXDU : Transmit Buffer Unavailable CR5<6> – RXCI : Receive Complete Interrupt
15	AISE	0b,RW	Abnormal Interrupt Summary Enable This bit is set to enable the interrupt for Abnormal Interrupt Summary. Abnormal interrupt includes all interrupt condition as shown below excluding Normal Interrupt conditions. They are TXPS(bit1), TXJT(bit3), TXFU(bit5), RXDU(bit7), RXPS(bit8), RXWT(bit9), TXER(bit10), GPT(bit11), SBE(bit13).
13	SBEE	0b,RW	System Bus Error Enable When set together with CR7<15>, CR5<13>, it enables the interrupt for System Bus Error. The type of system bus error is shown in CR5<24:23>.
11	GPTE	0b,RW	General-purpose Timer Expired Enable This bit is set together with CR7<15>, CR5<11> then it will enable the interrupt for the condition of the general-purpose timer (described in CR11) expired.
10	TXERE	0b,RW	Transmit Early Interrupt Enable This bit is set together with CR7<16>, CR5<10> then it enables the interrupt of the early transmit event.
9	RXWTE	0b,RW	Receive Watchdog Timer Expired Enable When this bit and CR7<15>, (CR5<9> are set together, it enable the interrupt of the condition of the receive watchdog timer expired.

8	RXPSE	0b,RW	Receive Process Stopped Enable When set together with CR7<15> and CR5<8>. This bit is set to enable the interrupt of receive process stopped condition.
7	RXDUE	0b,RW	Receive Buffer Unavailable Enable When this bit and CR7<15>, CR5<7> are set together, it will enable the interrupt of receive buffer unavailable condition.
6	RXCIE	0b,RW	Receive Complete Interrupt Enable When this bit and CR7<16>, CR5<6> are set together, it will enable the interrupt of receive process completed condition.
5	TXFUE	0b,RW	Transmit FIFO Under-run Enable When set together with CR7<15>, CR5<5>, it will enable the interrupt of the transmit FIFO under-run condition.
3	TXJTE	0b,RW	Transmit Jabber Timer Expired Enable When this bit and CR7<15>, CR5<3> are set together, it enables the interrupt of transmit Jabber Timer Expired condition.
2	TXDUE	0b,RW	Transmit Buffer Unavailable Enable When this bit and CR7<16>, CR5<2> are set together, the transmit buffer unavailable interrupt is enabled.
1	TXPSE	0b,RW	Transmit Process Stopped Enable When this bit is set together with CR7<15> and CR5<1>, it will enable the interrupt of the transmit process stopped
0	TXCIE	0b,RW	Transmit Complete Interrupt Enable When this bit and CR7<16>, CR5<0> are set, transmit interrupt is enabled.

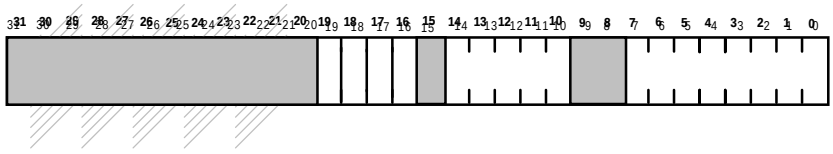
9. Statistical Counter Register (CR8)



Bit	Name	Default	Description
31	RXFU	0b,RO	Receive Overflow Counter Overflow This bit is set when the Purged Packet Counter (RXDU) has an overflow condition. It is a read only register bit.
30:17	RXDU	0000h,RO	Receive Purged Packet Counter This is a statistic counter to indicate the purged received packet count upon FIFO overflow.
16	RXPS	0b,RO	Receive Missed Counter Overflow This bit is set when the Receive Missed Frame Counter (RXCI) has an overflow condition. It is a read only register bit.
15:0	RXCI	0000h,RO	Receive Missed Frame Counter This is a statistic counter to indicate the Receive Missed Frame Count when there is a host buffer unavailable condition for receive process.

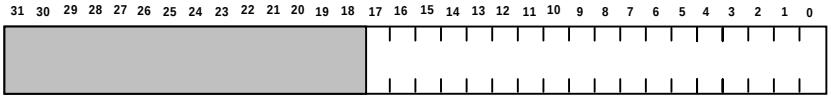
Note : CR8 is cleared after read

10. PROM & Management Access Register (CR9)



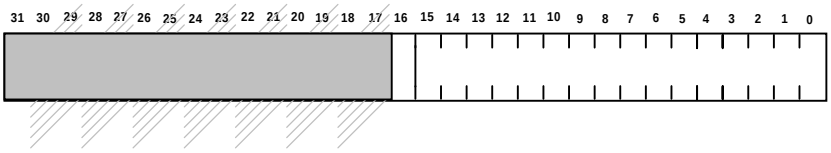
Bit	Name	Default	Description
19	MDIN	0b,RO	MII Management Data_In This is read only bit to indicate the MDIO input data.
18	MRW	0b,RW	MII Management Read/Write Mode Selection This bit defines the Read/Write Mode for MII management interface for PHY access.
17	MDOUT	0b,RW	MII Management Data_Out This bit is used to generate the output data signal for the MDIO pin.
16	MDCLK	0b,RW	MII Management Clock This bit is used to generate the output clock signal for the MDC pin.
14	MRC	0b,RW	Memory Read Control This bit is set to perform the read operation for the Boot PROM or EEPROM access.
13	EWC	0b,RW	Memory Write Control This bit is set to perform the write operation for the Boot PROM (Multiplex mode) or EEPROM access.
12	BRS	1b,RW	Boot ROM Selected This bit is set to select the Boot ROM access for memory interface.
11	ERS	0b,RW	EEPROM Selected This bit is set to select the EEPROM access for memory interface.
10	XRS	0b,RW	External Register Selected This bit is set to select an external register.
7:0	DATA	FFH,RW	Data input/output of Boot ROM This field contains the data read from or write to the Boot ROM when the Boot ROM mode is selected. (CR9<12> = 1) If EEPROM is selected (CR9<11> = 1), then CR9<3:0> are connected the serial ROM control pins.
3	CRDOUT	1b,RO	Data_Out from EEPROM This bit is set to reflect the signal status of EEDI pin when EEPROM mode is selected.
2	CRDIN	0b,RW	Data_In to EEPROM This bit is set to generate the output signal to EEDO pin when EEPROM mode is selected.
1	CRCLK	0b,RW	Clock to EEPROM This bit is set to generate the output clock to EECLK pin when EEPROM mode is selected.
0	CRCS	0b,RW	Chip_Select to EEPROM This bit is set to generate the output signal to EECS pin when EEPROM mode is selected.

11. Programming ROM Address Register (CR10)



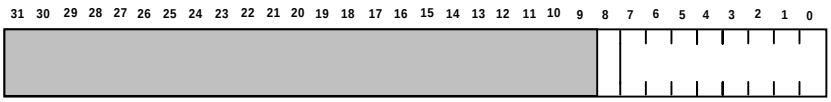
Bit	Name	Default	Description
17:0	BADR	Unpredictable	Boot ROM Address This field contains the address pointer for Boot ROM when the mode of programming by register is selected.

12. General Purpose Timer Register (CR11)



Bit	Name	Default	Description
16	TCON	0b,RW	Continuous Mode of Timer When this bit is set, the timer will continuously re-initiated upon the set time is up. When reset, the timer will be one-shot response after BCLK value is programmed.
15:0	MBCLK	0000h,RW	Multiple of Base Clock This field set the iteration number of base clock. The base clock duration is defined to be 81.92us --- for MII port/100M is selected 2us --- for MII port/10M is selected

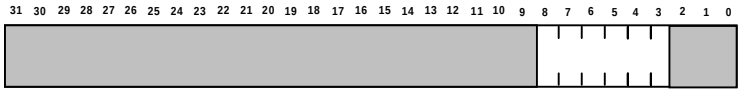
13. PHY Status Register (CR12)



Bit	Name	Default	Description
8	GEPC	X b, RW	GEPD Bits Control When in initialization, this bit is set and the unique “80h” must be written to the GEPD(7:0). After initialization, this bit is reset and it controls the functional mode of GEPD in bit0~7.
7	GEPD(7)	X b, RW	General PHY Reset Control It must be set to “1” if CR12<8> is set. When CR12<8> is reset, write “1” to this bit will reset the PHY of the DM9102.

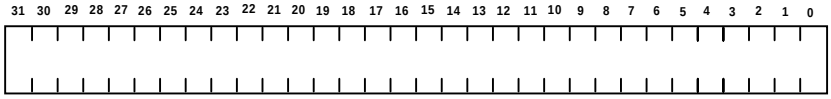
6:0	GEPD(6:0)	XXXXXXX b ,RW	General PHY Status When CR12<8> is set at initialization, it operates the only write operation and write the unique "0000000" to these seven bits. After initialization, CR12<8> is reset, write operation is meaningless and read these seven bits to indicate the PHY status. These status bits are shown below. bit 6:UTP-SIG bit 5:Signal Detection bit 4:RX-lock bit 3:Link status (the same as bit2 of PHY Register) bit 2:Full-duplex bit 1:Speed 100Mbps link bit 0:Speed 10Mbps link

14. Access Register (CR13)

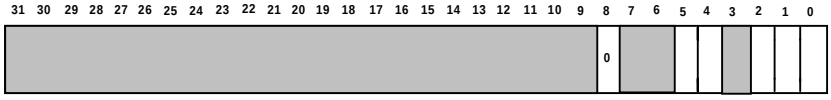


register	general definition	bit8 ~ 3	R/W
TxFIFO	transmit FIFO access port	32h	r/w
RxFIFO	receive FIFO access port	35h	r/w
DiagReset	general reset for diagnostic pointer port	38h	w

15. Data Register (CR14)



16. Watchdog and Jabber Timer Register (CR15)



Bit	Name	Default	Description
8	Reserved	0b,RW	Must be Zero.
5	TWDR	0b,RW	Time Interval of Watchdog Release This bit is used to select the time interval between receive Watchdog timer expiration until re-enabling of the receive channel. When this bit is set, the time interval is 40~48 bits time. When this bit is reset, it is 16~24 bits time.
4	TWDE	0b,RW	Watchdog Timer Disable When set, the Watchdog Timer is disabled. Otherwise it is enabled.

2	JC	0b,RW	Jabber Clock When set, the transmission is cut off after a range of 2048 bytes to 2560 bytes is transmitted. When reset, transmission for the 10Mbps port is cut off after a range of 26ms to 33ms. When reset, transmission for the 100Mbps port is cut off after a range of 2.6ms to 3.3ms.
1	TUNJ	0b,RW	Transmit Un-jabber Interval This bit is used to select the time interval between the transmit jabber timer expiration until re-enabling of the transmit channel. When set, the transmit channel is released right after the jabber expiration. When reset, the time interval is 365~420ms for 10Mb/s port and 36.5~42.0ms for 100Mb/s.
0	TJE	0b,RW	Transmit Jabber Disable When set, the transmit Jabber Timer is disabled. Otherwise it is enabled.

✧ **PHY Management Register Set**

Register Address	Register Name	Description
0	BMCR	Basic Mode Control Register
1	BMSR	Basic Mode Status Register
2	PHYIDR1	PHY Identifier Register #1
3	PHYIDR2	PHY Identifier Register #2
4	ANAR	Auto-Negotiation Advertisement Register
5	ANLPAR	Auto-Negotiation Link Partner Ability Register
6	ANER	Auto-Negotiation Expansion Register
7-15	Reserved	Reserved
16	DSCR	DAVICOM Specified Configuration Register
17	DSCSR	DAVICOM Specified Configuration/Status Register
18	10BTCSR	10BASE-T Configuration/Status Register
Others	Reserved	Reserved For Future Use-Do Not Read/Write To These Registers

Key to Default

In the register description that follows, the default column takes the form:
<Reset Value>, <Access Type> / <Attribute(s)>
Where：
<Reset Value>:
- 1 Bit set to logic one
- 0 Bit set to logic zero
- X No default value
- (PIN#) Value latched in from pin # at reset

<Access Type>:
- RO = Read only
- RW = Read/Write

<Attribute (s)>:
- SC = Self clearing
- P = Value permanently set
- LL = Latching low
- LH = Latching high

Basic Mode Control Register (BMCR) - Register 0

Bit	Name	Default	Description
0.15	Reset	0b, RW/SC	Reset: 1=Software reset 0=Normal operation This bit sets the status and controls the PHY registers of DM9102 to their default states. This bit, which is self-clearing, will keep returning a value of one until the reset process is completed
0.14	Loopback	0b, RW	Loopback: Loop-back control register 1=Loop-back enabled 0=Normal operation When in 100Mbps operation mode, setting this bit may cause the descrambler to lose synchronization and produce a 720ms "dead time" before any valid data appear at the MII receive outputs
0.13	Speed Selection	1b, RW	Speed Select: 1=100Mbps 0=10Mbps Link speed may be selected either by this bit or by Auto-negotiation. When Auto-negotiation is enabled and bit 12 is set, this bit will return Auto-negotiation selected media type.
0.12	Auto-negotiation Enable	1b, RW	Auto-negotiation Enable: 1= Auto-negotiation enabled: bit 8 and 13 will be in Auto-negotiation status 0= Auto-negotiation disabled: bit 8 and 13 will determine the link speed and mode
0.11	Power Down	0b, RW	Power Down: Setting this bit will power down the whole chip except crystal oscillator circuit. 1=Power Down 0=Normal Operation
0.10	Isolate	(PHYAD=00000b) ,RW	Isolate: 1= Isolates the DM9102 from the MII with the exception of the serial management. 0= Normal Operation
0.9	Restart Auto-negotiation	0b,RW/SC	Restart Auto-negotiation: 1= Restart Auto-negotiation. Re-initiates the Auto-negotiation process. When Auto-negotiation is disabled (bit 12 of this register cleared), this bit has no function and it should be cleared. This bit is self-clearing and it will keep returning a value of 1 until Auto-negotiation is initiated by the DM9102. The operation of the Auto-negotiation process will not be affected by the management entity that clears this bit 0= Normal Operation
0.8	Duplex Mode	1b,RW	Duplex Mode: 1= Full Duplex operation. Duplex selection is allowed when Auto-negotiation is disabled (bit 12 of this register is cleared). With Auto-negotiation enabled, this bit reflects the duplex capability selected by Auto-negotiation 0= Normal operation

0.7	Collision Test	0b,RW	Collision Test: 1= Collision Test enabled. When set, this bit will cause the COL signal to be asserted in response to the assertion of TX_EN 0= Normal Operation
0.6:0.0	Reserved	0000000b,RO	Reserved: Write as 0, ignore on read

Basic Mode Status Register (BMSR) - Register 1

Bit	Name	Default	Description
1.15	100BASE-T4	0b,RO/P	100BASE-T4 Capable: 1=DM9102 is able to perform in 100BASE-T4 mode 0=DM9102 is not able to perform in 100BASE-T4 mode
1.14	100BASE-TX Full Duplex	1b,RO/P	100BASE-TX FULL DUPLEX CAPABLE: 1= DM9102 able to perform 100BASE-TX in Full Duplex mode 0= DM9102 not able to perform 100BASE-TX in Full Duplex mode
1.13	100BASE-TX Half Duplex	1b,RO/P	100BASE-TX Half Duplex Capable: 1=DM9102 is able to perform 100BASE-TX in Half Duplex mode 0=DM9102 is not able to perform 100BASE-TX in Half Duplex mode
1.12	10BASE-T Full Duplex	1b,RO/P	10BASE-T Full Duplex Capable: 1=DM9102 is able to perform 10BASE-T in Full Duplex mode 0=DM9102 is not able to perform 10BASE-T in Full Duplex mode
1.11	10BASE-T Half Duplex	1b,RO/P	10BASE-T Half Duplex Capable: 1=DM9102 is able to perform 10BASE-T in Half Duplex mode 0=DM9102 is not able to perform 10BASE-T in Half Duplex mode
1.10-1.7	Reserved	0000b ,RO	Reserved: Write as 0, ignore on read
1.6	MF Preamble Suppression	0b,RO	MII Frame Preamble Suppression: 1=PHY will accept management frames with preamble suppressed 0=PHY will not accept management frames with preamble suppressed
1.5	Auto-negotiation Complete	0b,RO	Auto-negotiation Complete: 1=Auto-negotiation process completed 0=Auto-negotiation process not completed
1.4	Remote Fault	0b, RO/LH	Remote Fault: 1= Remote fault condition detected (cleared on read or by a chip reset). Fault criteria and detection method is DM9102 implementation specific. This bit will set after the RF bit in the ANLPAR (bit 13, register address 05) is set 0= No remote fault condition detected
1.3	Auto-negotiation Ability	1b,RO/P	Auto Configuration Ability: 1=DM9102 able to perform Auto-negotiation 0=DM9102 not able to perform Auto-negotiation
1.2	Link Status	0b ,RO/LL	Link Status: 1=Valid link established (for either 10Mbps or 100Mbps operation) 0=Link not established The link status bit is implemented with a latching function, so that the occurrence of a link failure condition causes the Link Status bit to be cleared and remain cleared until it is read via the management interface
1.1	Jabber Detect	0b,	Jabber Detect:

		RO/LH	1=Jabber condition detected 0=No jabber This bit is implemented with a latching function. Jabber conditions will set this bit unless it is cleared by a read to this register through a management interface or a DM9102 reset. This bit works only in 10Mbps mode
1.0	Extended Capability	1b,RO/P	Extended Capability: 1=Extended register capability 0=Basic register capability only

PHY ID Identifier Register #1 (PHYIDR1) - Register 2

The PHY Identifier Registers #1 and #2 work together in a single identifier of the DM9102. The Identifier consists of a concatenation of the Organizationally Unique Identifier (OUI), a vendor's model number, and a model revision number. DAVICOM Semiconductor's IEEE assigned OUI is 00606E.

Bit	Name	Default	Description
2.15-2.0	OUI_MSB	<0181H>	OUI Most Significant Bits: This register stores bit 3 to 18 of the OUI (00606E) to bit 15 to 0 of this register respectively. The most significant two bits of the OUI are ignored (the IEEE standard refers to these as bit 1 and 2)

PHY Identifier Register #2 (PHYIDR2) - Register 3

Bit	Name	Default	Description
3.15-3.10	OUI_LSB	<101110b> ,RO/P	OUI Least Significant Bits: Bit 19 to 24 of the OUI (00606E) are mapped to bit 15 to 10 of this register respectively
3.9-3.4	VNDR_MDL	<000000b> ,RO/P	Vendor Model Number: Six bits of vendor model number mapped to bit 9 to 4 (most significant bit to bit 9)
3.3-3.0	MDL_REV	<0000b>,RO/P	Model Revision Number: Four bits of vendor model revision number mapped to bit 3 to 0 (most significant bit to bit 3)

Auto-negotiation Advertisement Register (ANAR) - Register 4

This register contains the advertised abilities of this DM9102 device as they will be transmitted to its link partner during Auto-negotiation.

Bit	Name	Default	Description
4.15	NP	0b,RO/P	Next Page Indication: 0=No next page available 1=Next page available The DM9102 has no next page, so this bit is permanently set to 0
4.14	ACK	0b,RO	Acknowledge: 1=Link partner ability data reception acknowledged 0=Not acknowledged The DM9102's Auto-negotiation state machine will automatically control this bit in the outgoing FLP bursts and set it at the appropriate time during the Auto-negotiation process. Software should not attempt to write to this bit.
4.13	RF	0b, RW	Remote Fault: 1=Local Device senses a fault condition

			0=No fault detected
4.12-4.11	Reserved	00b, RW	Reserved: Write as 0, ignore on read
4.10	FCS	0b, RW	Flow Control Support: 1=Controller chip supports flow control ability 0=Controller chip doesn't support flow control ability
4.9	T4	0b, RO/P	100BASE-T4 Support: 1=100BASE-T4 supported by the local device 0=100BASE-T4 not supported The DM9102 does not support 100BASE-T4 so this bit is permanently set to 0
4.8	TX_FDX	1b, RW	100BASE-TX Full Duplex Support: 1=100BASE-TX Full Duplex supported by the local device 0=100BASE-TX Full Duplex not supported
4.7	TX_HDX	1b, RW	100BASE-TX Support: 1=100BASE-TX supported by the local device 0=100BASE-TX not supported
4.6	10_FDX	1b, RW	10BASE-T Full Duplex Support: 1=10BASE-T Full Duplex supported by the local device 0=10BASE-T Full Duplex not supported
4.5	10_HDX	1b, RW	10BASE-T Support: 1=10BASE-T supported by the local device 0=10BASE-T not supported
4.4-4.0	Selector	<00001b>, RW	Protocol Selection Bits: These bits contain the binary encoded protocol selector supported by this node. <00001> indicates that this device supports IEEE 802.3 CSMA/CD.

Auto-negotiation Link Partner Ability Register (ANLPAR) - Register 5

This register contains the advertised abilities of the link partner when received during Auto-negotiation.

Bit	Name	Default	Description
5.15	NP	0b, RO	Next Page Indication: 0= Link partner, no next page available 1= Link partner, next page available
5.14	ACK	0b, RO	Acknowledge: 1=Link partner ability data reception acknowledged 0=Not acknowledged The DM9102's Auto-negotiation state machine will automatically control this bit from the incoming FLP bursts. Software should not attempt to write to this bit.
5.13	RF	0b, RO	Remote Fault: 1=Remote fault indicated by link partner 0=No remote fault indicated by link partner
5.12-5.10	Reserved	000b, RO	Reserved: Write as 0, ignore on read
5.9	T4	0b, RO	100BASE-T4 Support: 1=100BASE-T4 supported by the link partner 0=100BASE-T4 not supported by the link partner
5.8	TX_FDX	0b, RO	100BASE-TX Full Duplex Support:

			1=100BASE-TX Full Duplex supported by the link partner 0=100BASE-TX Full Duplex not supported by the link partner
5.7	TX_HDX	0b, RO	100BASE-TX Support: 1=100BASE-TX Half Duplex supported by the link partner 0=100BASE-TX Half Duplex not supported by the link partner
5.6	10_FDX	0b, RO	10BASE-T Full Duplex Support: 1=10BASE-T Full Duplex supported by the link partner 0=10BASE-T Full Duplex not supported by the link partner
5.5	10_HDX	0b, RO	10BASE-T Support: 1=10BASE-T Half Duplex supported by the link partner 0=10BASE-T Half Duplex not supported by the link partner
5.4-5.0	Selector	<00000b>, RO	Protocol Selection Bits: Link partner's binary encoded protocol selector

Auto-Negotiation Expansion Register (ANER)-Register 6

Bit	Name	Default	Description
6.15-6.5	Reserved	0b, RO	Reserved: Write as 0, ignore on read
6.4	PDF	0b, RO/LH	Local Device Parallel Detection Fault: PDF=1: A fault detected via parallel detection function. PDF=0: No fault detected via parallel detection function
6.3	LP_NP_ABLE	0b, RO	Link Partner Next Page Able: LP_NP_ABLE=1: Link partner, next page available LP_NP_ABLE=0: Link partner, no next page
6.2	NP_ABLE	0b,RO/P	Local Device Next Page Able: NP_ABLE=1: DM9102, next page available NP_ABLE=0: DM9102, no next page DM9102 does not support this function, so this bit is always 0.
6.1	PAGE_RX	0b, RO/LH	New Page Received: A new link code word page received. This bit will be automatically cleared when the register (Register 6) is read by management
6.0	LP_AN_ABLE	0b, RO	Link Partner Auto-negotiation Able: A "1" in this bit indicates that the link partner supports Auto-negotiation.

DAVICOM Specified Configuration Register (DSCR) - Register 16

Bit	Name	Default	Description
16.15:16.13	Reserved	0b, RW	Reserved
16.12	Reserved	0b, RW	This bit must set to be 0.
16.11	Reserved	0b, RW	This bit must set to be 0
16.10	TX	1b, RW	This bit must set to be 1
16.9	UTP	1b, RW	UTP Cable Control: 1=The media is a UTP cable, 0=STP
16.8	Reserved	0b, RW	Reserved
16.7	F_LINK_100	0b, RW	Force Good Link in 100Mbps: 0=Normal 100Mbps operation 1=Force 100Mbps good link status This bit is useful for diagnostic purposes.
16.6	Reserved	1b, RW	This bit must forced to be 1.

16.5	LED_CTL	0b,RW	LED Mode Select: (control LEDTRF, LED100M, LED10M) 0 = LEDTRF is Activity LED, and LED100M indicates good link to 100Mbps, LED10M indicates good link to 10Mbps . 1 = LEDTRF is no use, LED100M, LED10M indicate Link and Activity. When good links to 100Mbps, LED100M actives and flashes if any traffic exists. When good links to 10Mbps, LED10M actives and flashes if any traffic exists.
16.4	Reserved	0b,RW	This bit must forced to be 0
16.3	SMRST	0b,RW	Reset State Machine: When write 1 to this bit, all state machines of PHY will be reset. This bit is self-clear after reset is completed.
16.2	MFPSC	0b,RW	MF Preamble Suppression Control: MII frame preamble suppression control bit 1 = MF preamble suppression bit on 0 = MF preamble suppression bit off
16.1	SLEEP	0b,RW	Sleep Mode: Writing a 1 to this bit will cause PHY entering the Sleep mode and power down all circuit except oscillator and clock generator circuit. When waking up from Sleep mode (write this bit to 0), the configuration will go back to the state before sleep; but the state machine will be reset
16.0	RLOUT	0b,RW	Remote Loop out Control: When this bit is set to 1, the received data will loop out to the transmit channel. This is useful for bit error rate testing

DAVICOM Specified Configuration and Status Register (DSCSR) - Register 17

Bit	Name	Default	Description
17.15	100FDX	1b, RO	100M Full Duplex Operation Mode: After Auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 100Mbps Full Duplex mode. The software can read bit[15:12] to see which mode is selected after Auto-negotiation. This bit is invalid when it is not in the Auto-negotiation mode.
17.14	100HDX	1b, RO	100M Half Duplex Operation Mode: After auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 100Mbps half-duplex mode. The software can read bit[15:12] to see which mode is selected after Auto-negotiation. This bit is invalid when it is not in the Auto-negotiation mode.
17.13	10FDX	1b, RO	10M Full Duplex Operation Mode: After auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 10Mbps Full Duplex mode. The software can read bit[15:12] to see which mode is selected after Auto-negotiation. This bit is invalid when it is not in the Auto-negotiation mode.
17.12	10HDX	1b, RO	10M Half Duplex Operation Mode: After Auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 10Mbps Half Duplex mode. The software can read bit[15:12] to see which mode is selected after Auto-negotiation. This bit is invalid when it is not in the Auto-negotiation mode.

17.11-17.9	Reserved	000b, RW	Reserved: Write as 0, ignore on read
17.8-17.4	PHYAD[4:0]	00001b, RW	PHY Address Bit 4:0: The first PHY address bit transmitted or received is the MSB of the address (bit 4). A station management entity connected to multiple PHY entities must know the appropriate address of each PHY. A PHY address of <00000> will cause the isolate bit of the BMCR (bit 10, Register Address 00) to be set.
17.3-17.0	ANMB[3:0]	0000b, RO	Auto-negotiation Monitor Bits: These bits are for debug only. The Auto-negotiation status will be written to these bits. b3 b2 b1 b0 0 0 0 0 In IDLE state 0 0 0 0 Ability match 0 0 1 0 Acknowledge match 0 0 1 1 Acknowledge match fail 0 1 0 0 Consistency match 0 1 0 1 Consistency match fail 0 1 1 0 Parallel detects signal_link_ready 0 1 1 1 Parallel detects signal_link_ready fail 1 0 0 0 Auto-negotiation completed successfully

10BASE-T Configuration/Status (10BTCSRCSR) - Register 18

Bit	Name	Default	Description
18.15	Reserved	0b, RO	Reserved: Write as 0, ignore on read
18.14	LP_EN	1b, RW	Link Pulse Enable: 1=Transmission of link pulses enabled 0=Link pulses disabled, good link condition forced This bit is valid only in 10Mbps operation.
18.13	HBE	1b,RW	Heartbeat Enable: 1=Heartbeat function enabled 0=Heartbeat function disabled When the DM9102 is configured for Full Duplex operation, this bit will be ignored (the collision/heartbeat function is invalid in Full Duplex mode). It must set to be 1.
18.12	Reserved	0b, RO	Reserved: Write as 0, ignore on read
18.11	JABEN	1b, RW	Jabber Enable: Enables or disables the Jabber function when the DM9102 is in 10BASE-T Full Duplex or 10BASE-T Transceiver Loopback mode 1= Jabber function enabled 0= Jabber function disabled
18.10	Reserved	0b,RW	Reserved
18.9-18.1	Reserved	0b, RO	Reserved
18.0	Reserved	0b, RO	Reserved

■ Functional Description

✧ System Buffer Management

1. Overview

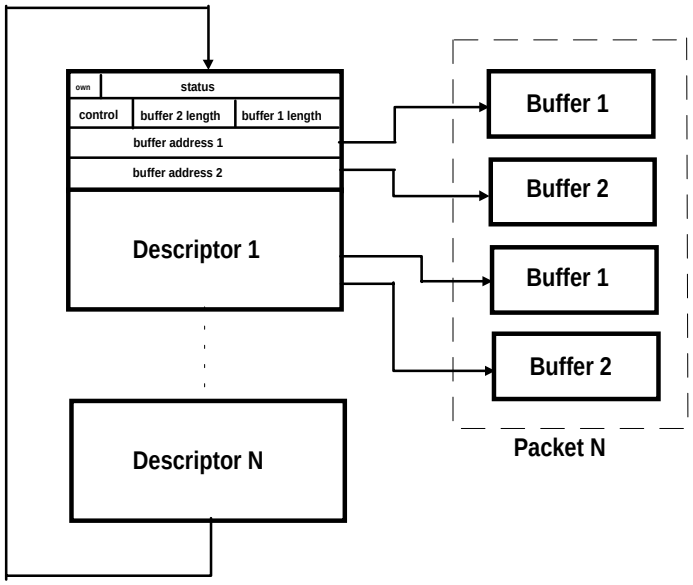
The data buffers for reception and transmission which data reside in the host memory. They are directed with the descriptor lists that are located in another region of the host memory. All actions for the buffer management are operated by the DM9102 in conjunction with the driver. The data structures and processing algorithms are described in the following text.

2. Data Structure and Descriptor List

There are two types of buffers that reside in the host memory, the transmit buffer and the receive buffer. The buffers are composed of many distributed regions in the host memory. They are linked together and controlled by the descriptor lists that reside in another region of the host memory. The content of each descriptor includes pointer to the buffer, count of the buffer, command and status for the packet to be transmitted or received. Each descriptor list starts from the address setting of CR3 (receive descriptor base address) and CR4 (transmit descriptor base address). The descriptor lists have two types of structure, Ring structure and Chain structure.

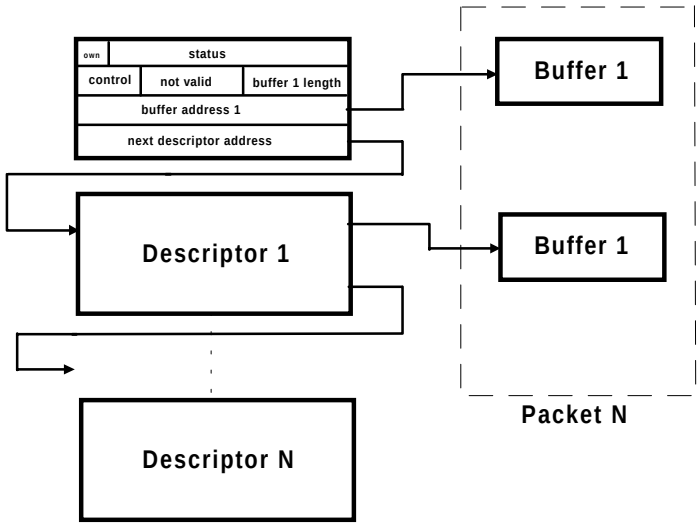
3. Buffer Management: Ring Structure Method

As the Ring structure depicted below, the descriptors are linked directly one after another. The first and last descriptor on the list has the necessary information for the DM9102 to return to the beginning of the list after the bottom descriptor is accessed. Each descriptor points to the two buffer regions and one packet may cross many descriptor boundaries.



4. Buffer Management: Chain Structure Method

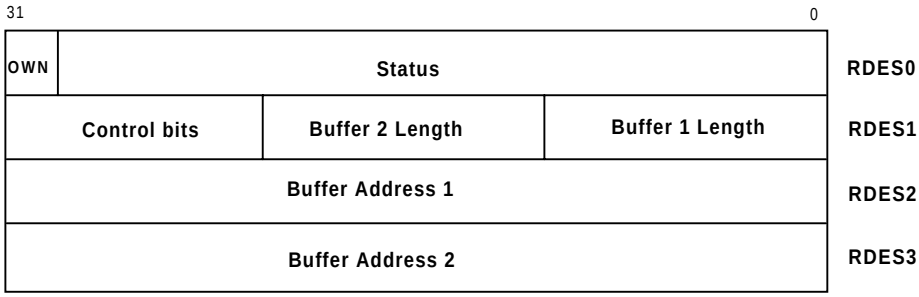
As the Chain structure depicted below, each descriptor contains two pointers, one point to a single buffer and the other to the next descriptor chained. The first descriptor is chained with the last descriptor under host driver's control. With this structure, a descriptor can be allocated anywhere in host memory and is chained to the next descriptor. The Chain Structure and the Ring Structure may be combined to make the buffer structure more flexible.



5. Descriptor List: Buffer Descriptor Format

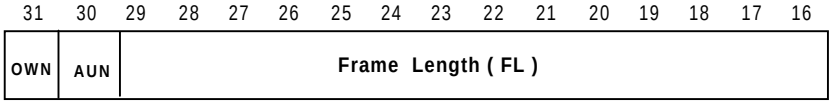
(a). Receive Descriptor Format

Each receive descriptor has four double-word entries and may be read or written by the host or the DM9102. The descriptor format is shown below with a detailed functional description.



Receive Descriptor Format

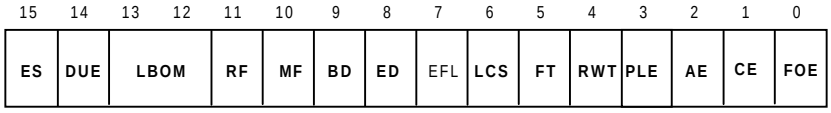
RDES0: Owner bit with receive status



OWN: 1=owned by DM9102, 0=owned by host
This bit should be reset after packet reception is completed. It will be set by the host after received data are removed.

FL: Frame length indicating total byte count of received packet.

AUN: Received address unmatched.



This word-wide content includes status of received frame. They are loaded after the received buffer that belongs to the corresponding descriptor is full. All status bits are valid only when the last descriptor (End Descriptor) bit is set.

Bit 15: ES, Error Summary
It is set for the following error conditions: Descriptor Unavailable Error (DUE =1), Runt Frame (RF=1), Excessive Frame Length (EFL=1), Late Collision Seen (LCS=1), CRC error (CE=1), FIFO Overflow error (FOE=1). Valid only when ED is set.

Bit 14: DUE, Descriptor Unavailable Error
It is set when the frame is truncated due to the buffer unavailable. It is valid only when ED is set.

Bit 13,12: LBOM, Loopback Operation Mode
These two bits show the received frame is derived from
00 --- normal operation
01 --- internal loopback
10 --- external loopback
11 --- reserved

Bit 11: RF, Runt Frame
It is set to indicate the received frame has the size smaller than 64 bytes. Valid only when ED is set and FOE is reset.

Bit 10: MF, Multicast Frame
It is set to indicate the received frame has a multicast address. Valid only when ED is set.

Bit 9: BD, Begin Descriptor
This bit is set for the descriptor indicating start of a received frame.

Bit 8: ED, Ending Descriptor
This bit is set for the descriptor indicates end of a received frame.

Bit 7: EFL, Excessive Frame Length
It is set to indicate the received frame length exceeds 1518 bytes. Valid only when ED is set.

Bit 6: LCS: Late Collision Seen
It is set to indicate a late collision found during the frame reception. Valid only when ED is set.

Bit 5: FT, Frame Type
It is set to indicate the received frame is the Ethernet-type. It is reset to indicate the received frame is the EEE802.3- type. Valid only when ED is set

Bit 4: RWT, Receive Watchdog Timeout
It is set to indicate receive Watchdog time-out during the frame reception. CR5<9> will also be set. Valid only when ED is set.

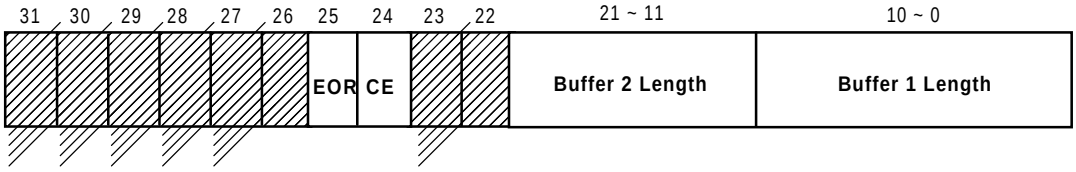
Bit 3: PLE, Physical Layer Error
It is set to indicate a physical layer error found during the frame reception.

Bit 2: AE, Alignment Error
It is set to indicate the received frame ends with a non-byte boundary.

Bit 1: CE, CRC Error
It is set to indicate the received frame ends with a CRC error. Valid only when ED is set.

Bit 0: FOE, FIFO Overflow Error
This bit is valid for Ending Descriptor is set. (ED = 1)
It is set to indicate a FIFO Overflow error happens during the frame reception.

RDES1: Descriptor Status and Buffer Size



Bit 25: EOR, End of Ring
Set to indicate that the descriptor is located on the bottom of the descriptor list.

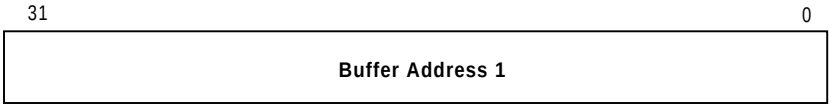
Bit 24: CE, Chain Enable
Set to indicate that the second address is the chained descriptor instead of the other buffer.
Used as the indication of the Chain structure.

Bit 21-11: Buffer 2 Length
Indicates the size of the second buffer. It has no meaning in chain type descriptor.

Bit 10-0: Buffer 1 Length
Indicates the size of the first buffer in Ring type structure and single buffer in Chain type structure.

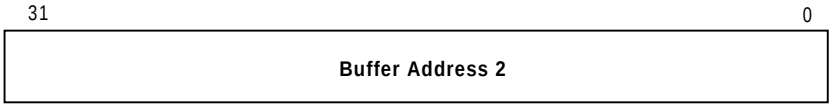
RDES2: Buffer 1 Starting Address

Indicates the physical starting address of buffer 1.



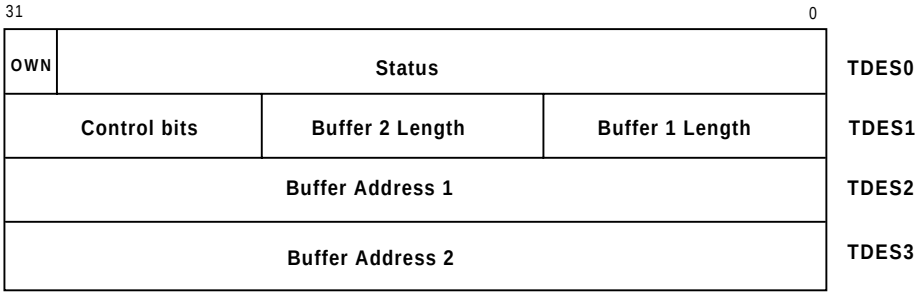
RDES3: Buffer 2 Starting Address

Indicates the physical starting address of buffer 2 under the Ring structure and that of the chained descriptor under the Chain descriptor structure.



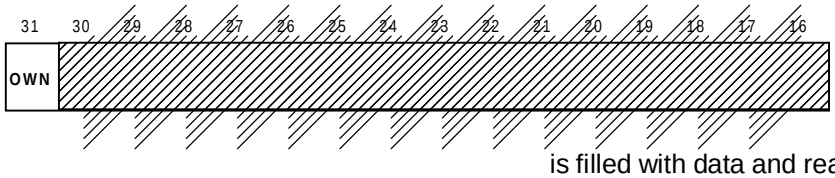
(b). Transmit Descriptor Format

Each transmit descriptor has four doubleword content and may be read or written by the host or by the DM9102. The descriptor format is shown below with detailed description.

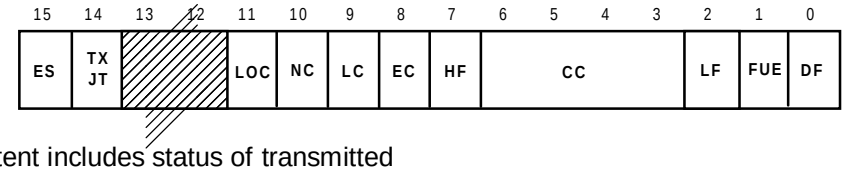


Transmit Descriptor Format

TDES0: Owner Bit with Transmit Status



Bit 31: OWN,
1=owned by DM9102, 0=owned by host, this bit should be set when the transmitting buffer is filled with data and ready to be transmitted. It will be reset by DM9102 after transmitting the whole data buffer.



This word wide content includes status of transmitted frame. They are loaded after the data buffer that belongs to the corresponding descriptor is transmitted.

Bit 15: ES, Error Summary
It is set for the following error conditions: Transmit Jabber Time-out (TXJT=1), Loss of Carrier (LOC=1), No Carrier (NC=1), Late Collision (LC=1), Excessive Collision (EC=1), FIFO Underrun Error (FUE=1).

Bit 14: TXJT, Transmit Jabber Time Out
It is set to indicate the transmitted frame is truncated due to transmit jabber time out condition. The transmit jabber time out interrupt CR5<3> is set.

Bit 11: LOC, Loss of Carrier
It is set to indicate the loss of carrier during the frame transmission, not valid in internal loopback mode.

Bit 10: NC, No Carrier
It is set to indicate that no carrier signal from transceiver is found, not valid in internal loopback mode.

Bit 9: LC, Late Collision
It is set to indicate a collision occurs after the collision window of 64 bytes. Not valid if FUE is set.

Bit 8: EC, Excessive collision
It is set to indicate the transmission is aborted due to 16 excessive collisions.

Bit 7: HF, Heartbeat Fail
It is set to indicate the Heartbeat check failed after complete transmission. Not valid if FUE is set. When TDES0<14> is set, this bit is not valid.

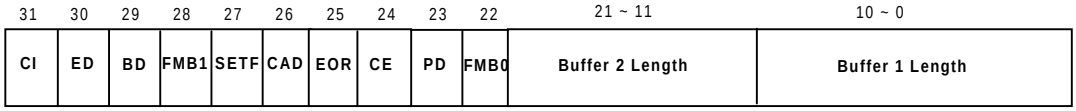
Bits 6-3: CC, Collision Count
These bits show the number of collision before transmission. Not valid if excessive collision bit is also set.

Bit 2: LF, Link test Fail
It is set to indicate the link test fails before the frame transmission.

Bit 1: FUE, FIFO Underrun Error
It is set to indicate the transmission aborted due to transmit FIFO underrun condition.

Bit 0: DF, Deferred
It is set to indicate the frame is deferred before ready to transmit.

TDES1: Transmit buffer control and buffer size



Bit 31: CI, Completion Interrupt
It is set to enable transmit interrupt after the present frame has been transmitted. It is valid only when TDES1<30> is set or when it is a setup frame.

Bit 30: ED, Ending Descriptor
It is set to indicate the pointed buffer contains the last segment of a frame.

Bit 29: BD, Begin Descriptor
It is set to indicate the pointed buffer contains the first segment of a frame.

Bit 28: FMB1, Filtering Mode Bit 1
This bit is used with FMB0 to indicate the filtering type when the present frame is a setup frame.

Bit 27: SETF, Setup Frame
It is set to indicate the current frame is a setup frame.

Bit 26: CAD, CRC Append Disable
It is set to disable the CRC appending at the end of the transmitted frame. Valid only when TDES1<29> is set.

Bit 25: EOR, End of Ring Descriptor
It is set to indicate the descriptor is located on the bottom of the descriptor list.

Bit 24: CE, Chain Enable
This bit is set to indicate the second address (TDES3) is the chained descriptor instead of the other buffer. It is used as the indication of the Chain structure. When reset, it indicates the Ring structure.

Bit 23: PD, Padding Disable
This bit is set to disable the padding field for a packet shorter than 64 bytes.

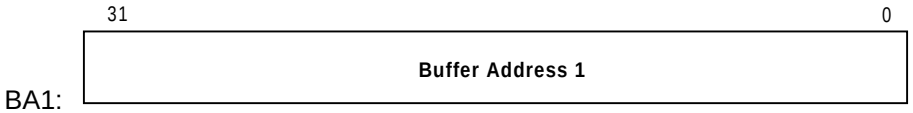
Bit 22: FMB0, Filtering Mode Bit 0
This bit is used with FMB1 to indicate the filtering type when the present frame is a setup frame.

FMB1	FMB0	Filtering Type
0	0	Perfect Filtering
0	1	Hash Filtering
1	0	Inverse Filtering
1	1	Hash-Only Filtering

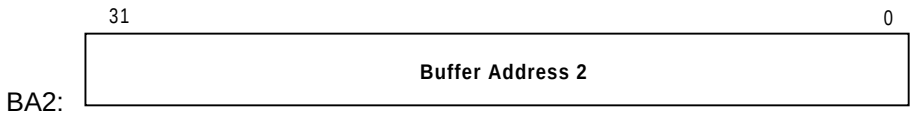
Bits 21-11: Buffer 2 length
Indicates the size of second buffer. It has no meaning with chain structure descriptor type.

Bit 10-0: Buffer 1 length
Indicates the size of the first buffer in Ring type structure and single buffer in Chain type structure.

TDES2 : Buffer 1 Starting Address indicates the physical starting address of buffer 1.



TDES3 : Buffer 2 Starting Address indicates the physical starting address of buffer 2 under the Ring structure.



Initialization Procedure

After hardware or software reset, transmit and receive processes are placed in the STOP state. The DM9102 can accept the host commands to start operation. The general procedure for initialization is described below:

(1) Read/write suitable values for the PCI configuration registers.
(2) Write CR3 and CR4 to provide the starting address of each descriptor list.
(3) Write CR0 to set global host bus operation parameters.
(4) Write CR7 to mask unnecessary interrupt causes.
(5) Write CR6 to set global parameters and start both the receive and transmit processes. The receive and transmit processes will enter the running state and attempt to acquire descriptors from the respective descriptor lists.
(6) Wait for any interrupt.

Data Buffer Processing Algorithm

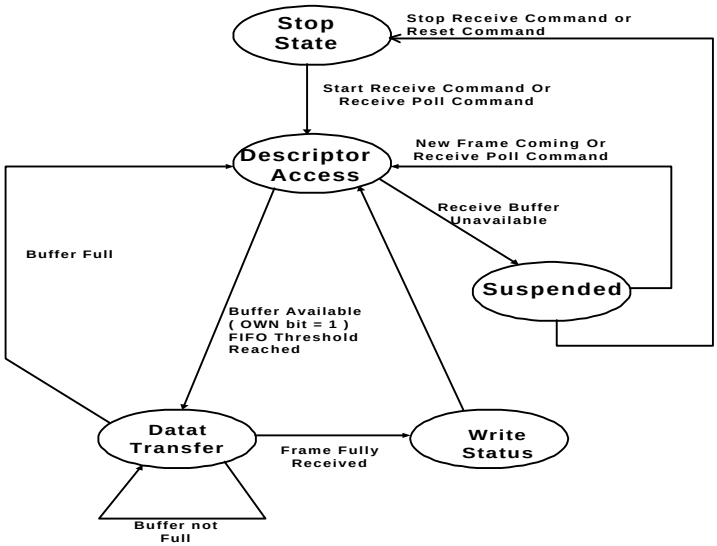
The data buffer process algorithm is based on the cooperation of the host and the DM9102. The host sets CR3 (receive descriptor base address) and CR4 (transmit descriptor base address) for the descriptor list initialization. The DM9102 will start the data buffer transfer after the descriptor polling and get the ownership. For detailed processing procedure, please see below.

1. Receive Data Buffer Processing

The DM9102 always attempts to acquire an extra descriptor in anticipation of the incoming frames. Any incoming frame size covers a few buffer regions and descriptors. The following conditions satisfy the descriptor acquisition attempt:

- When start/stop receive sets immediately after being placed in the running state.
- When the DM9102 begins writing frame data to a data buffer pointed to by the current descriptor and the buffer ends before the frame ends.
- When the DM9102 completes the reception of a frame and the current receive descriptor is closed.
- When receive process is suspended due to no free buffer for the DM9102 and a new frame is received.
- When receive poll demand is issued.

After acquiring the free descriptor, the DM9102 processes the incoming frame and places it in the acquired descriptor's data buffer. When the whole received frame data has been transferred, the DM9102 will write the status information to the last descriptor. The same process will repeat until it encounters a descriptor flagged as being owned by the host. If this occurs, receive process enters the suspended state and waits the host to service.

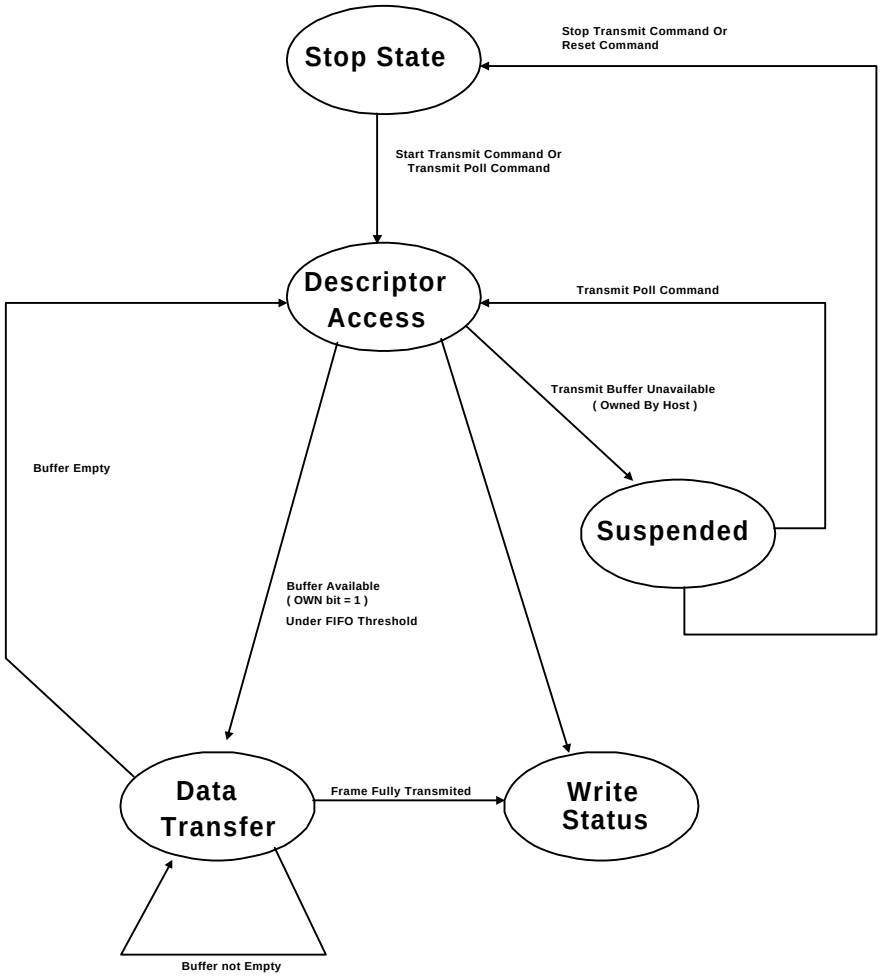


Receive Buffer Management State Transition

2. Transmit Data Buffer Processing

When start/stop transmit command is set and the DM9102 is in running state, transmit process polls transmit descriptor list for frames requiring transmission. When it completes a frame transmission, the status related to the transmitted frame will be written into the transmit descriptor. If the DM9102 detects a descriptor flagged as owned by the host and no transmit buffers are available, transmit process will be suspended. While in the running state, transmit process can simultaneously acquire two frames. As transmit process completes copying the first frame, it immediately polls the transmit descriptor list for the second frame. If the second frame is valid, transmit process copies the frame before writing the status information of the first frame.

Both conditions below will make transmit process be suspended: (i) The DM9102 detects a descriptor owned by the host. (ii) A frame transmission is aborted when a locally induced error is detected. Under either condition, the host driver has to service the condition before the DM9102 can resume.



Transmit Buffer Management State Transition

✧ Network Function

1. Overview

This chapter will introduce the normal state machine operation and MAC layer management like collision backoff algorithm. In transmit mode, the DM9102 initiates a DMA cycle to access data from a transmit buffer. It prefaces the data with the preamble, the SFD pattern, and it appends a 32-bit CRC. In receive mode, the data is de-serialized by receive mechanism and fed into the internal FIFO. For detailed process, please see below.

2. Receive Process and State Machine

a. Reception Initiation
As a preamble being detected on the receive data lines, the DM9102 synchronizes itself to the data stream during the preamble and waits for the SFD. The synchronization process is based on byte boundary and the SFD byte is 10101011. If the DM9102 receives a 00 or a 11 after the first 8 preamble bits and before receiving the SFD, the reception process will be terminated.

b. Address Recognition
After initial synchronization, the DM9102 will recognize the 6-byte destination address field. The first bit of the destination address signifies whether it is a physical address (=0) or a multicast address (=1). The DM9102 filters the frame based on the node address of receive address filter setting. If the frame passes the filter, the subsequent serial data will be delivered into the host memory.

c. Frame Decapsulation
The DM9102 checks the CRC bytes of all received frames before releasing the frame along with the CRC to the host processor.

3. Transmit Process and State Machine

a. Transmission Initiation
Once the host processor prepares a transmit descriptor for the transmit buffer, the host processor signals the DM9102 to take it. After the DM9102 has been notified of this transmit list, the DM9102 will start to move the data bytes from the host memory to the internal transmit FIFO. When transmit FIFO is adequately filled to the programmed threshold level, or when there is a full frame buffered into the transmit FIFO, the DM9102 begins to encapsulate the frame. The transmit encapsulation is performed by the transmit state machine, which delays the actual transmission onto the network until the network has been idle for a minimum interframe gap time.

b. Frame Encapsulation
The transmit data frame encapsulation stream consists of two parts: Basic frame beginning and basic frame end. The former contains 56 preamble bits and SFD, the later, FCS. The basic frame read from the host memory includes the destination address, the source address, the type/length field, and the data field. If the data field is less than 46 bytes, the DM9102 will pad the frame with the pattern 00 up to 46 bytes.

c. Collision
When concurrent transmissions from two or more nodes occur (termed; collision), the DM9102 halts the transmission of data bytes and begins a jam pattern consisting of AAAAAAAA. At the end of the jam transmission, it begins the backoff wait time. If the collision was detected during the preamble transmission, the jam pattern is transmitted after completing the preamble. The backoff process is called truncated binary exponential backoff. The delay is a random integer multiple of slot times. The number of slot times of delay before the N^{th} retransmission attempt is chosen as a uniformly distributed random integer in the range:

$$0 \le r < 2^k$$

$$k = \min (n, N) \text{ and } N=10$$

4. Physical Layer Overview:

The DM9102 provides 100M/10Mbps dual port operation. It provides a direct interface either to Unshielded Twisted pair Cable UTP5 for 100BASE-TX Fast Ethernet, or UTP5/UTP3 Cable for 10BASE-T Ethernet. In physical level operation, it consists of the following blocks:

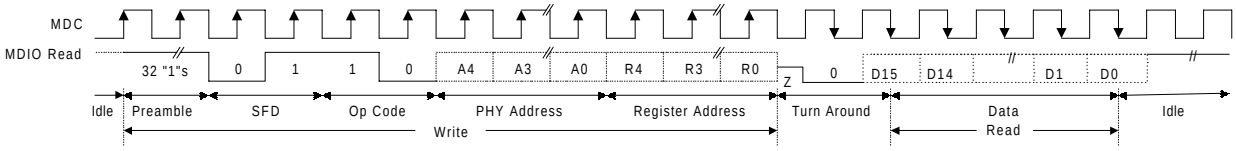
- PCS
- Clock generator
- NRE/NREI, MLT 3 encoder/decoder and driver
- MANCHESTER encoder/decoder
- 10BASE-T filter and driver

✧ Serial Management Interface

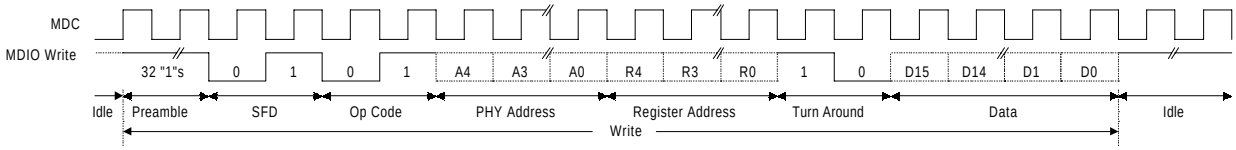
The serial management interface uses a simple, two-wired serial interface to obtain and control the status of PHY management register set through an MDC and MDIO. The Management Data Clock (MDC) is equipped with a maximum clock rate of 2.5MHz, while Management Data Input /Output (MDIO) works as a bi-directional, shared by up to 32 devices.

In read/write operation, the management data frame is 64-bit long start with 32 contiguous logic one bits (preamble) synchronization clock cycles on MDC. The Start of Frame Delimiter (SFD) is indicated by a <01> pattern followed by the operation code (OP):<10> indicates Read operation and <01> indicates Write operation. For read operation, a 2-bit turnaround (TA) filing between Resistor Address field and Data field is provided for MDIO to avoid contention. “Z” stands for high impedance state. Following turnaround time, a 16-bit data is read from or written onto management registers.

Management Interface - Read Frame Structure



Management Interface - Write Frame Structure



■ Configuration ROM Overview

The purpose of Configuration ROM (EEPROM) is to support the DM9102 information to the driver for the card. The CROM must support 64 words or more space for configuration data. The format of the CROM is as followed:

The format of EEPROM.

Field Name	Offset	Size
Subsystem ID block	0	18
CROM version	18	1
Controller count	19	1
Controller_0 Information	20	n
Controller_1 Information	20+n	m
: (depends on controller count)	:	:
CRC checksum	126	2

1. Subsystem ID Block

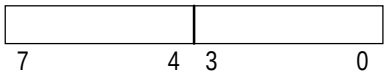
Every card must have a Subsystem ID to indicate the system vendor information. The content will be transferred into the PCI configuration space during a Hardware reset function.

(a) Vendor ID & Device ID can be set in EEPROM content & auto-loaded to PCI configuration register after reset. (default value = 1282, 9102) This function must be selectable for enable/disable by Auto_Load_Control (offset 08 of EEPROM) setting to avoid damaging default value due to

(b) incorrectly auto-load operation.
CRC check circuit of EEPROM contents to decide the auto-load operation of Vendor ID & Subsystem.

Subsystem ID Block		Byte Offset.
Subsystem Vendor ID		0
Subsystem ID		2
Reserved		4
Reserved		6
NCE	Auto_load_control	8
PCI Vender ID		10
PCI Device ID		12
Reserved	Reserved	14
Reserved	ID_block_CRC	17,16

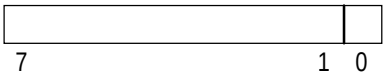
Byte Offset (08): Auto_Load_Control



Bit3~0: "1010" to enable auto-load of PCI Vendor_ID & Device_ID, "0" to disable.

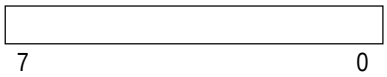
Bit7~4: "1X1X" to enable auto-load of NCE, to PCI configuration space.

Byte Offset (09): New_Capabilities_Enable



Bit0: Directly mapping to bit20 (New Capabilities) of the PCICS

Byte Offset (16): ID_BLOCK_CRC



This field is implemented to confirm the correct reading of the EEPROM contents.

2. CROM Version

Current version number is 03.

3. Controller Count

The configuration ROM supports multiple controllers in one board. Every controller has its unique controller information block. Controller count indicates the number of controllers put in the card.

4. Controller_X Information

Each controller has its information block to address its node ID, GPR control, supported connect media types (Media Information Block) and other application circuit information block.

Controller Information Header

ITEM	Offset	Size
Node Address	0	6
Controller_x Number	6	1
Controller_x Info. Block Offset	7	1

5. Controller Information Body Pointed By Controller_X Info Block Offset Item In Controller Information Header:

Item	Offset	Size
Connection Type Selected	0	2
GPR Control	2	1
Block Count	3	1
Block_1	4	n
:	4+n	m

* Connect Type Selected indicates the default connect media type selected.
* GPR Control defines the input or output direction of GPR.

There are three types of block:

1. **PHY Information Block (type=01)**
2. **Media Information Block (type=00)**
3. **Delay Period Block (type=80)**

PHY information Block (type=01)

Item	Offset	Size
Block Length	0	1
Block Type(01)	1	1
PHY Number	2	1
GPR Initial Length(G_i)	3	1
GPR Initial Data	4	G_i
Reset Sequence Length(R_i)	4+G_i	1
Reset Data	5+G_i	R_i
Media Capabilities	5+G_i+R_i	2
Nway Advertisement	7+G_i+R_i	2
FDX Bit Map	9+G_i+R_i	2
TTM Bit Map	11+G_i+R_i	2

Note 1: The definition of Media Capabilities and Nway Advertisement is the same with 802.3U in terms of Auto-negotiation.

Media Information Block (Type = 00)

ITEM	Offset	Size
Block Length	0	1
Block Type(00)	1	1
Media Code	2	1
GPR Data	3	1
Command	4	2

Note 1: Media Code: 10BASE_T Half Duplex 00
10 BASE_T Full Duplex 04
100 BASE_T Half Duplex 01
100 BASE_T Full Duplex 05

Note 2: Command Format

Delay Period Block (Type = 80) Define the delay time unit in us.

ITEM	Offset	Size
Block Length	0	1
Block Type(80)	1	1
Time Unit	2	2

■ Absolute Maximum Ratings*

Supply Voltage (VCC) ..... -0.5V to 5.5V
Maximum DC Input Voltage (VIN) -0.5V to VCC+0.5V
DC Output Voltage (VOUT) .....-0.5V to VCC +0.5V
Storage Temperature Rang (Tstg) ..-65℃ to +150℃
Case Temperature Range……..…0℃ to 85℃
Infrared Solder Reflow Peak Temp. (10 to 20 sec.)
..... 220℃to 225℃
ESD Rating (Rzap=1.5K, Czap=100Pf) 4000V

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

✧ DC Electrical Characteristics

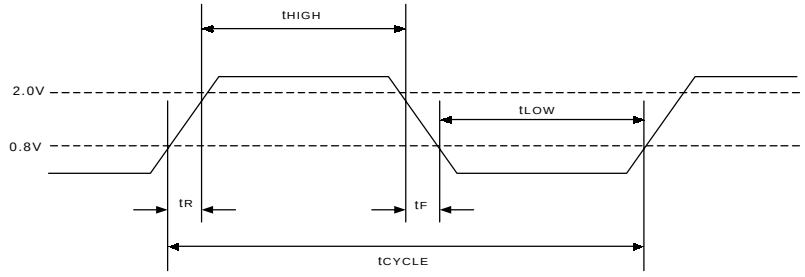
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
VCC	Supply Voltage	4.75	-	5.25	V	-
TOP	Operation Temperature	-20	-	70	C	-
VIL	Input Low Voltage	-	-	0.8	V	-
VIH	Input High Voltage	2.0	-	-	V	-
VOL	Output Low Voltage (Iol = 8mA)	-	-	0.5	V	-
VOH	Output High Voltage (Ioh = -2mA)	2.4	-	-	V	-
IIL	Input Leakage Current	-	-	10	uA	-
IDD	Operation Supply Current	-	230	250	mA	-
IPD	Power down Supply Current	-	T/D	-	uA	-

Receiver						
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**	
VICM	RXI+/RXI- Input Common-Mode Voltage	1.5	2.0	2.5	V	100 Ω termination Across
Transmitter						
ITD100	100TXO+/- 100BASE-TX Mode Differential Output Current	19		21	mA	Absolute Value
ITD10	10TX+/- 10BASE-T Differential Output Current	44	50	56	mA	Absolute Value

* -: No defined value
*T/D: To be determined

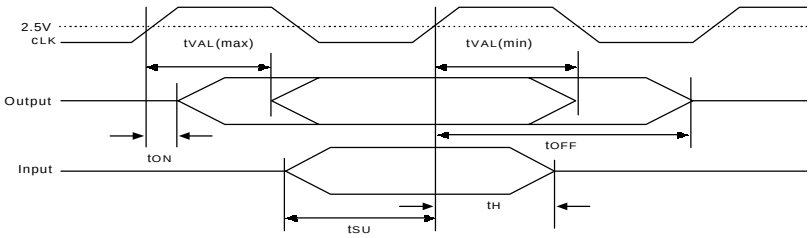
✧ AC Electrical Characteristics

- **PCI Clock Specifications Timing**



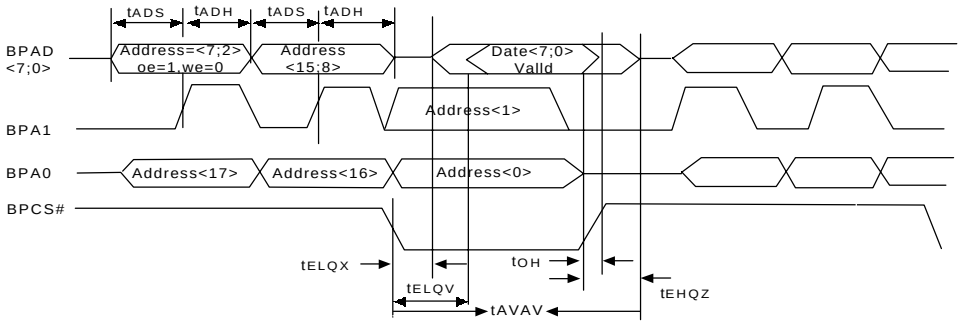
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tR	PCI_CLK rising time	4	-	-	ns	-
tF	PCI_CLK falling time	4	-	-	ns	-
tCYCLE	Cycle time	30	-	-	ns	-
tHIGH	PCI_CLK High Time	12	-	-	ns	-
tLOW	PCI_CLK Low Time	12	-	-	ns	-

- **Other PCI Signals Timing Diagram**



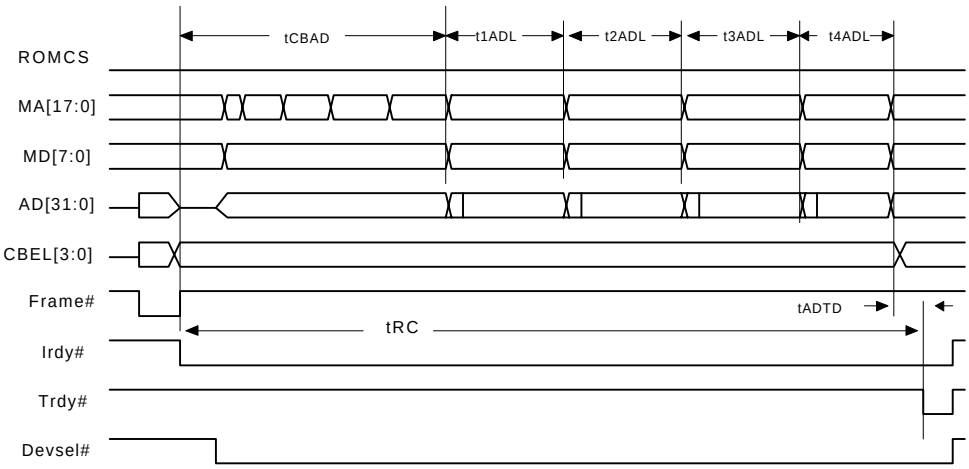
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tVAL	Clk-To-Signal Valid Dealy	2	-	11	ns	Cload = 50 pF
tON	Float-To-Active Delay From Clk	2	-	-	ns	-
tOFF	Active-To-Float Dealy From Clk	-	-	28	ns	-
tSU	Input Signal Valid Setup Time Before Clk	7	-	-	ns	-
tH	Input Signal Hold Time From Clk	0	-	-	ns	-

- **Multiplex Mode Boot ROM Timing**



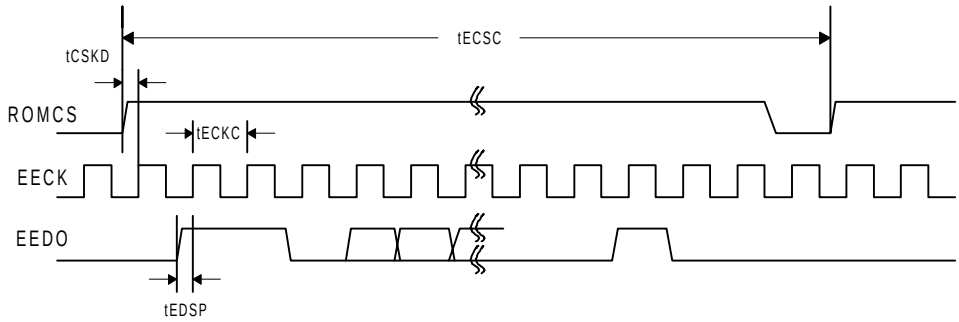
Symbol	Parameter	Min.	Type	Max.	Unit	Conditions
TAVAV	Read Cycle Time	-	31	-	PCI clock	-
tELQV	BPCS# To Output Delay	0	-	7	PCI clock	-
tEHQZ	BPCS# Rising Edge To Output High Impedance	-	1	-	PCI clock	-
tOH	Output Hold From BPCS#	0	-	-	PCI clock	-
tADS	Address Setup To Latch Enable High	4	-	-	PCI clock	-
tADH	Address Hold From Latch Enable High	4	-	-	PCI clock	-

- **Direct Mode Boot ROM Timing**



Symbol	Parameter	Min.	Type	Max.	Unit	Conditions
tRC	Read Cycle Time	-	50	-	PCI clock	-
tCBAD	Bus Command to first address delay	-	18	-	PCI clock	-
t1ADL	first address length	-	8	-	PCI clock	-
t2ADL	second address delay	-	8	-	PCI clock	-
t3ADL	third address delay	-	8	-	PCI clock	-
t4ADL	fourth address delay	-	7	-	PCI clock	-
tADTD	end of address to Tardy active	-	1	-	PCI clock	-

- **EEPROM Timing**

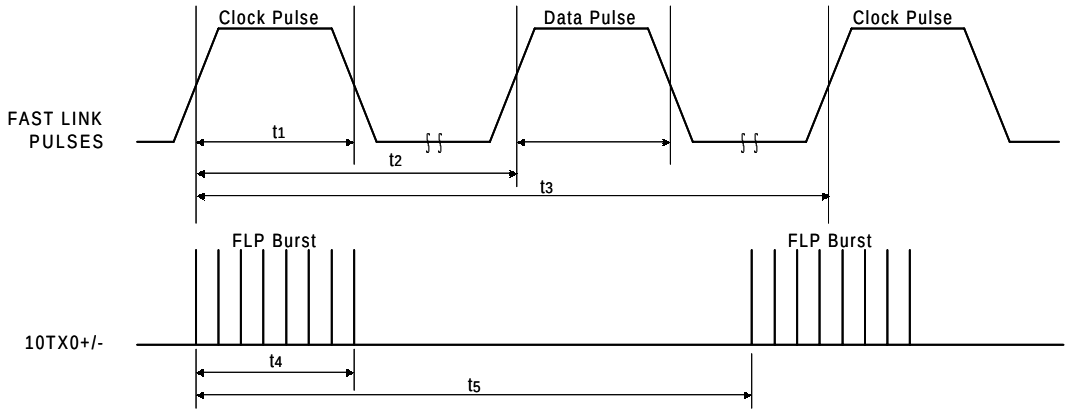


Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tECKC	Serial ROM clock EECK period	64	-	-	PCI clock	-
tECSC	Read Cycle Time	1792	-	-	PCI clock	-
tCSKD	Delay from ROMCS High to EECK High	28	-	-	PCI clock	-
tEDSP	Setup Time of EEDO to EECK	24	-	-	PCI clock	-

- **PHYceiver :**

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Transmitter						
tTR/F	100TXO+/- Differential Rise/Fall Time	3.0		5.0	ns	
tTM	100TXO+/- Differential Rise/Fall Time Mismatch	-0.5		0.5	ns	
tTDC	100TXO+/- Differential Output Duty Cycle Distortion	-0.5		0.5	ns	
tT/T	100TXO+/- Differential Output Peak-to-Peak Jitter		800		ps	
XOST	100TXO+/- Differential Voltage Overshoot			5	%	

- **Auto-negotiation and Fast Link Pulse Timing Diagram**

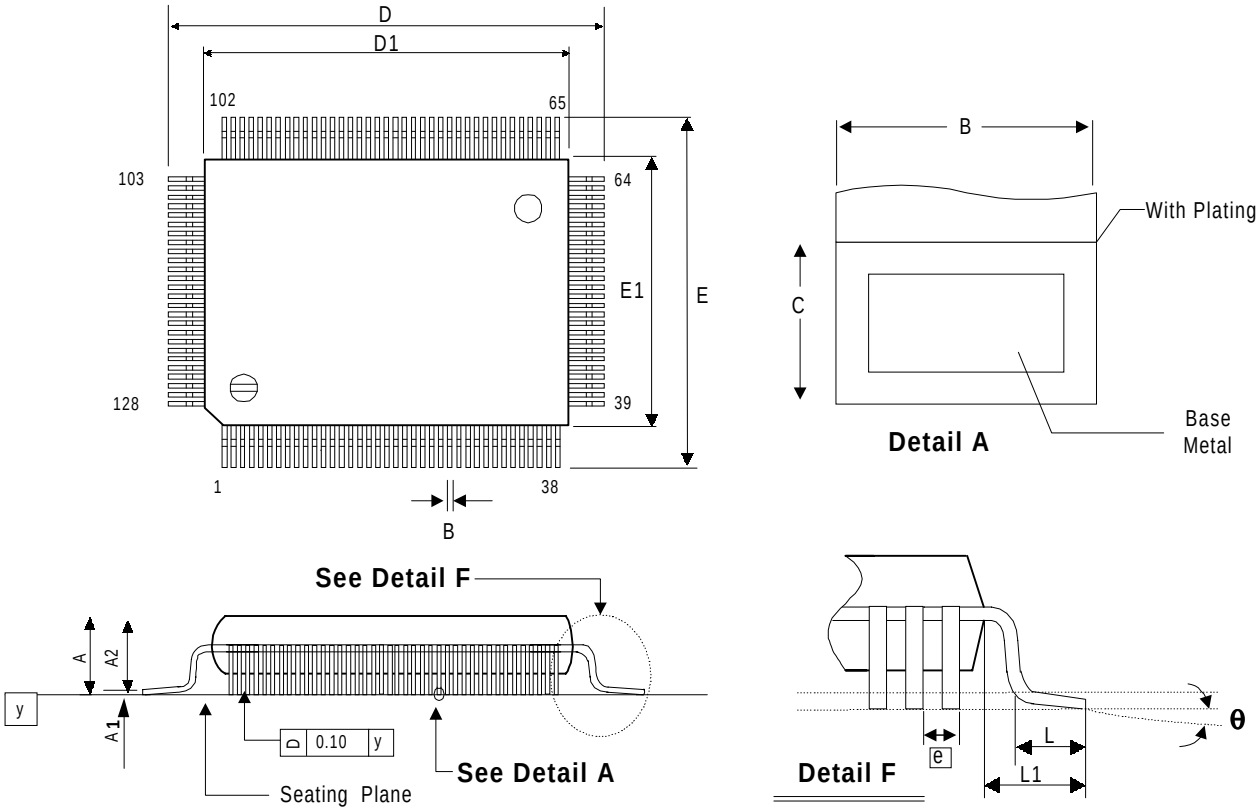


Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_1	Clock/Data Pulse Width	-	100	-	ns	
t_2	Clock Pulse To Data Pulse Period	-	62.5	-	us	DATA = 1
t_3	Clock Pulse To Clock Pulse Period	-	125	-	us	
t_4	FLP Burst Width	-	2	-	ms	
t_5	FLP Burst To FLP Burst Period	-	13.93	-	ms	
-	Clock/Data Pulses Per Burst	33	33	33	ea	

Package Information

QFP 128L Outline Dimensions

Unit: Inches/mm



Symbol	Dimension In Inch	Dimension In mm
A	0.134 Max.	3.40 Max.
A1	0.010 Min.	0.25 Min.
A2	0.112± 0.005	2.85± 0.12
B	0.009± 0.002	0.22±0.05
C	0.006± 0.002	0.145± 0.055
D	0.913± 0.007	23.20± 0.20
D1	0.787± 0.004	20.00 ± 0.10
E	0.677± 0.008	17.20± 0.20
E1	0.551± 0.004	14.00± 0.10
e	0.020 BSC	0.5 BSC
L	0.035± 0.006	0.88± 0.15
L1	0.063 BSC	1.60 BSC
y	0.004 Max.	0.10 Max.
θ	0°~12°	0°~12°

Note:

1. Dimension D1 and E1 do not include resin fins.
2. All dimensions are based on metric system.
3. General appearance spec. should base itself on final visual inspection spec.

Ordering Information

Part Number	Pin Count	Package
DM9102F	128	QFP

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WARNING
Conditions beyond those listed for the absolute maximum may destroy or damage the products. In addition, conditions for sustained periods at near the limits of the operating ranges will stress and may temporarily (and permanently) affect and damage structure, performance and/or function.

Appendix A

DM9102 SROM Format

Total Size: 128 Bytes

Field Name	Offset (Bytes)	Size (Bytes)	Value (Hex)	Commentary
Sub-Vendor ID	0	2	0291	**ID Block**
Sub-Device ID	2	2	8212	
Reserved1	4	4	00000000	
Auto_Load_Control	8	1	00	Auto-load function definition: **Bit 3..0 = 1010** → Auto-Load PCI Vendor ID/Device ID enabled **Bit 7..4 = 1010** → Auto-Load PMC/PMCSR enabled (P.S.: For DM9102 E7 and later **Bit 7..4 = 1x1x** → Auto-Load PMC/PMCSR enabled)
New_Capabilities_Enable (NCE)	9	1	00	Please refer to DM9102 Spec.
PCI Vendor ID	10	2	1282	If Auto-Load PCI Vendor ID/Device ID function disabled, the PCI Vendor ID/Device ID will use the default values (**1282h**, **9102h**).
PCI Device ID	12	2	9102	
Reserved	14	1	00	Please refer to DM9102 Spec.
Reserved	15	1	00	Please refer to DM9102 Spec.
ID_BLOCK_CRC	16	1	-	Offset 0..15, 17 ID CRC
Reserved2	17	1	00	
SROM Format Version	18	1	03	Version 3.0
Controller Count	19	1	01	
IEEE Network Address	20	6	-	**Controller Info Header**
Controller_0 Dev Number	26	1	00	
Controller_0 Info Leaf Offset	27	2	001E	Offset 30
Reserved3	29	1	00	
Selected Connected Type	30	2	0800	**Controller_0 Info Leaf Block**
General Purpose Control	32	1	80	MAC CR12 Register
Block Count	33	1	06	6 Blocks
F(1)+Length	34	1	8E	**Block 1 (PHY Info Block)**
Type	35	1	01	PHY Information Block
PHY Number	36	1	01	PHY Address
GPR Length	37	1	00	
Reset Sequence Length	38	1	02	
Reset Sequence	39	2	0080	
Media Capabilities	41	2	7800	
Nway Advertisement	43	2	01E0	
FDX Bit Map	45	2	5000	
TTM Bit Map	47	2	1800	

Field Name	Offset (Bytes)	Size (Bytes)	Value (Hex)	Commentary
F(1)+Length	49	1	85	**Block 2 (Delay Period Block)**
Type	50	1	80	Delay Period Block
Delay Sequence	51	4	40002000	MicroSecond
F(1)+Length	55	1	85	**Block 3 (Media Info Block)**
Type	56	1	00	Media Information Block
Media Code	57	1	00	10Base-T Half_Duplex
GPR Data	58	1	00	
Command	59	2	0087	
F(1)+Length	61	1	85	**Block 4 (Media Info Block)**
Type	62	1	00	Media Information Block
Media Code	63	1	01	100Base-TX Half_Duplex
GPR Data	64	1	00	
Command	65	2	0087	
F(1)+Length	67	1	85	**Block 5 (Media Info Block)**
Type	68	1	00	Media Information Block
Media Code	69	1	04	10Base-T Full_Duplex
GPR Data	70	1	00	
Command	71	2	0087	
F(1)+Length	73	1	85	**Block 6 (Media Info Block)**
Type	74	1	00	Media Information Block
Media Code	75	1	05	100Base-TX Full_Duplex
GPR Data	76	1	00	
Command	77	2	0087	
SROM_CRC	126	2	-	Offset 0..125 SROM CRC