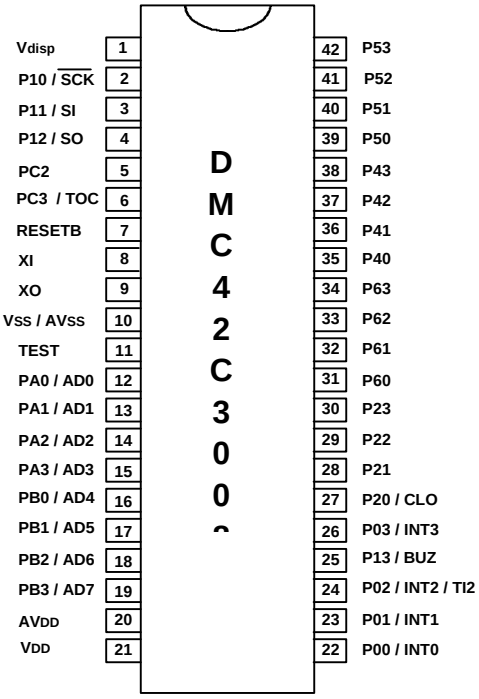
4Bit Single Chip Microcontroller **DMC42C3008**

DESCRIPTION

The DMC42C3008 is a 4-bit single chip microcomputer having 8K bytes ROM and is designed with CMOS silicon gate technology. The DMC42C3008 includes such peripherals as various timers, A/D converter, serial communication interface,on-chip oscillator and clock circuitry. It also comes with high-voltage I/O pins that can directly drive a fluorescent display.

The high performance CPU and internal peripherals allow flexible & cost effective system design in industrial and home appliances. AND the OTP device (42P3008) can shorten system development periods and help the process for software debugging.

PIN CONFIGURATION



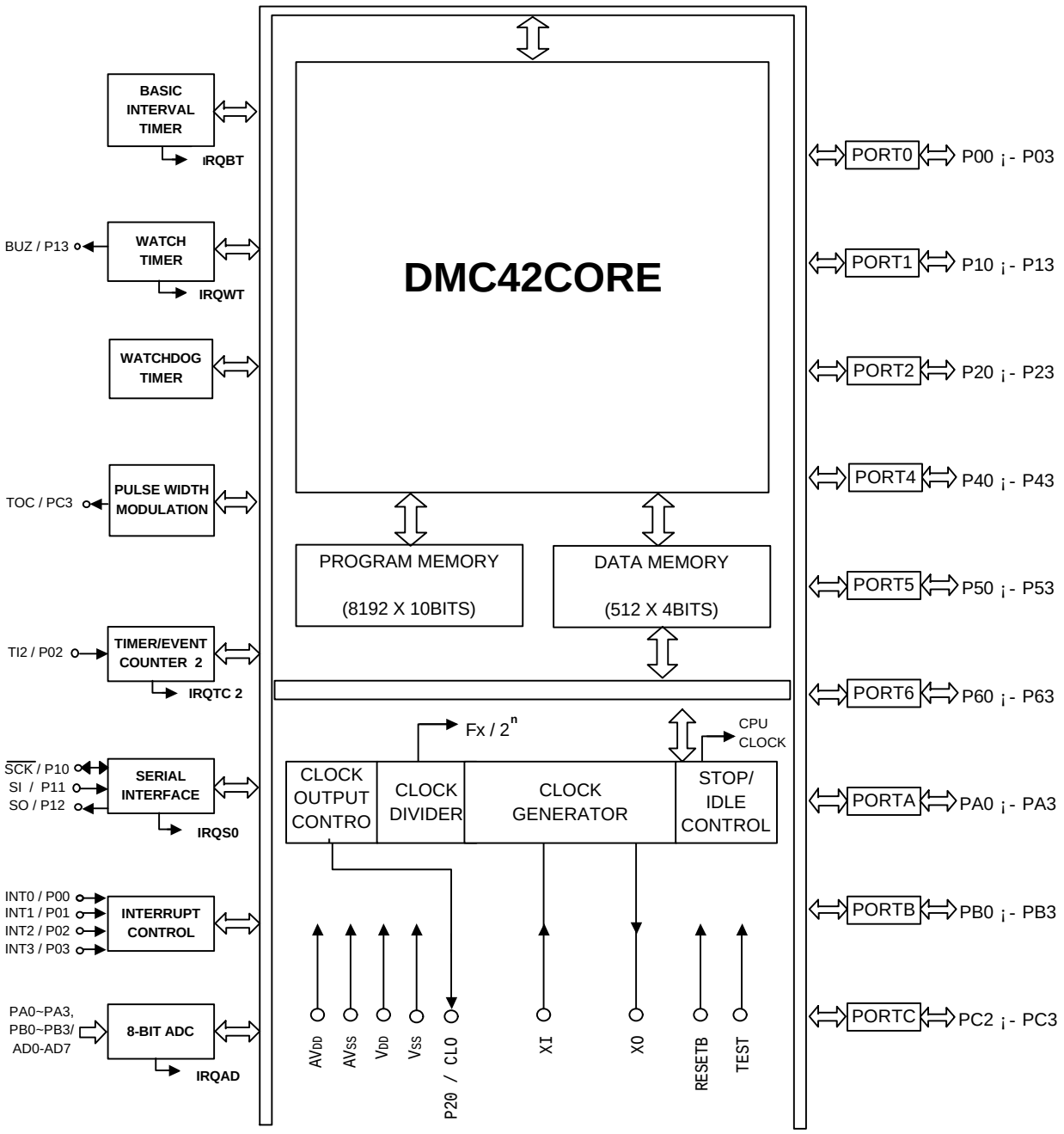
FEATURES

- Memory mapped I/O
- Program memory : 8192 x 10bits
- Data memory : 512 x 4bits
- Instructions
  - Various bit manipulation
  - 8-bit data operation
  - 7-bit relative branch
  - 1 byte absolute call
- Instruction cycle times
  - Main (XI = 4.19MHz)
    . 15.3 us (XI/64 = 65.5KHz)
    . 1.91 us (XI/8 = 524.0KHz)
    . 0.95 us (XI/4 = 1.05MHz)
- 4 Register Bank
- General register : 8 x 4-bit respectively
- Accumulator
  - Bit Accumulator (CY), 4 bit Accumulator (A), 8 bit Accumulator (XA)
- Multiple vectored interrupt source
  - External interrupt : 4
  - Internal interrupt : 6
- Watch timer(at 4.19MHz)
  - fast mode : 3.91 msec
  - normal mode : 0.5 sec
  - buzzer output : 1, 2, 4 KHz
- Basic interval timer
  - 8 kinds of period
  - Used stabilization wait timer to wake up Stop mode
- One 8-bit timer / event counter
- Watchdog timer
  - 4 kinds of period
- PWM
  - 14 bit PWM output X 1ch
- 8-bit serial communication interface
  - External / Internal clock selection
  - Mode : Transmit, Receive
    Receive only
    Clock continuous
- 8-bit A/D converter
  - 8-bit successive approximate type
  - 8 channels
  - Sample and hold
  - Conversion time : 17.1us at 4.19MHz
- 34 I/O Pins
  - CMOS Pins : 13
  - High voltage Pins : 21
  - Internal pull-up resistor (Mask option)
  - Internal pull-down resistor (Mask option)
- Power saving mode
  - STOP : Main clock, CPU clock stop
  - STBY : Only CPU clock stop
    Main clock operation
- Operating voltage range
  - VDD = 5V ± 10%
  - V_{disp} = VDD - 40V
- Package : 42 SDIP

APPLICATION

Microwave Oven, Home Appliances

BLOCK DIAGRAM



PROGRAM MEMORY (ROM)

	CONTENTS
0000H	VECTOR ADDRESS AREA
001FH	
0020H	ZERO-PAGE CALL AREA
002FH	
0060H	**8K Byte**
1FFFH	

VECTOR ADDRESS

	Prioty	INTERRUPT SUORCE	
0000H	0	RESET	Reset Signal
0002H	1	IRQBT	Basic Interval Timer
0004H	2	IRQ0	External interrupt 0
0006H	3	IRQ1	External interrupt 1
0008H			
000AH			
000CH	6	IRQ2	External interrupt 2
000EH	7	IRQTC2	Timer Event Counter 2
0010H	8	IRQ3	External interrupt 3
0012H	9	IRQS0	Serial I/O 0
0014H	10	IRQAD	8 bit ADC
0016H			
0018H	12	IRQWT	Watch Timer
001AH	13	IRQKS	Key Scan
001CH			
001EH	15	-	reserved

DATA MEMORY (RAM)

		DIRECT	INDIRECT			STACK	GENERAL REGISTER	
		m	@HL		@DE @DL			
	$00 PAGE0 (256 Byte) $FF			**MP=0**		**SPS=0**	**RB=0 RB=2**	**RB=1 RB=4**
	$00 PAGE1 (256 Byte) $FF	**MB=0**	**MB=0**	**MP=1**		**SPS=1**		
BANK 0 (1K)	$00 PAGE2 (256 Byte) $FF			**MP=2**		**SPS=2**		
	$00 PAGE3 (256 Byte) $FF	**I/O MEMORY**		**MP=3**				

; Usable

I/O ADDRESS MAP

ADDRESS	Hardware Module Name				R/W	Addressing Unit			REMARKS	INITIAL
	b3	b2	b1	b0		1 bit	4 bit	8bit		VALUE
318H	Stack pointer low (SPL)				R/W			O	Stack pointer low	E
319H	Stack pointer high (SPH)				R/W			O	stack pointer high	F
31AH	SP3	SP2	SP1	SP0	R/W			O	Stack Page Select Low (SPSL)	0
31BH	-	-	SP5	SP4	R/W			O	Stack Page Select High (SPSh)	0
31CH	AC		IS1	IS0	R/W	O	O	O	Psw low (PSWL)	0
31DH	CY	Z	OV	T					Psw high (PSWH)	0
32CH	T/E counter mode register 2				W	32CH.3			clock source select. counter	00
32DH	(TMOD2)								start (ch2)	
32EH	T/E counter register 2				R				readable count value (ch2)	00
32FH	(TMCNT2)									
330H	T/E reference register 2				W				count reference register (ch2)	FF
331H	(TMREF2)									
332H	Basic Timer mode register(BMOD)				R/W	332H.3			clock select, Bit start	0
334H	Basic interval timer count				R				readable count register	00
335H	register(BITCNT)									
336H	Watch timer mode register				R/W	336H.3			clock/buzzer select. bit3	00
337H	(WMOD)								readable	
338H	Watch dog timer mode register				W				clock source sel. timer EN/DIS	00
	(WDTM)									
339H				WDTF	R				WDT flag	0
340H	Pwm mode register0(PWMOD0)				R/W				6.14bit pwm counter EN/DIS	0
342H	Pwm0 data register high				W			O	14bit pwm data register high	00
343H	(PWMODH)									
344H	Pwm0 data register low				W			O	14bit pwm data register low	00
345H	(PWMODL)									
354H	PWM3	PWM2	PWM1	PWM0	W			O	pwm output enable mode	00
355H		PWM6	PWM5	PWM4					register (PWM0 = 14bit)	
386H	Adc8 mode register (ADCM8)				R/W	386H.3		O	analog input pin select. start &	00
387H									low 4bit readable	
388H	Adc8 output latch (ADCOL8)				R			O	8bit conversion data	00
389H										
3A0H	Power control register				R/W		O		system clock select, idle, stop	00
	(PCON)								mode	
3A2H	Operating mode register (SCMOD)				R/W	O			main/sub system clock select	0
3A4H	Clock output mode register				W		O		cpu clock output select, clock	00
	(CLOMD)								out EN/DIS	
3A8H	Serial interface mode register0				W	3A8H.3		O	receive/transmit mode. clock	00
3A9H	(SIOM0)								select	
3AAH	Serial interface buffer0				R/W				serial shift register 0	XX
3ABH	(SBUFF0)									
3B2H	Power on flag (PONF)				P/W	3B2H.0		O	power on reset flag	0
3C2H	IME				R/W	3C2H.3		O	Interrupt priorty select, IME flag.	00
3C3H	IPSR3	IPSR2	IPSR1	IPSR0						

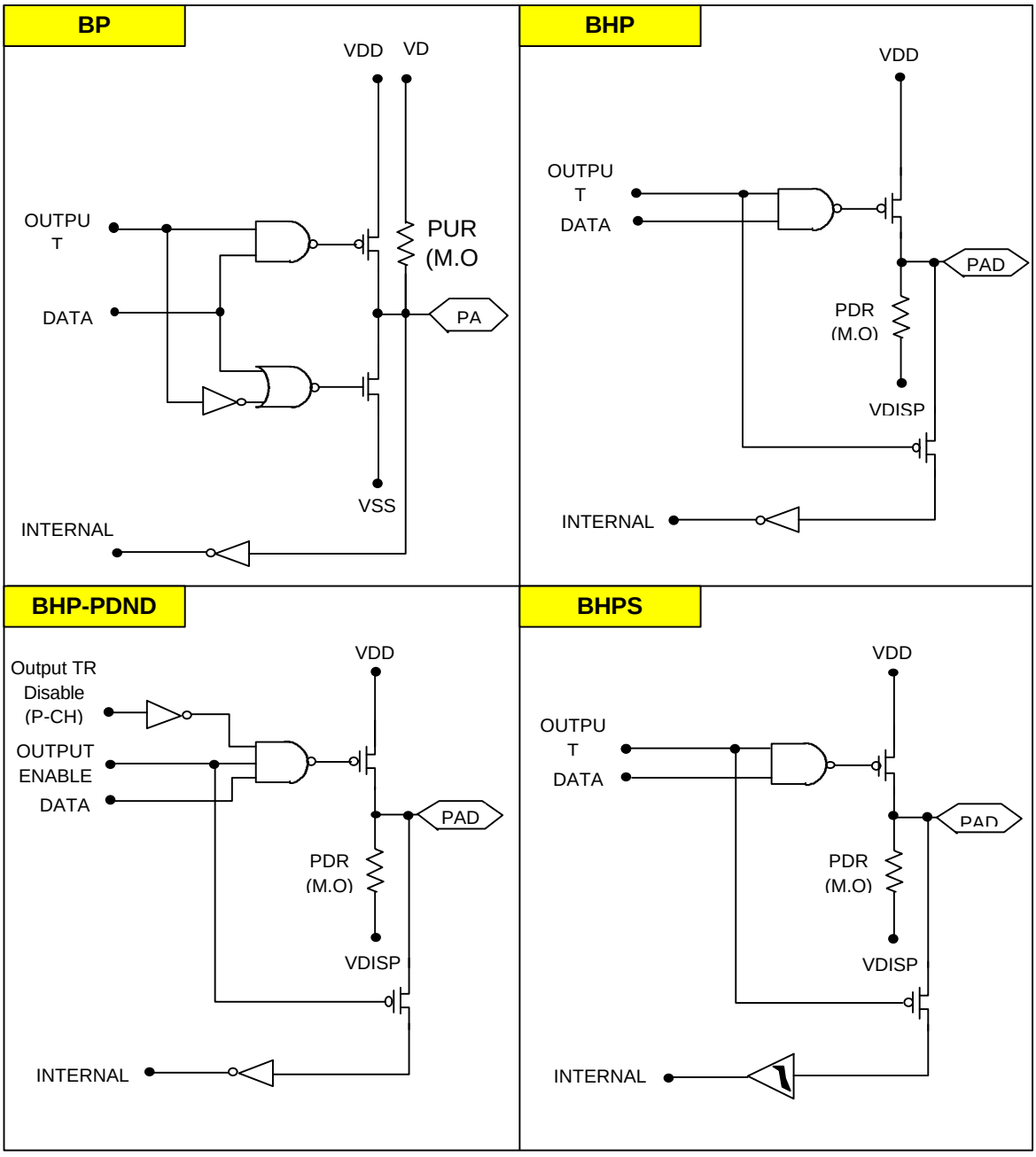
ADDRESS	Hardware Module Name				R/W	Addressing Unit			REMARKS	INITIAL VALUE
	b3	b2	b1	b0		1 bit	4 bit	8bit		
3C4H	External interrupt mode register0 (IMOD0)				W		O		external interrupt 0 edge detection	00
3C5H	External interrupt mode register1 (IMOD1)				W		O		external interrupt 1 edge detection	00
3C6H	External interrupt mode register2 (IMOD2)				W		O		external interrupt 2 edge detection	00
3C7H	External interrupt mode register3 (IMOD3)				W		O		external interrupt 3 edge detection	00
3D8H	IE2	IRQ2	IEBT	IRQBT	R/W	O	O		Interrupt EN/IRQ flag	0
3D9H	IEAD8	IRQAD8	IEWT	IRQWT	R/W	O	O		Interrupt EN/IRQ flag	0
3DAH			IES0	IRQS0	R/W	O	O		Interrupt EN/IRQ flag	0
3DBH					R/W	O	O		Interrupt EN/IRQ flag	0
3DCH	IE1	IRQ1	IE0	IRQ0	R/W	O	O		Interrupt EN/IRQ flag	0
3DDH	IETC2	IRQTC2			R/W	O	O		Interrupt EN/IRQ flag	0
3DEH			IE3	IRQ3	R/W	O	O		Interrupt EN/IRQ flag	0
3E0H	PW03	PW02	PW01	PW00	W			O	port 0, 1 mode register (PMGA)	00
3E1H	PW13	PW12	PW11	PW10						
3E2H	PW23	PW22	PW21	PW20	W			O	port 2, 3 mode register (PMGB)	00
3E3H	PW33	PW32	PW31	PW30						
3E4H	PW43	PW42	PW41	PW40	W			O	port 4, 5 mode register (PMGC)	00
3E5H	PW53	PW52	PW51	PW50						
3E6H	PW63	PW62	PW61	PW60	W			O	port 6, 7 mode register (PMGD)	00
3E7H	PW73	PW72	PW71	PW70						
3EAH	PWA3	PWA2	PWA1	PWA0	W			O	port a, b mode register (PMGF)	00
3EBH	PWB3	PWB2	PWB1	PWB0						
3ECH	PWC3	PWC2	PWC1	PWC0	W			O	port c, d mode register (PMGG)	00
3EDH	PWD3	PWD2	PWD1	PWD0						
3F0H	PORT0 (R0)				R/W	O	O		R0 Port Data Register	0
3F1H	PORT1 (R1)				R/W	O	O		R1 Port Data Register	0
3F2H	PORT2 (R2)				R/W	O	O		R2 Port Data Register	0
3F4H	PORT4 (R4)				R/W	O	O	O	R4 Port Data Register	0
3F5H	PORT5 (R5)				R/W	O	O		R5 Port Data Register	0
3F6H	PORT6 (R6)				R/W	O	O		R6 Port Data Register	0
3FAH	PORTA (RA)				R/W	O	O		RA Port Data Register	0
3FBH	PORTB (RB)				R/W	O	O		RB Port Data Register	0
3FCH	PORTC (RC)				R/W	O	O	O	RC Port Data Register	0

PIN DESCRIPTION

PIN SYMBOL	SHARED PIN	I/O	FUNCTION	RESET	PORT TYPE
P00 P01 P02 P03	INT0 INT1 INT2/TI2 INT3	I/O	4-BIT I/O HIGH VOLTAGE PORT PORT 0		BHPS
P10	SCK	I/O	4-BIT I/O PORT PORT 1 (P13 HIGH VOLTAGE PIN)		BP
P11	SI				
P12	SO				
P13	BUZ				BHP
P20	CLO	I/O	4-BIT I/O HIGH VOLTAGE PORT PORT 2		BHP
P21~ P23	-				
P4	-		4-BIT I/O HIGH VOLTAGE PORT. PORT4		BHP
P5	-		4-BIT I/O HIGH VOLTAGE PORT. PORT5		BHP
P6	-		4-BIT I/O HIGH VOLTAGE PORT. PORT6		BHP-PDND
PA	AD0~AD3		4-BIT I/O PORT. PORTA		BP
PB	AD4~AD7		4-BIT I/O PORT. PORTB		BP
PC2	-		2-BIT I/O PORT. PORTC		BP
PC3	TOC				
INT0	P00	I	External interrupt input port rising/falling edge detection Event pulse input port for the timer/event counters	INPUT	BHPS
INT1	P01				
INT2/TI2	P02				
INT3	P03				
SCK	P10	I/O	Serial clock in/out port		BP
SI	P11	I	Serial data input port		
SO	P12	O	Serial data output port		
BUZ	P13	O	Buzzer output port		BHP
CLO	P20	O	Clock output port		BHP
TOC	PC3	O	PWM output port		BP
Key scan	P4-P5	I	4, 6, 8 bits Key scan input selectable		BHP
AD0~AD3	PA	I	Analog input for the 8-bit A/D converter		BP
AD4~AD7	PB				
XI	-	I	XI, XO are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator.		BIN
X		O			BOU
RESETB	-	I	Reset input pin		BIN
TEST	-	I	Normally connect to VSS		BIN
V_{disp}	-		Used as a high-voltage output power supply pin.		
AVDD, AVSS	-		Power & ground for the A/D converter		
VDD, VSS	-		Power & ground		

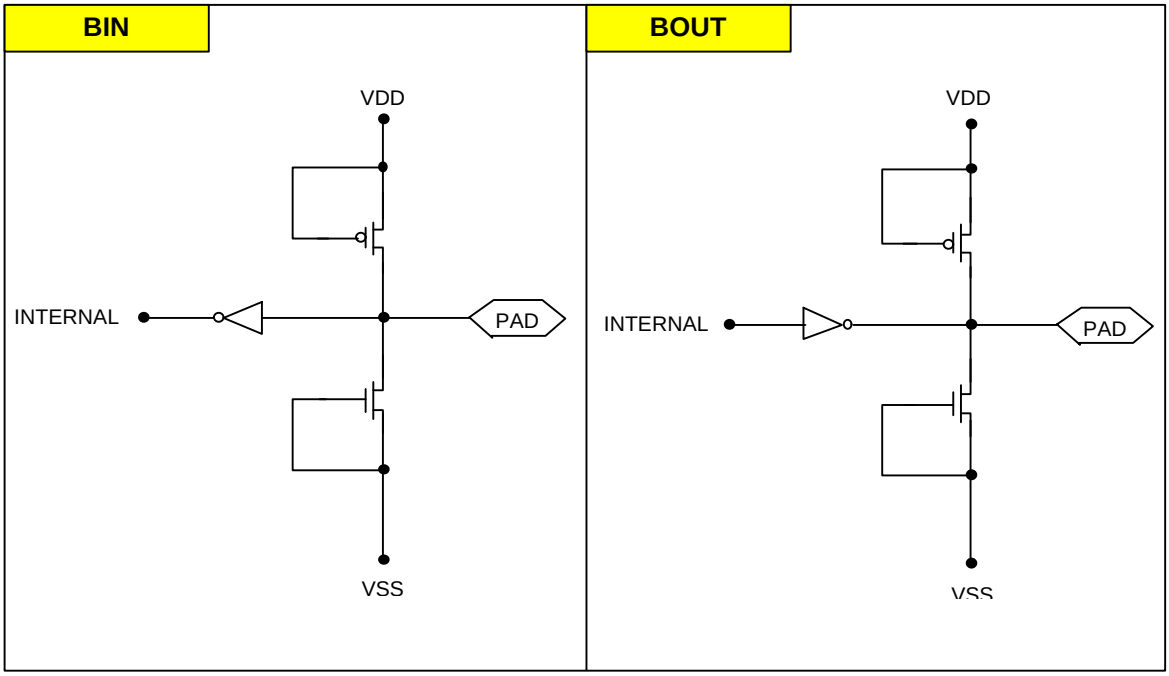
* Note) P4, P5 : 8-bit operation possible

I/O CIRCUITS



NOTE) PDR : Pull-Down Resistor
PUR : Pull-Up Resistor
M.O : Mask Option

I/O CIRCUITS



ABSOLUTE MAXIMUM RATINGS

(T_A = 0¡É to 70¡É, V_{DD} = 5V ±10%, f_X = 4.19MHz)

PARAMETER	SYMBOL	CONDITION		RATING	UNIT
Supply Voltage		V_{DD}		-0.3 to + 6.0	V
Programming Voltage		V_{PP}	Note 1	-0.3 to 13.0	V
Pin Voltage		V_T	Note 2	-0.3 to V_{DD}+0.3	V
			Note 3	V_{DD}-45 to V_{DD}+0.3	
Total Permissible Input Current		¢²I_O	Note 4	70	mA
Total Permissible Output Current		-¢²I_O	Note 5	150	mA
Maximum Input Current		I_O	Note 6, 7	4	mA
			Note 6, 8	20	
Maximum Output Current		-I_O	Note 9, 10	4	mA
			Note 10, 11	30	
Operating Temperature		T_A		-40 to +85	¡É
Storage Temperature		T_{stg}		-55 to +125	¡É
V_{disp} Voltage		V_{disp}	Note 12	V_{DD} - 40	V

Notes : Permanent damage may occur if these absolute maximum rating are exceeded. Normal operation must be under the conditions stated in the electrical characteristics tables. If these conditions are exceeded, the LSI may malfunction or its reliability may be affected.

1. Applies to pin AV_{DD} (V_{PP}) of DMC42P3008.
2. Applies to all standard voltage pins.
3. Applies to all high voltage pins.
4. The total permissible input current is the total input currents simultaneously flowing in from all I/O pins to V_{SS}.
5. The total permissible output current is the total output currents simultaneously flowing out from V_{DD} to all I/O pins.
6. The maximum input current is the maximum current flowing from each I/O pin to V_{SS}.
7. Applies to ports PA, PB.
8. Applies to ports P1, PC.2, PC.3.
9. Applies to ports P1, PA, PB, PC.2, PC.3.
10. The maximum output current is the maximum current flowing from V_{DD} to each I/O pin.
11. Applies to ports P0, P1.3, P2, P4, P5 and P6.
12. The maximum applied voltage is V_{DD} - 40V.

DC ELECTRICAL CHARACTERISTICS

(VSS = 0, VDD = 5V ±10%, TA = 25¡É, fX = 4.19MHz)

PARAMETER	SYMBOL	TEST CONDITION		LIMIT			UNIT	NOT
				MIN.	TYP.	MAX.		
Supply Voltage	VDD	VDD		4.5	-	5.5	V	
High Level Input Voltage	VIH	RESETB $\overline{SCK}$, SI INT0~3 TI2		0.8VDD	-	VDD+0.	V	
		XI		VDD-	-	-	V	
Low Level Input Voltage	VIL	RESETB $\overline{SCK}$, SI		-0.3	-	0.2VDD	V	
		INT0~3 TI2		VDD-40	-	0.2VDD	V	
		XI		-0.3	-	0.5	V	
High Level Output Voltage	VOH	$\overline{SCK}$, SO TOC	-IOH = 0.5mA	VDD-	-	-	V	
Low Level Output Voltage	VOL	$\overline{SCK}$, SO TOC	IOL = 0.4mA	-	-	0.4	V	
I/O Leakage Current	| IIL |	RESETB,TOC $\overline{SCK}$, SI, SO XI	VIN = 0 V to VDD	-	-	3	uA	1
		INT0~3 TI2	VIN = VDD - 40V to VDD	-	-	15	uA	
Supply Current	IDD		VDD = 5V fX = 4MHz	-	-	10	mA	2, 5
	ISBY		VDD = 5V fX = 4MHz	-	-	5	mA	3, 5
	ISTOP		VDD = 5V	-	-	2	uA	4

Notes : 1. Excludes current flowing through pull-up MOS output buffers.

2. I_{DD} is the source current when no I/O current is flowing while the MCU is in reset state.
   Test condition : MCU : Reset
   Pins : RESETB, TEST at V_{SS}
   P1.0~1.2, PA, PB, PC.2~3 at V_{DD}
   P0, P1.3, P2, P4, P5, P6 at V_{disp}

3. I_{SBY} is the source current when no I/O current is flowing while the MCU timer is operating.
   Test condition : MCU : I/O Reset
   Standby mode
   Pins : RESETB at V_{DD}
   TEST at V_{SS}
   P1.0~1.2, PA, PB, PC.2~3 at V_{DD}
   P0, P1.3, P2, P4, P5, P6 at V_{disp}

4. This is the source current when no I/O current is flowing.
   Test condition : Pins : P1.0~1.2, PA, PB, PC.2~3 at V_{DD}
   P0, P1.3, P2, P4, P5, P6 at V_{SS}
   XI clock stop after stop mode

5. Current dissipation is in proportion to f_X while the MCU is operating or in standby mode.

DC ELECTRICAL CHARACTERISTICS

1. STANDARD I/O PINS

(V_{SS} = 0, V_{DD} = 5V ±10%, T_A = 25¡É, f_X = 4.19MHz)

PARAMETER	SYMBOL	TEST CONDITION		LIMIT MIN.	LIMIT TYP.	LIMIT MAX.	UNIT	NOTE
High Level Input Voltage	V_{IH}	P10~2,PC2~3 PA,PB		0.8V_{DD}	-	V_{DD}+0.3	V	
Low Level Input Voltage	V_{IL}	P10~2,PC2~3 PA,PB		-0.3	-	0.3V_{DD}	V	
High Level Output Voltage	V_{OH}	P10~2,PC2~3 PA,PB	-I_{OH} = 0.5mA	V_{DD}-0.5	-	-	V	
Low Level Output Voltage	V_{OL}	P10~2,PC2~3 PA,PB	I_{OL} = 1.6mA	-	-	0.4	V	
Input Leakage Current	| I_{OL} |	P10~2,PC2~3 PA, PB	V_{IN} = 0V to V_{DD}	-	-	3	uA	1

Note : 1. Output buffer current is excluded.

2. HIGH VOLTAGE I/O PINS

V_{DD} = 4.5 to 5.5V, V_{SS} = 0V, V_{disp} = V_{DD} - 40V to V_{DD}

PARAMETER	SYMBOL	TEST CONDITION		LIMIT MIN.	LIMIT TYP.	LIMIT MAX.	UNIT	NOTE
High Level Input Voltage	V_{IH}	P0,P13,P2 P4, P5, P6		0.8V_{DD}	-	V_{DD}+0.3	V	
Low Level Input Voltage	V_{IL}	P0,P13,P2 P4, P5, P6		V_{DD}-40	-	0.3V_{DD}	V	
High Level Output Voltage	V_{OH}	P0,P13	-I_{OH} = 15mA	V_{DD}-3.0	-	-	V	
		P2, P4, P5	-I_{OH} = 10mA	V_{DD}-2.0	-	-	V	
		P6, BUZ	-I_{OH} = 4mA	V_{DD}-1.0	-	-	V	
Low Level Output Voltage	V_{OL}	P0,P13	V_{disp} = V_{DD} - 40V	-	-	V_{DD}-37	V	1
		P2, P4, P5 P6, BUZ	150§Ú at V_{DD} - 40 V	-	-	V_{DD}-37	V	2
Input Leakage Current	| I_{OL} |	P0,P13 P2, P4, P5 P6, BUZ	V_{disp} = V_{DD} - 40V to V_{DD}	-	-	20	uA	3
Pull-down MOS Current	I_d	P0,P13,P2 P4,P5,P6,BUZ	V_{disp} = V_{DD} - 35V V_{IN} = V_{DD}	200	-	1000	uA	1

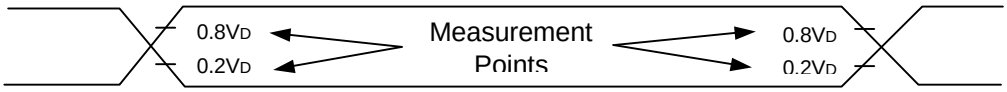
Notes : 1. Applies to pins with pull-down MOS as selected by the mask option.
2. Applies to pins without pull-down MOS as selected by the mask option.
3. Excludes outputs buffer current.

AC ELECTRICAL CHARACTERISTICS

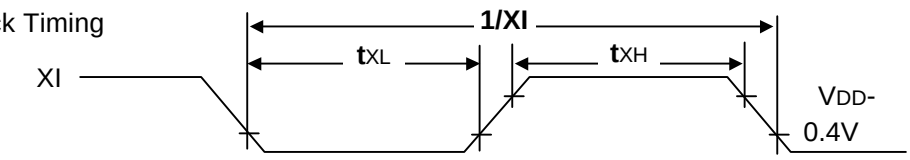
(T_A = -40 to +85¡É, V_{DD} = 2.7 to 6.0V)

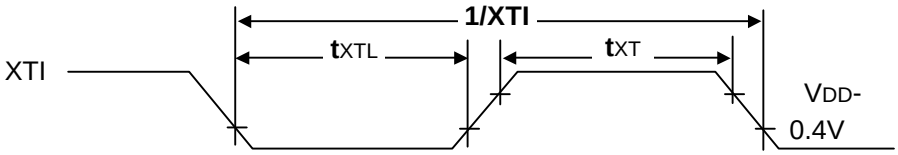
PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Cycle Time	t_{CY}	V_{DD} = 4.5 to 6.0V		0.95	-	64	uS
		V_{DD} = 2.7 to 3.3V		3.8	-	64	uS
TI Input Frequency	f_{TI}	V_{DD} = 4.5 to 6.0V		0	-	1	MHz
TI Input High, Low Level Width	t_{TIH}	V_{DD} = 4.5 to 6.0V		0.48	-	-	uS
$\overline{SCK}$ Cycle Time	t_{KCY}	V_{DD} = 4.5 to	Input	800	-	-	nS
			Output	950	-	-	nS
$\overline{SCK}$ High, Low Level Width	t_{KH}	V_{DD} = 4.5 to	Input	400	-	-	nS
			Output	t_{KCY}/2~50	-	-	nS
SI Set up Time to $\overline{SCK}$ High	t_{SIK}			100	-	-	nS
SI Hold Time to $\overline{SCK}$ High	t_{KSI}			400	-	-	nS
$\overline{SCK}$ to S0 Output Delay Time	t_{KSO}	V_{DD} = 4.5 to	Input	-	-	300	nS
			Output	-	-	250	nS
INT 0 ~ 4 Input Level High, Low	t_{INTH}			5	-	-	uS
	t_{INTL}			5	-	-	uS
RESETB Low Level	t_{RSL}			5	-	-	uS

AC Timing Measurement Points (Except XI and XTI)

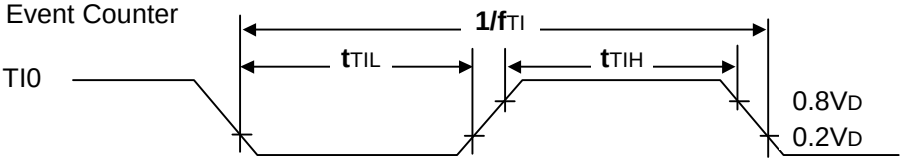


Clock Timing

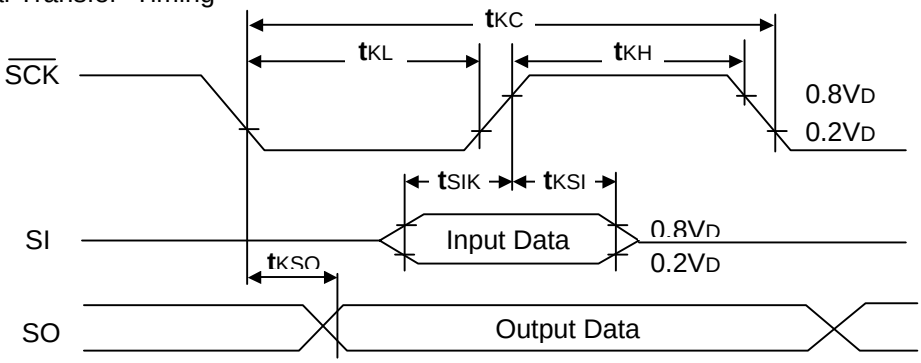




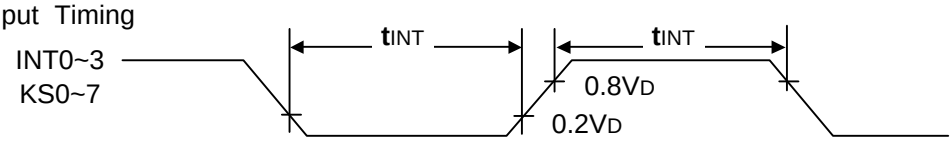
Timer Event Counter



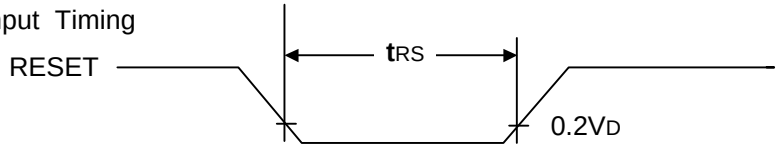
Serial Transfer Timing



Interrupt Input Timing



RESETB Input Timing



RAM DATA RETENTION CHARACTERISTICS (in STOP Mode)

(T_A = -40 to +85¡É)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Data Retention Supply Voltage	V_{DDDR}		2.0	-	6.0	V
Data Retention Supply Current	I_{DDDR}	V_{DDDR} = 2.0V	-	0.1	10	uA
Release Signal Set Time	t_{SREL}		0	-	-	uS
Oscillation Stabilization Wait Time	t_{WAIT}	When released by RESETB	-	2^{17}/fx	-	mS
		When released by interrupt Signal	-	NOTE 1)	-	mS

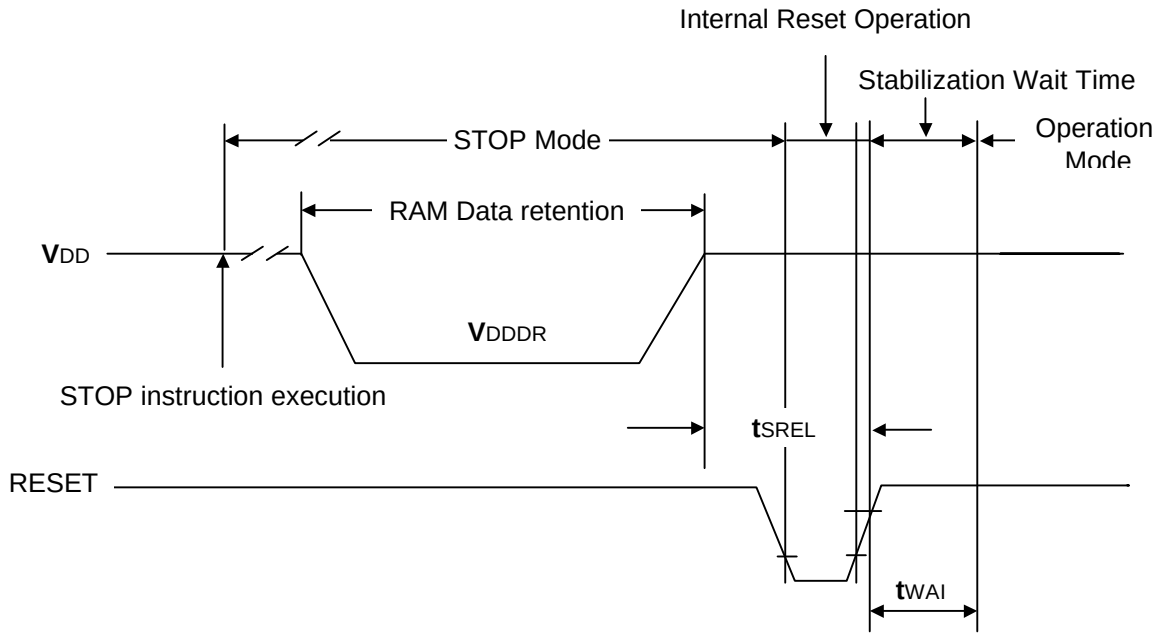
NOTE 1) Depends on the setting of the basic interval timer mode register.
(refer to the table below)

(fx = 4.19MHz)

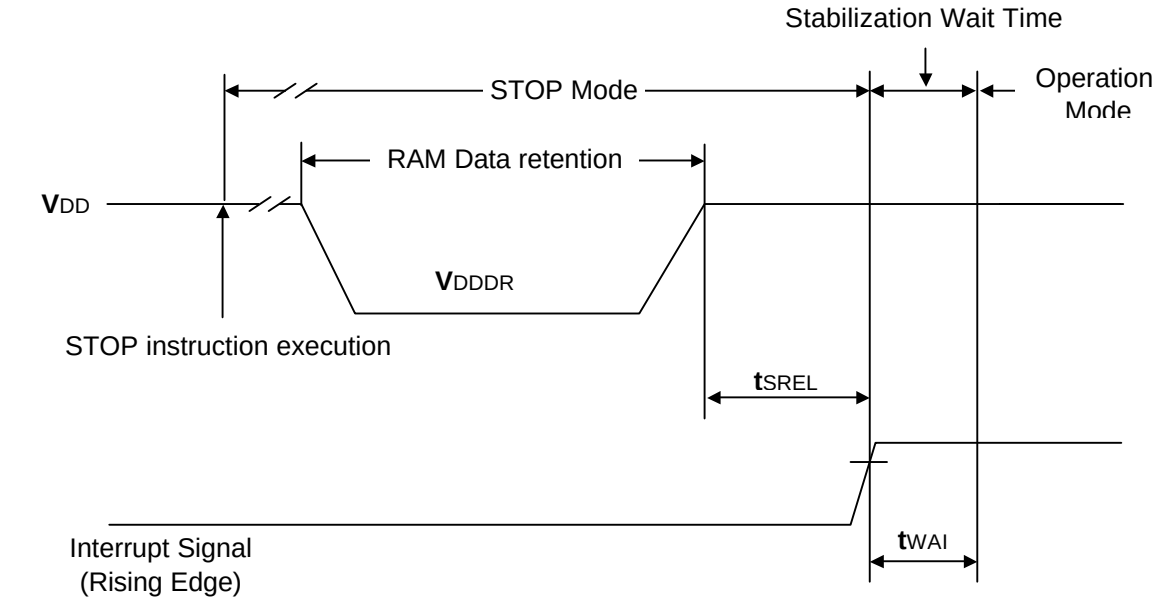
BMOD2	BMOD1	BMOD0	Oscillation Stabilization
0	0	0	2^{20}/fx (Approximately 250ms)
0	1	1	2^{17}/fx (Approximately 31.3ms)
1	0	0	2^{15}/fx (Approximately 7.82ms)
1	0	1	2^{13}/fx (Approximately 1.95ms)

RAM DATA RETENTION TIMING

When STOP mode is released by RESETB input



When STOP mode is released by interrupt signal



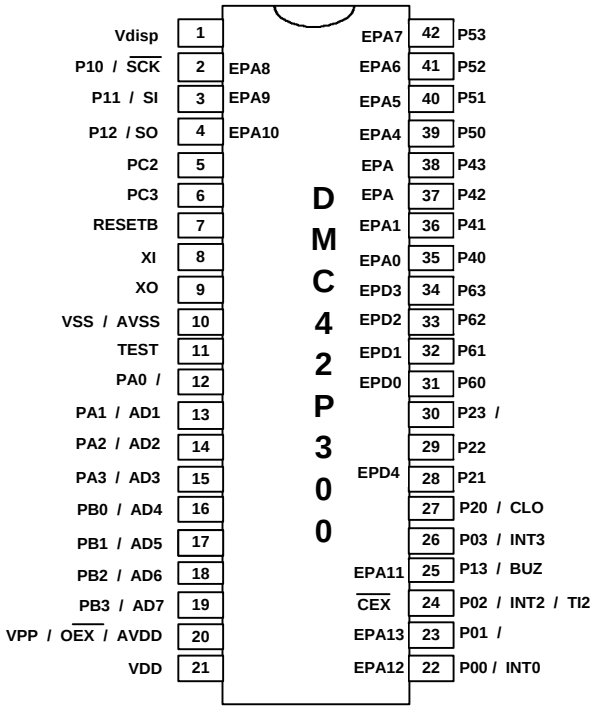
DMC42P3008

DESCRIPTION

The DMC42P3008 is a system evaluation LSI having a built in One-time PROM for DMC42C3008. A programming and verification for the internal PROM is achieved by using a general EPROM programmer with an adapter socket. The function of this device is exactly same as the DMC42C3008 by programming to the internal PROM. The DMC42P3008 is OTP version of the DMC42C3008 whose internal ROM has been changed from MASK ROM to EPROM.

* CAUTION : P3008 does not include internal pull-down resistor for high voltage output, so user has to connect externally.

PIN CONFIGURATION



DEVICE OPERATION

The operational modes of the DMC42P3008 are listed in Table 1.
A single 5V power supply is required in the read mode.
All inputs are TTL levels except for V_{PP} / $\overline{OEX}$.

V_{PP} = 12.5±0.5V

PINS / MODE	$\overline{CEX}$	V_{PP} / $\overline{OEX}$	V_{DD}	OUTPU
READ	V_{IL}	V_{IL}	5.0V	D_{OUT}
PROGRAM	V_{IL}	V_{PP}	6.0V	D_{IN}
VERIFY	V_{IL}	V_{IL}	6.0V	D_{OUT}
PROGRAM INHIBIT	V_{IH}	V_{PP}	6.0V	High Z

TABLE 1. Operating Modes

PIN NAME	MODE	
	EPROM MODE	USER MODE
TEST	V_{IH}	V_{IL}
RESETB	V_{IL}	V_{IH} / V_{II}

TABLE 2. The modes of DMC42P3008

DC PROGRAMMING CHARACTERISTICS

PARAMETER	SYMBO	TEST CONDITION	LIMIT		UNIT
			MIN.	MAX.	
Input Low Voltage	V_{IL}		-0.1	0.8	V
Input High Voltage	V_{IH}		2.0	V_{DD}	V
Output Low Voltage during Verify	V_{OL}	I_{OL} = 2.1mA	-	0.45	V
Output High Voltage during Verify	V_{OH}	I_{OH} = -400uA	2.4	-	V
Quick-pulse Programming	V_{PP}		12.5	13.0	V
Quick-pulse Programming	V_{DD}		6.0	6.5	V

PACKAGE DIMENSION

[UNIT : Millimeter]

42 SDIP