DALLAS
SEMICONDUCTOR

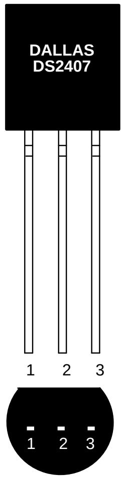
DS2407
Dual Addressable Switch Plus 1K–Bit Memory

FEATURES

- Open drain PIO pins are controlled and their logic level can be determined over 1–Wire^{TM} bus for closed–loop control
- Dual Channel operation (TSOC package)
- PIO pin channel A sink capability of 50 mA at 0.4V with soft turn–on; channel B 8 mA at 0.4V
- Maximum operating voltage of 13V at PIO–A, 6.5V at PIO–B
- 1024 bits user–programmable OTP EPROM
- 7 bytes of user–programmable status memory to control the device
- Multiple DS2407s can be identified on a common 1–Wire bus and be turned on or off independently of other devices on the bus
- Unique, factory–lasered and tested 64–bit registration number (8–bit family code + 48–bit serial number + 8–bit CRC tester) assures error–free selection and absolute identity because no two parts are alike
- On–chip CRC16 generator allows detection of data transfer errors
- Built–in multidrop controller ensures compatibility with other MicroLAN^{TM} products
- Reduces control, address, data, programming and power to a single data pin
- Directly connects to a single port pin of a microprocessor and communicates at up to 16.3k bits/s
- Low cost TO–92 or 6–pin TSOC surface mount package
- 1–Wire communication operates over a wide voltage range of 2.8V to 6.0V from –40°C to +85°C
- Supports Conditional Search with user–programmable condition
- V_{CC} bondout for optional external supply to the device (TSOC package only)
- Hidden Mode; the device will respond only to a Match ROM command or a Conditional Search when in this mode.

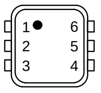
PIN ASSIGNMENT

TO–92



BOTTOM VIEW
See Mech. Drawings
Section

TSOC PACKAGE



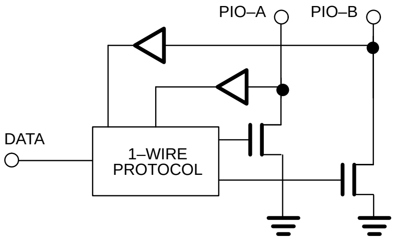
TOP VIEW
3.7 X 4.0 X 1.5 mm

SIDE VIEW

See Mech. Drawings
Section

PIN DESCRIPTION

	TO–92	TSOC
Pin 1	Ground	Ground
Pin 2	Data	Data
Pin 3	PIO–A	PIO–A
Pin 4	——	V_{CC}
Pin 5	——	NC
Pin 6	——	PIO–B



ORDERING INFORMATION

DS2407	TO–92 package
DS2407P	6–pin TSOC package
DS2407T	Tape & Reel version of DS2407
DS2407V	Tape & Reel version of DS2407P
DS2407X	Chip Scale Pkg., Tape & Reel

ADDRESSABLE SWITCH^{TM} DESCRIPTION

The DS2407 Dual Addressable Switch Plus Memory is a pair of open drain N–channel transistors that can be turned on or off via the 1–Wire bus. Alternatively, either open drain output can serve as a logic input that can be monitored via the same 1–Wire bus. In addition, the device has 1024 bits of EPROM to store relevant information such as switch function, physical location, etc. The device is addressed by matching its individual 64–bit factory–lasered registration number. The 64–bit number consists of an 8–bit family code, a unique 48–bit serial number, and an 8–bit cyclic redundancy check. Communication with the DS2407 follows the standard Dallas Semiconductor 1–Wire protocol and can be accomplished with a single port pin of a microcontroller. Multiple DS2407 devices can reside on a common 1–Wire bus creating a MicroLAN. The network controller circuitry is embedded within the chip including a search algorithm to determine the identity of each DS2407 on the network. The open drain outputs (PIO pins) for each DS2407 on the MicroLAN can be independently switched on or off whether there is one or many devices sharing the same 1–Wire bus. The logic level of the PIO pins for each device on the MicroLAN can also be individually sensed and reported to the bus master. The device also supports a Conditional Search command to identify and access devices that qualify for certain user–specified conditions. Qualification may be the status of a PIO–pin, the state of the output transistor or a latched activity flag.

OVERVIEW

The DS2407 Dual Addressable Switch Plus Memory provides a means for assigning an electronically readable identification to a particular node or location with additional control capability provided by two open–drain N–channel MOSFETs that can be remotely switched and sensed via communication over the 1–Wire bus (Figure 1). The DS2407 contains a factory–lasered registration number that includes a unique 48–bit serial number, an 8–bit CRC, and an 8–bit family code (12h). The 64–bit ROM portion of the DS2407 not only creates an absolutely unique electronic identification for the device itself but also is a means to locate and obtain or change the state of the switches that are associated with the 64–bit ROM.

The device derives its power entirely from the 1–Wire bus by storing energy on an internal capacitor during periods of time when the signal line is high and continues to operate off of this “parasite” power source during the low times of the 1–Wire line until it returns high to replenish the parasite (capacitor) supply. For applications in feeder–networks where the low–times of the 1–Wire line may be very long, the V_{CC} pin may be connected to an external voltage supply to operate the device.

The DS2407 uses the standard Dallas Semiconductor 1–Wire protocol for data transfers (Figure 2), with all data being read and written least significant bit first. Communication to and from the DS2407 requires a single bi–directional line that is typically a port pin of a microcontroller. The 1–Wire bus master (microcontroller) must first issue one of five ROM function commands: 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Skip ROM, or 5) Conditional Search ROM. These commands operate on the 64–bit lasered ROM portion of each device and can singulate a specific device if many are present on the 1–Wire line as well as indicate to the bus master how many and what type of each device is present. After a ROM function command is successfully executed, the open–drain outputs can be switched or sensed, or the contents of the memory can be read or written via the 1–Wire bus. Writing the 1024 bits of data memory or writing to the EPROM sections of the status memory requires a 12V programming pulse. When programming the DS2407, only EPROM–based devices are allowed to be present on the 1–Wire line.

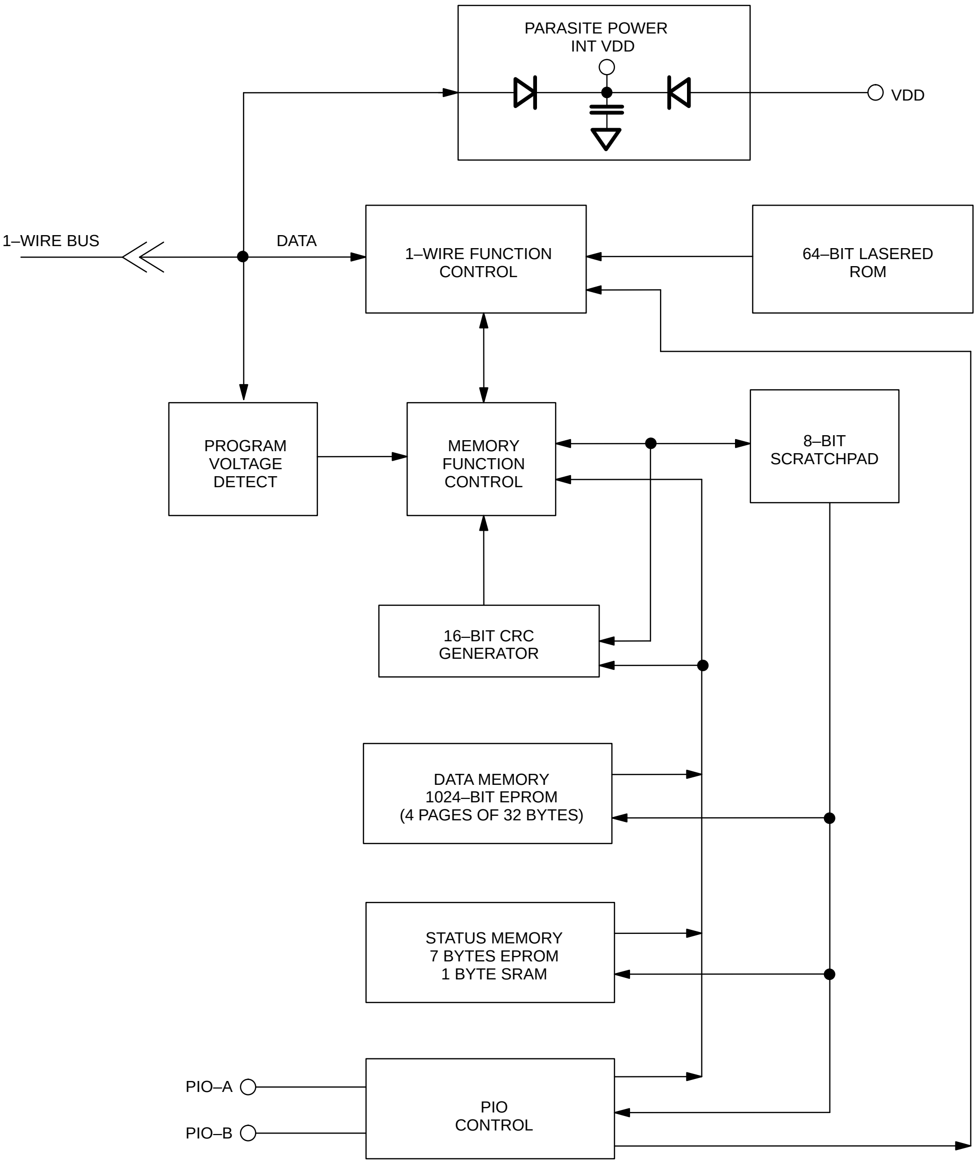
64–BIT LASERED ROM

Each DS2407 contains a unique ROM code that is 64 bits long. The first eight bits are a 1–Wire family code. The next 48 bits are a unique serial number. The last eight bits are a CRC of the first 56 bits. (See Figure 3.) The 1–Wire CRC of the lasered ROM is generated using the polynomial $X^8 + X^5 + X^4 + 1$. Additional information about the Dallas Semiconductor 1–Wire Cyclic Redundancy Check is available in the Book of DS19xx iButton Standards. The 64–bit ROM and ROM Function Control section allow the DS2407 to operate as a 1–Wire device and follow the 1–Wire protocol detailed in the section “1–Wire Bus System”. The functions required to read and write the data and status memory of the DS2407 and to access the switches are not accessible until the ROM function protocol has been satisfied. This protocol is described in the ROM functions flow chart (Figure 12). The 1–Wire bus master must first provide one of the five ROM function commands. After a ROM function sequence has been successfully executed, the bus master may then provide any one of the memory function commands specific to the DS2407 (Figure 6).

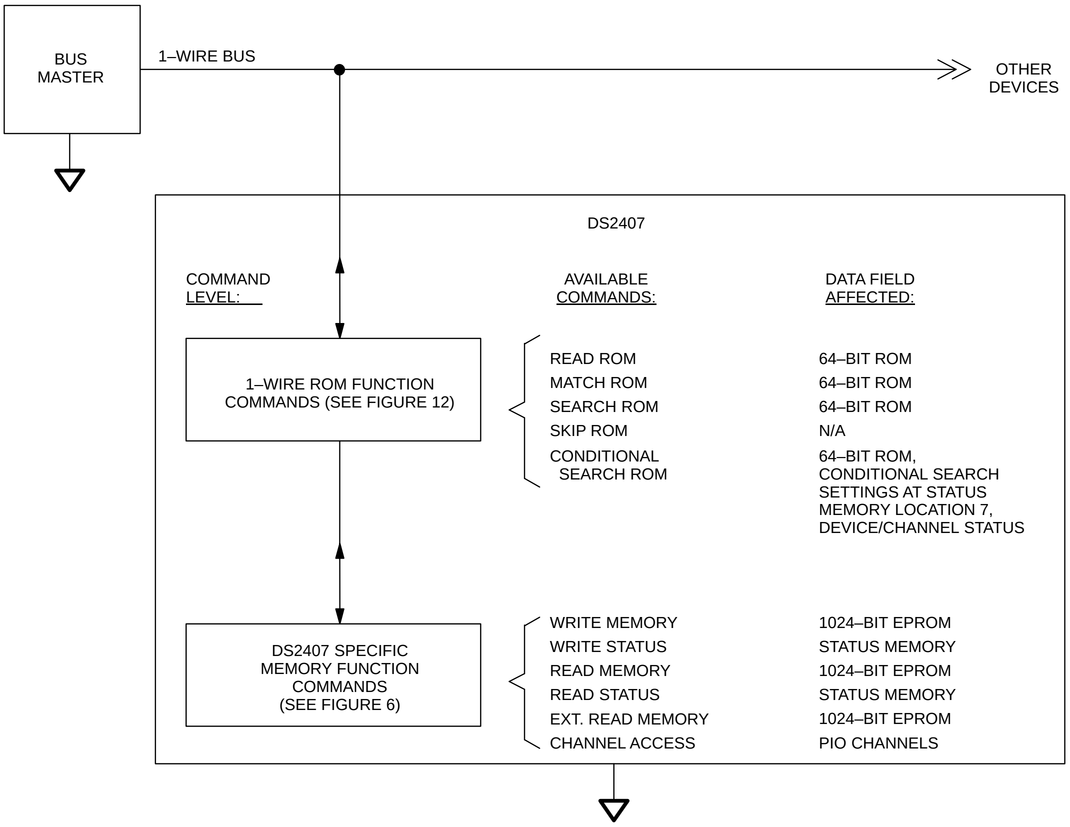
MEMORY

The DS2407 contains two memory sections, Data Memory and Status Memory. The data memory consists of 1024 bits of one–time programmable EPROM organized as 4 pages of 32 bytes each. The size of the device’s status memory is 8 bytes. The first seven bytes of status memory (addresses 0 to 6) are also realized as EPROM. The eighth byte (address 7) consists of SRAM cells which shadow the contents of address 6 each time the device powers up. The complete memory map is shown in Figure 4. The 8–bit scratchpad is an additional register that acts as a buffer when writing the memory. Data is first written to the scratchpad and then verified by reading a 16–bit CRC from the DS2407 that confirms proper receipt of the data and address. If the buffer contents are correct, a programming pulse should be applied and the byte of data will be written into the selected address in memory. This process insures data integrity when programming the memory. The details for reading and programming the EPROM portions of the DS2407 are given in the Memory Function Commands section.

DS2407 BLOCK DIAGRAM Figure 1


PARASITE POWER
INT VDD
VDD
1–WIRE BUS
DATA
1–WIRE FUNCTION CONTROL
64–BIT LASERED ROM
PROGRAM VOLTAGE DETECT
MEMORY FUNCTION CONTROL
8–BIT SCRATCHPAD
16–BIT CRC GENERATOR
DATA MEMORY
1024–BIT EPROM
(4 PAGES OF 32 BYTES)
STATUS MEMORY
7 BYTES EPROM
1 BYTE SRAM
PIO–A
PIO–B
PIO CONTROL

HIERARCHICAL STRUCTURE FOR 1–WIRE PROTOCOL Figure 2

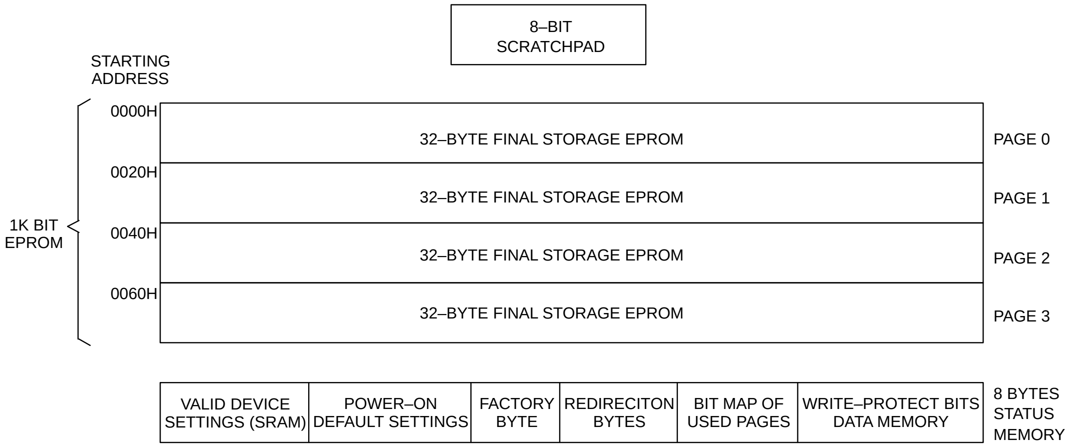

BUS MASTER
1–WIRE BUS
OTHER DEVICES
DS2407
COMMAND LEVEL:
AVAILABLE COMMANDS:
DATA FIELD AFFECTED:
1–WIRE ROM FUNCTION COMMANDS (SEE FIGURE 12)
DS2407 SPECIFIC MEMORY FUNCTION COMMANDS (SEE FIGURE 6)

COMMAND LEVEL:	AVAILABLE COMMANDS:	DATA FIELD AFFECTED:
1–WIRE ROM FUNCTION COMMANDS (SEE FIGURE 12)	READ ROM	64–BIT ROM
	MATCH ROM	64–BIT ROM
	SEARCH ROM	64–BIT ROM
	SKIP ROM	N/A
	CONDITIONAL SEARCH ROM	64–BIT ROM, CONDITIONAL SEARCH SETTINGS AT STATUS MEMORY LOCATION 7, DEVICE/CHANNEL STATUS
DS2407 SPECIFIC MEMORY FUNCTION COMMANDS (SEE FIGURE 6)	WRITE MEMORY	1024–BIT EPROM
	WRITE STATUS	STATUS MEMORY
	READ MEMORY	1024–BIT EPROM
	READ STATUS	STATUS MEMORY
	EXT. READ MEMORY	1024–BIT EPROM
	CHANNEL ACCESS	PIO CHANNELS

64–BIT LASERED ROM Figure 3

8–Bit CRC Code		48–Bit Serial Number		8–Bit Family Code (12H)	
MSB	LSB	MSB	LSB	MSB	LSB

DS2407 MEMORY MAP Figure 4


8–BIT
SCRATCHPAD
STARTING
ADDRESS
1K BIT
EPROM
0000H
0020H
0040H
0060H
32–BYTE FINAL STORAGE EPROM
32–BYTE FINAL STORAGE EPROM
32–BYTE FINAL STORAGE EPROM
32–BYTE FINAL STORAGE EPROM
PAGE 0
PAGE 1
PAGE 2
PAGE 3
VALID DEVICE SETTINGS (SRAM)
POWER–ON DEFAULT SETTINGS
FACTORY BYTE
REDIRECITON BYTES
BIT MAP OF USED PAGES
WRITE–PROTECT BITS DATA MEMORY
8 BYTES
STATUS
MEMORY

DS2407 STATUS MEMORY MAP Figure 5

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0 (EPROM)	BM 3	BM 2	BM 1	BM 0	WP 3	WP 2	WP 1	WP 0
1 (EPROM)	1	1	1	1	1	1	Redir. 0	Redir. 0
2 (EPROM)	1	1	1	1	1	1	Redir. 1	Redir. 1
3 (EPROM)	1	1	1	1	1	1	Redir. 2	Redir. 2
4 (EPROM)	1	1	1	1	1	1	Redir. 3	Redir. 3
5 (EPROM)	EPROM factory byte							
6 (EPROM	X	Pwr–On Status PIO–B	Pwr–On Status PIO–A	Pwr–On Status CSS4	Pwr–On Status CSS3	Pwr–On Status CSS2	Pwr–On Status CSS1	Pwr–On Status CSS0
7 (SRAM)	Supply Indication (read only)	PIO–B Channel Flip–Flop	PIO–A Channel Flip–Flop	CSS4 Channel Select	CSS3 Channel Select	CSS2 Source Select	CSS1 Source Select	CSS0 Polarity

STATUS MEMORY

The Status Memory can be read or written to indicate various conditions to the software interrogating the DS2407. These conditions include special features for the data memory, definition of the power–on default and actual settings for the Conditional Search as well as the channel flip–flops and the external power supply indication. How these functions are assigned to the bits of the Status Memory is detailed in Figure 5. The channel flip–flops and power supply indication are also included in the Channel Info Byte of the Channel Access command protocol (see Figure 6).

The first four bits of the Status Memory (address 0, bits 0 to 3) contain the Write Protect Page bits which inhibit programming of the corresponding page in the 1024–bit data memory area if the appropriate write protection bit is programmed. Once a bit has been programmed in the Write Protect Page section of the Status Memory, the entire 32 byte page that corresponds to that bit can no longer be altered but may still be read. The remaining 4 bits of Status Memory location 0 are reserved for use by the iButton operating software TMEX. Their purpose is to indicate which memory pages are already in use. Originally, all of these bits are unprogrammed, indicating that the device does not contain any data. As soon as data is written to any page of the device under control of TMEX, the bit inside this bitmap corresponding to that page will be programmed to 0, marking this page as used. These bits are application flags only and have no impact on the internal logic of the DS2407.

The next four bytes of the Status Memory (addresses 1 to 4) contain the Page Address Redirection Bytes which indicate if one or more of the pages of data in the 1024–bits EPROM memory section have been invalidated by software and redirected to the page address contained in the appropriate redirection byte. The hardware of the DS2407 makes no decisions based on the contents of the Page Address Redirection Bytes. Since with EPROM technology bits can only be changed from a logical 1 to a logical 0 by programming, it is not possible to simply rewrite a page if the data requires changing or updating. But with space permitting, an entire page of data can be redirected to another page within the DS2407. Under TMEX, a page is redirected by writing the one’s complement of the new page address into the Page Address Redirection Byte that corresponds to the original (replaced) page. This architecture allows the user’s software to make a “data patch” to the EPROM by indicating that a particular page or pages should be replaced with those indicated in the Page Address Redirection Bytes.

Under TMEX, if a Page Address Redirection Byte has a FFh value, the data in the main memory that corresponds to that page is valid. If a Page Address Redirection Byte has some other hex value than FFh, the data in the page corresponding to that redirection byte is invalid. According to the TMEX definitions, the valid data will now be found at the one’s complement of the page address indicated by the hex value stored in the associated Page Address Redirection Byte. A value of FDh in the redirection byte for page 1, for example, would indicate that the updated data is now in page 2. Since the data memory consists of four pages only, the 6 most significant bits of the redirection bytes cannot be programmed to zeros.

Status Memory location 5 is programmed to 00h at the factory. Status Memory location 6 contains the power–on default settings for the Conditional Search Select (CSS0 to CSS4, bits 0 to 4) and the PIO channels. The power–on settings become valid as they are internally transferred by the device into Status Memory location 7 after the device has powered up and the bus master sends a ROM Function Command byte for the first time. The codes for the Conditional Search Settings are detailed with the description of the Conditional Search command later in this data sheet. If both CSS1 and CSS2 in Status Memory Location 7 are set to zero, the DS2407 will enter a “Hidden Mode” where it will keep its status but only responds to Match ROM and Conditional Search. To respond to Conditional Search the polarity (CSS0) needs to be 1. The “Hidden Mode” can be ended either by a power–on reset or by matching the device’s registration number and setting CSS1 or CSS2 to 1.

The output transistors of both channels are controlled by their channel flip–flops. These flip–flops are accessible through bit locations 5 and 6 of Status Memory address 7 as well as through the Channel Access command. Setting a channel flip–flop to 0 will make the associated PIO–transistor conducting or on, setting the flip–flop to 1 will switch the transistor off. When powering up, the output transistors of both channels are non–conducting or off. They may change their status as the user–programmed power–on status is transferred into Status Memory location 7. Bit 7 of Status Memory Location 7 indicates if the DS2407 is connected to an external power supply. Without external supply this read–only bit will be 0. If the voltage applied to the V_{CC} pin is high enough to keep the device powered up, this bit will be 1.

The Status Memory is programmed similarly to the data memory. Details for reading and programming the status memory portion of the DS2407 are given in the Memory Function Commands section.

MEMORY FUNCTION COMMANDS

The "Memory Function Flow Chart" (Figure 6) describes the protocols necessary for accessing the various data fields and PIO channels within the DS2407. The Memory Function Control section, 8–bit scratchpad, and the Program Voltage Detect circuit combine to interpret the commands issued by the bus master and create the correct control signals within the device. A three–byte protocol is issued by the bus master. It is comprised of a command byte to determine the type of operation and two address bytes to determine the specific starting byte location within a data field or to supply and exchange setup and status data when accessing the PIO channels. The command byte indicates if the device is to be read or written or if the PIO channels are to be accessed. Writing data involves not only issuing the correct command sequence but also providing a 12–volt programming voltage at the appropriate times. To execute a write sequence, a byte of data is first loaded into the scratchpad and then programmed into the selected address. Write sequences always occur a byte at a time. To execute a read sequence, the starting address is issued by the bus master and data is read from the part beginning at that initial location and continuing to the end of the selected data field or until a reset sequence is issued. All bits transferred to the DS2407 and received back by the bus master are sent least significant bit first.

READ MEMORY [F0h]

The Read Memory command is used to read data from the 1024–bit EPROM data memory field. The bus master follows the command byte with a two–byte address (TA1=(T7:T0), TA2=(T15:T8)) that indicates a starting byte location within the data field. Since the data memory contains 128 bytes, T15:T8 and T7 should all be zero. With every subsequent read data time slot the bus master receives data from the DS2407 starting at the initial address and continuing until the end of the 1024–bits data field is reached or until a Reset Pulse is issued. If reading occurs through the end of memory space, the bus master may issue sixteen additional read time slots and the DS2407 will respond with a 16–bit CRC of the command, address bytes and all data bytes read from the initial starting byte through the last byte of memory. This CRC is the result of clearing the CRC generator and then shifting in the command byte followed by the two address bytes and the data bytes beginning at the first addressed memory location and continuing through to the last byte of the EPROM data memory. After the CRC is received by the bus master, any subsequent read time slots will appear as logical 1s until a Reset Pulse is issued. Any reads ended by a Reset Pulse prior to reaching the end of memory will not have the 16–bit CRC available.

Typically the software controlling the device should store a 16–bit CRC with each page of data to insure rapid, error–free data transfers that eliminate having to read a page multiple times to determine if the received data is correct or not. (See Book of DS19xx iButton Standards, Chapter 7 for the recommended file structure to be used with the 1–Wire environment). If CRC values are imbedded within the data it is unnecessary to read the end–of–memory CRC. The Read Memory command can be ended at any point by issuing a Reset Pulse.

EXTENDED READ MEMORY [A5h]

The Extended Read Memory command supports page redirection when reading data from the 1024–bit EPROM data field. One major difference between the Extended Read Memory and the basic Read Memory command is that the bus master receives the Redirection Byte (see description of Status Memory) first before investing time in reading data from the addressed memory location. This allows the bus master to quickly decide whether to continue and access the data at the selected starting page or to terminate and restart the reading process at the redirected page address.

In addition to page redirection, the Extended Read Memory command also supports "bit–oriented" applications where the user cannot store a 16–bit CRC with the data itself. With bit–oriented applications the EPROM information may change over time within a page boundary making it impossible to include an accompanying CRC that will always be valid. Therefore, the Extended Read Memory command concludes each page with the DS2407 generating and supplying a 16–bit CRC that is based on and therefore always consistent with the current data stored in each page of the 1024–bit EPROM data field.

After having sent the command code of the Extended Read Memory command, the bus master sends a two–byte address (TA1=(T7:T0), TA2=(T15:T8)) that indicates a starting byte location within the data field. By sending eight read data time slots, the master receives the Redirection Byte associated with the page given by the starting address. With the next sixteen read data time slots, the bus master receives a 16–bit CRC of the command byte, address bytes and the Redirection Byte. This CRC is computed by the DS2407 and read back by the bus master to check if the command word, starting address and Redirection Byte were received correctly.

If the CRC read by the bus master is incorrect, a Reset Pulse must be issued and the entire sequence must be repeated. If the CRC received by the bus master is correct, the bus master issues read time slots and receives data from the DS2407 starting at the initial address and continuing until the end of a 32–byte page is reached. At that point the bus master will send sixteen additional read time slots and receive a 16–bit CRC that is the result of shifting into the CRC generator all of the data bytes from the initial starting byte to the last byte of the current page.

With the next 24 read data time slots the master will receive the Redirection Byte of the next page followed by a 16–bit CRC of the Redirection Byte. After this, data is again read from the 1024–bits EPROM data field starting at the beginning of the new page. This sequence will continue until the final page and its accompanying CRC are read by the bus master.

The Extended Read Memory command provides a 16–bit CRC at two locations within the transaction flow chart: 1) after the Redirection Byte and 2) at the end of each memory page. The CRC at the end of the memory page is always the result of clearing the CRC generator and shifting in the data bytes beginning at the first addressed memory location of the EPROM data page until the last byte of this page. With the initial pass through the Extended Read Memory flow chart the 16–bit CRC value after the Redirection Byte is the result of shifting the command byte into the cleared CRC generator, followed by the two address bytes and the Redirection Byte. Subsequent passes through the Extended Read Memory flow chart will generate a 16–bit CRC that is the result of clearing the CRC generator and then shifting in the Redirection Byte only. After the 16–bit CRC of the last page is read, the bus master will receive logical 1s from the DS2407 until a Reset Pulse is issued. The Extended Read Memory command sequence can be ended at any point by issuing a Reset Pulse.

WRITING EPROM MEMORY

The DS2407 has two independent EPROM memory fields, Data Memory and Status Memory. The function flow for writing either field is almost identical. After the appropriate write command has been issued, the bus master will send a two–byte starting address (TA1=(T7:T0), TA2=(T15:T8)) and a byte of data (D7:D0). A 16–bit CRC of the command byte, address bytes, and data byte is computed by the DS2407 and read back by the bus master to confirm that the correct command word, starting address, and data byte were received.

If the CRC read by the bus master is incorrect, a Reset Pulse must be issued and the entire sequence must be repeated. If the CRC received by the bus master is correct, a programming pulse (12 volts on the 1–Wire bus for 480 µs) is issued by the bus master. Prior to programming, the entire unprogrammed EPROM memory field will appear as logical 1s. For each bit in the data byte provided by the bus master that is set to a logical 0, the corresponding bit in the selected byte of the EPROM memory is programmed to a logical 0 after the programming pulse has been applied.

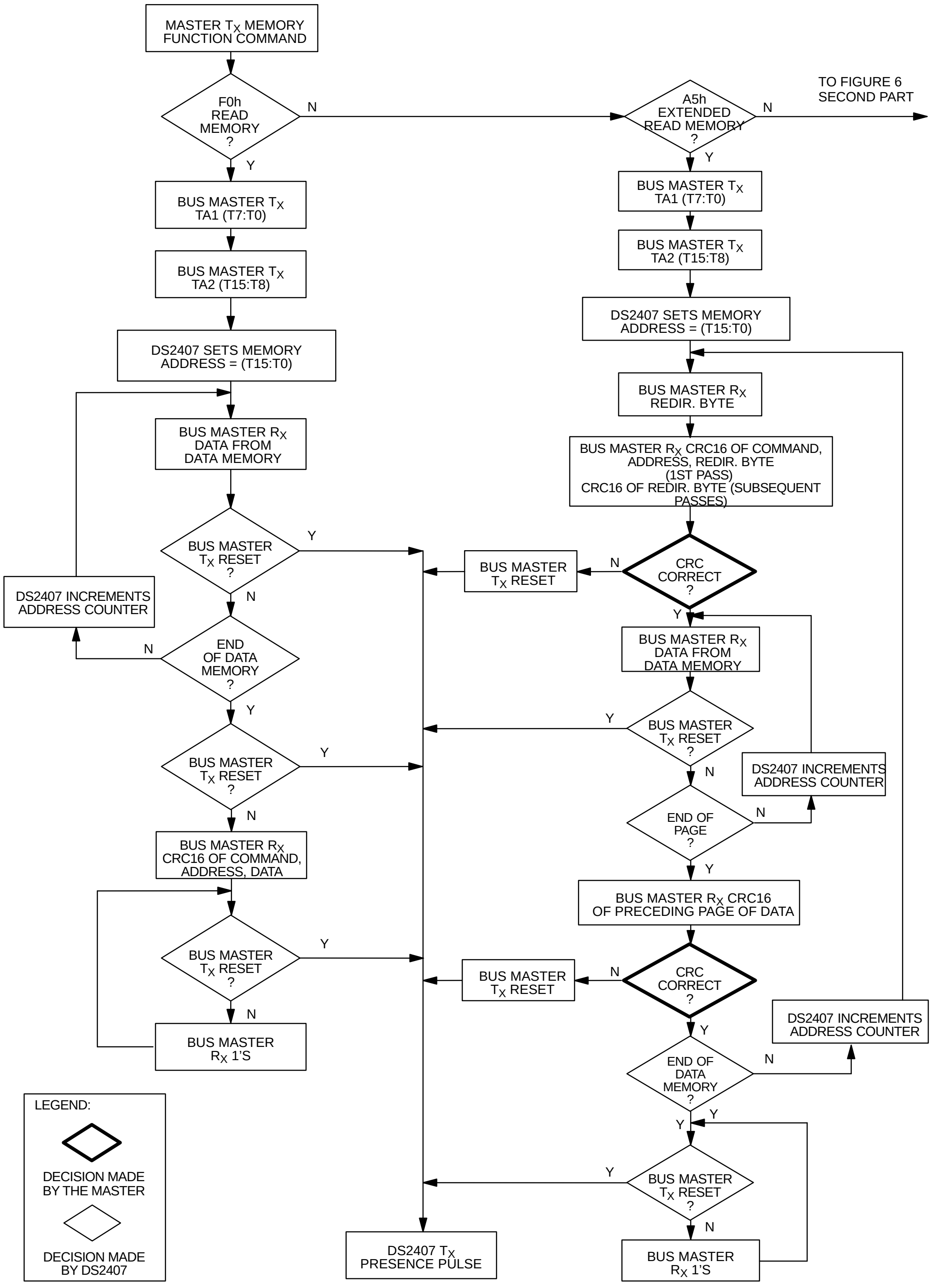
After the 480 µs programming pulse is applied and the data line returns to the idle level (5 volts), the bus master issues eight read time slots to verify that the appropriate bits have been programmed. The DS2407 responds with the data from the selected EPROM address sent least significant bit first. This byte contains the bitwise logical AND of all data ever written to this address. If the EPROM byte contains 1s in bit positions where the byte issued by the master contained 0s, a Reset Pulse should be issued and the current byte address should be programmed again. If the DS2407 EPROM byte contains 0s in the same bit positions as the data byte, the programming was successful and the DS2407 will automatically increment its address counter to select the next byte in the EPROM memory field. The new two–byte address will also be loaded into the 16–bit CRC generator as a starting value. The bus master will issue the next byte of data using eight write time slots.

As the DS2407 receives this byte of data into the scratchpad, it also shifts the data into the CRC generator that has been preloaded with the current address and the result is a 16–bit CRC of the new data byte and the new address. After supplying the data byte, the bus master will read this 16–bit CRC from the DS2407 with sixteen read time slots to confirm that the address incremented properly and the data byte was received correctly. If the CRC is incorrect, a Reset Pulse must be issued and the write sequence must be restarted. If the CRC is correct, the bus master will issue a programming pulse and the selected byte in memory will be programmed.

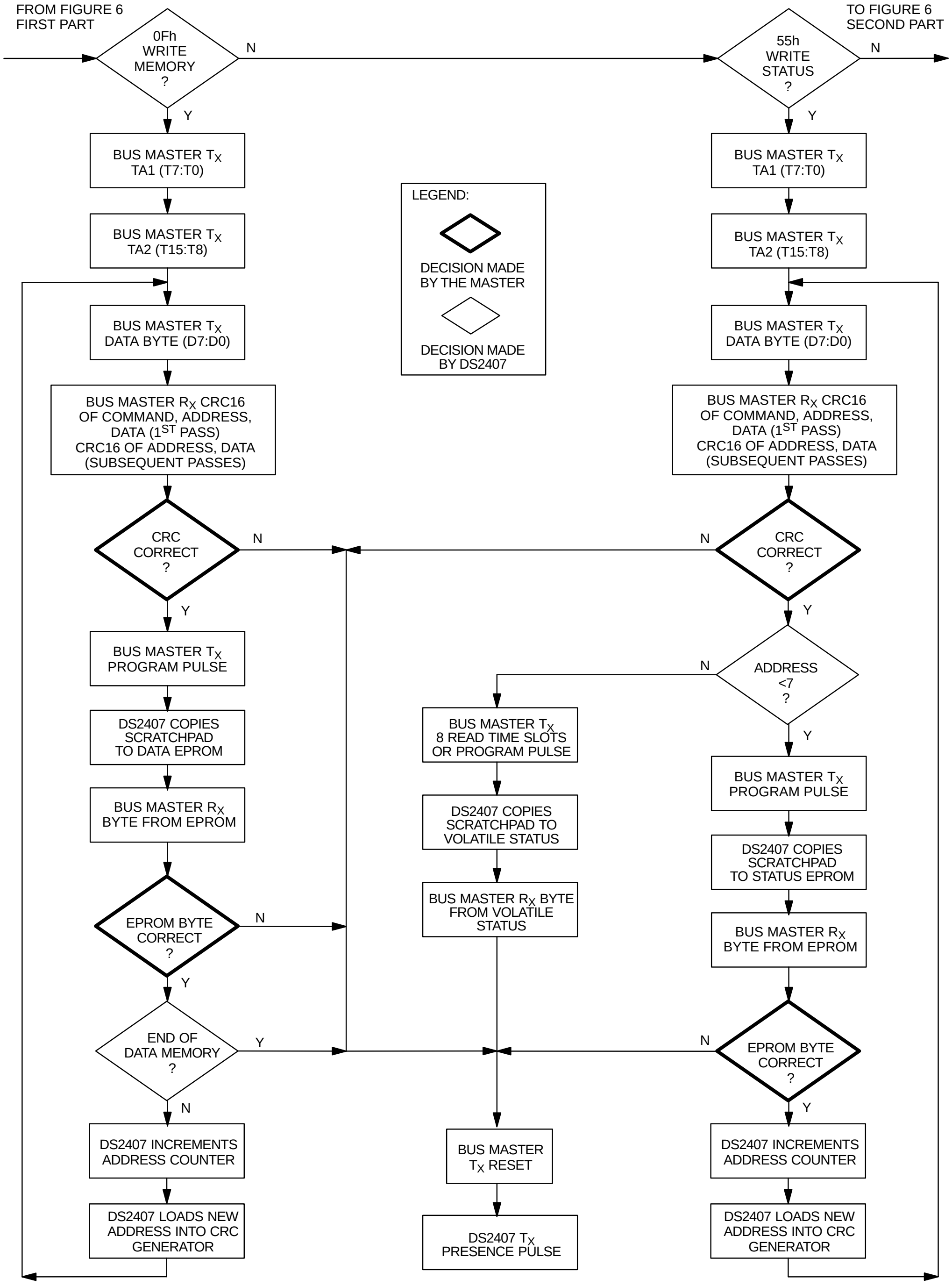
Note that the initial pass through the write flow chart will generate an 16–bit CRC value that is the result of shifting the command byte into the CRC generator, followed by the two address bytes, and finally the data byte. Subsequent passes through the write flow chart due to the DS2407 automatically incrementing its address counter will generate a 16–bit CRC that is the result of loading (not shifting) the new (incremented) address into the CRC generator and then shifting in the new data byte.

For both of these cases, the decision to continue (to apply a program pulse to the DS2407) is made entirely by the bus master, since the DS2407 will not be able to determine if the 16–bit CRC calculated by the bus master agrees with the 16–bit CRC calculated by the DS2407. If an incorrect CRC is ignored and a program pulse is applied by the bus master, incorrect programming could occur within the DS2407. Also note that the DS2407 will always increment its internal address counter after the receipt of the eight read time slots used to confirm the programming of the selected EPROM byte. The decision to continue is again made entirely by the bus master. Therefore if the EPROM data byte does not match the supplied data byte but the master continues with the write command, incorrect programming could occur within the DS2407. The write command sequence can be ended at any point by issuing a Reset Pulse.

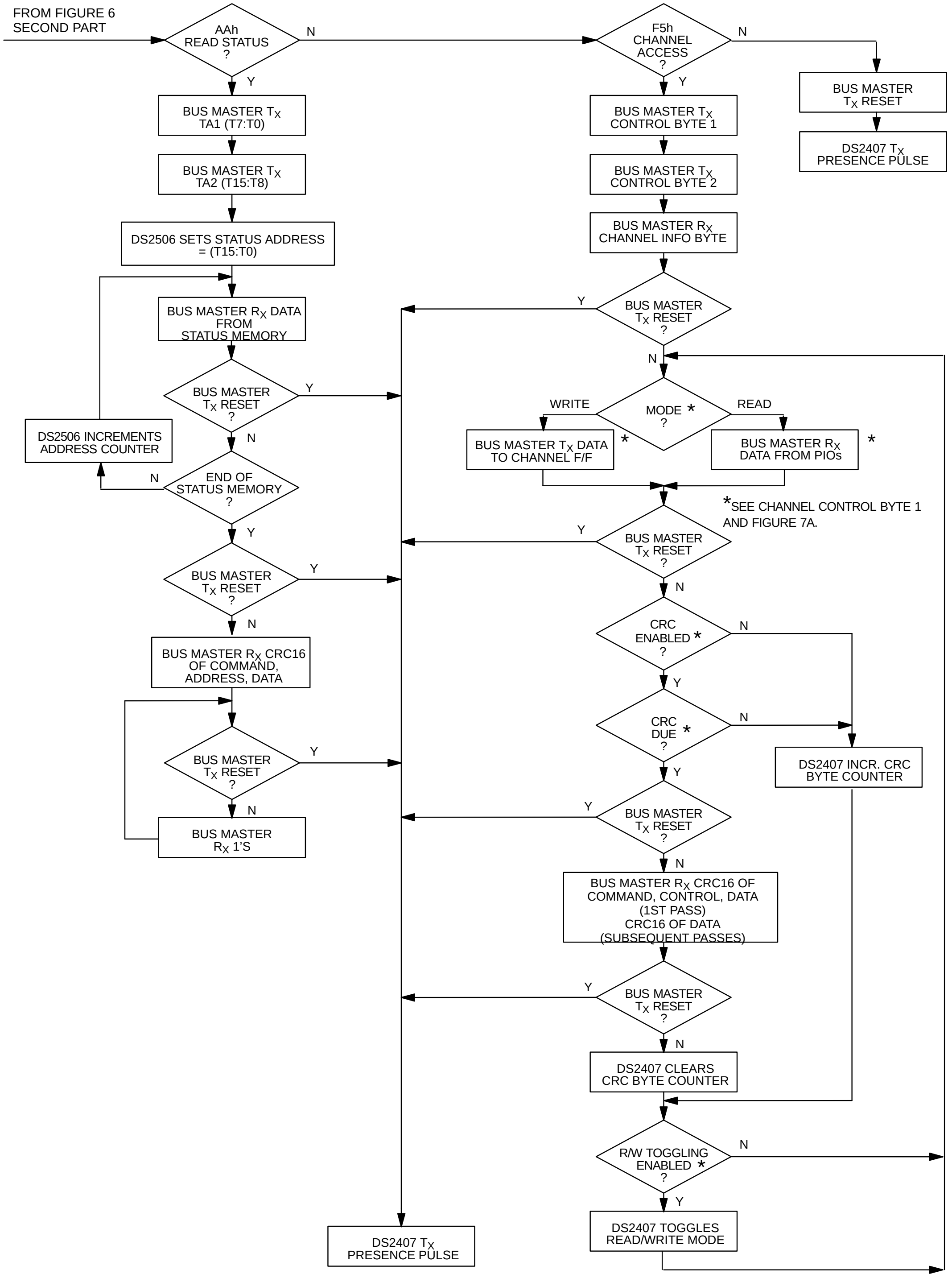
MEMORY FUNCTION FLOW CHART Figure 6


MASTER T_X MEMORY FUNCTION COMMAND
F0h READ MEMORY ?
N
Y
A5h EXTENDED READ MEMORY ?
N
TO FIGURE 6 SECOND PART
Y
BUS MASTER T_X TA1 (T7:T0)
BUS MASTER T_X TA2 (T15:T8)
DS2407 SETS MEMORY ADDRESS = (T15:T0)
BUS MASTER T_X TA1 (T7:T0)
BUS MASTER T_X TA2 (T15:T8)
DS2407 SETS MEMORY ADDRESS = (T15:T0)
BUS MASTER R_X REDIR. BYTE
BUS MASTER R_X DATA FROM DATA MEMORY
BUS MASTER R_X CRC16 OF COMMAND, ADDRESS, REDIR. BYTE (1ST PASS) CRC16 OF REDIR. BYTE (SUBSEQUENT PASSES)
BUS MASTER T_X RESET ?
Y
N
BUS MASTER T_X RESET
CRC CORRECT ?
N
Y
DS2407 INCREMENTS ADDRESS COUNTER
END OF DATA MEMORY ?
N
Y
BUS MASTER R_X DATA FROM DATA MEMORY
BUS MASTER T_X RESET ?
Y
N
BUS MASTER T_X RESET ?
Y
N
DS2407 INCREMENTS ADDRESS COUNTER
END OF PAGE ?
N
Y
BUS MASTER R_X CRC16 OF COMMAND, ADDRESS, DATA
BUS MASTER R_X CRC16 OF PRECEDING PAGE OF DATA
BUS MASTER T_X RESET ?
Y
N
BUS MASTER T_X RESET
CRC CORRECT ?
N
Y
DS2407 INCREMENTS ADDRESS COUNTER
BUS MASTER R_X 1'S
END OF DATA MEMORY ?
N
Y
LEGEND:
DECISION MADE BY THE MASTER
DECISION MADE BY DS2407
Y
BUS MASTER T_X RESET ?
Y
N
DS2407 T_X PRESENCE PULSE
BUS MASTER R_X 1'S

MEMORY FUNCTION FLOW CHART Figure 6 (cont'd)


FROM FIGURE 6
FIRST PART
0Fh
WRITE
MEMORY
?
N
Y
TO FIGURE 6
SECOND PART
55h
WRITE
STATUS
?
N
Y
BUS MASTER T_X
TA1 (T7:T0)
BUS MASTER T_X
TA2 (T15:T8)
BUS MASTER T_X
DATA BYTE (D7:D0)
BUS MASTER R_X CRC16
OF COMMAND, ADDRESS,
DATA (1^{ST} PASS)
CRC16 OF ADDRESS, DATA
(SUBSEQUENT PASSES)
LEGEND:
DECISION MADE
BY THE MASTER
DECISION MADE
BY DS2407
CRC
CORRECT
?
N
Y
BUS MASTER T_X
PROGRAM PULSE
DS2407 COPIES
SCRATCHPAD
TO DATA EPROM
BUS MASTER R_X
BYTE FROM EPROM
EPROM BYTE
CORRECT
?
N
Y
END OF
DATA MEMORY
?
Y
N
DS2407 INCREMENTS
ADDRESS COUNTER
DS2407 LOADS NEW
ADDRESS INTO CRC
GENERATOR
ADDRESS
<7
?
N
Y
BUS MASTER T_X
8 READ TIME SLOTS
OR PROGRAM PULSE
DS2407 COPIES
SCRATCHPAD TO
VOLATILE STATUS
BUS MASTER R_X BYTE
FROM VOLATILE
STATUS
BUS MASTER T_X
PROGRAM PULSE
DS2407 COPIES
SCRATCHPAD
TO STATUS EPROM
BUS MASTER R_X
BYTE FROM EPROM
EPROM BYTE
CORRECT
?
N
Y
BUS MASTER
T_X RESET
DS2407 T_X
PRESENCE PULSE
DS2407 INCREMENTS
ADDRESS COUNTER
DS2407 LOADS NEW
ADDRESS INTO CRC
GENERATOR

MEMORY FUNCTION FLOW CHART Figure 6 (cont’d)


FROM FIGURE 6
SECOND PART
AAh
READ STATUS
?
N
Y
BUS MASTER T$_X$
TA1 (T7:T0)
BUS MASTER T$_X$
TA2 (T15:T8)
DS2506 SETS STATUS ADDRESS
= (T15:T0)
BUS MASTER R$_X$ DATA
FROM
STATUS MEMORY
BUS MASTER
T$_X$ RESET
?
Y
N
DS2506 INCREMENTS
ADDRESS COUNTER
END OF
STATUS MEMORY
?
N
Y
BUS MASTER
T$_X$ RESET
?
Y
N
BUS MASTER R$_X$ CRC16
OF COMMAND,
ADDRESS, DATA
BUS MASTER
T$_X$ RESET
?
Y
N
BUS MASTER
R$_X$ 1’S
DS2407 T$_X$
PRESENCE PULSE
F5h
CHANNEL
ACCESS
?
N
Y
BUS MASTER
T$_X$ RESET
DS2407 T$_X$
PRESENCE PULSE
BUS MASTER T$_X$
CONTROL BYTE 1
BUS MASTER T$_X$
CONTROL BYTE 2
BUS MASTER R$_X$
CHANNEL INFO BYTE
BUS MASTER
T$_X$ RESET
?
Y
N
MODE *
?
WRITE
READ
BUS MASTER T$_X$ DATA
TO CHANNEL F/F
*
BUS MASTER R$_X$
DATA FROM PIOs
*
*SEE CHANNEL CONTROL BYTE 1
AND FIGURE 7A.
BUS MASTER
T$_X$ RESET
?
Y
N
CRC
ENABLED *
?
N
Y
CRC
DUE *
?
N
Y
DS2407 INCR. CRC
BYTE COUNTER
BUS MASTER
T$_X$ RESET
?
Y
N
BUS MASTER R$_X$ CRC16 OF
COMMAND, CONTROL, DATA
(1ST PASS)
CRC16 OF DATA
(SUBSEQUENT PASSES)
BUS MASTER
T$_X$ RESET
?
Y
N
DS2407 CLEARS
CRC BYTE COUNTER
R/W TOGGLING
ENABLED *
?
N
Y
DS2407 TOGGLES
READ/WRITE MODE

WRITE MEMORY [0Fh]

The Write Memory command is used to program the 1024–bit EPROM data field. The details of the functional flow chart are described in the section “WRITING EPROM MEMORY”. The data memory address range is 0000h to 007Fh. If the bus master sends a starting address higher than this, the nine most significant address bits are set to zeros by the internal circuitry of the chip. This will result in a mismatch between the CRC calculated by the DS2407 and the CRC calculated by the bus master, indicating an error condition.

WRITE STATUS [55h]

The Write Status command is used to program the Status Memory field, which includes specification of power–on default settings of the Conditional Search and the channel flip–flops as well as dynamic changes of the Conditional Search Settings and channel flip–flops. The details of the functional flow chart are described in the section “WRITING EPROM MEMORY”.

The Status Memory address range is 0000h to 0007h. The general programming algorithm is valid for the EPROM section of the Status Memory (addresses 0 to 6) only. Status Memory Address 7 consists of SRAM cells rather than EPROM. As a consequence, writing to this location does not require a 12V programming pulse and the bits 0 to 6 can be reprogrammed to any value without limitation. Bit 7 is read–only; attempts to write to it are ignored. The function flow for writing to status memory location 7 is basically the same as for the EPROM Status Memory Bytes. However, the programming pulse may be, but need not be, replaced by sending 8 Read Data Time Slots.

READ STATUS [AAh]

The Read Status command is used to read data from the Status Memory field. The functional flow chart of this command is identical to the Read Memory command. Since the Status Memory is only 8 bytes, the DS2407 will send the 16–bit CRC after the last byte of status information has been transmitted.

CHANNEL ACCESS [F5h]

The Channel Access command is used to access the PIO channels to sense the logical status of the output node and the output transistor and to change the status of the output transistor. The bus master will follow the command byte with two Channel Control Bytes and will receive back the Channel Info byte.

The Channel Control bytes allow the master to select a PIO–channel to communicate with, to specify communication parameters and to reset the activity latches. Figure 7 shows the details. The bits CHS0 and CHS1 (Channel Control Byte 1) select the channels to communicate with. One can select one of the two channels or both channels together.

The codes for CHS0 and CHS1 are as follows:

CHS1	CHS0	
0	0	(not allowed)
0	1	channel A only
1	0	channel B only
1	1	both channels interleaved

When reading a single channel only, the logic level at the selected PIO is sampled at the beginning of each read time slot (Figure 9a) and immediately signaled through the 1–Wire line. Because the PIO logic levels are sensed at the beginning of the time slot, transitions at the PIO during the time slot are not seen by the bus master. When writing to a single channel, the selected PIO will show the new status after (but not necessarily immediately after) the 1–Wire line has returned to its idle level of typically 5V (see Figure 9a). If the bus master transmits a 1 (Write One Time Slot), the output transistor of the selected channel will change its status after time td1, which is 15 µs to 60 µs after the begin of the time slot. If the bus master transmits a 0 (Write Zero Time Slot), the output transistor will change its status with a delay of td0 after the 1–Wire line has returned to its idle level. The value of td0 may vary between 200 and 300 ns (see Figure 9a). Depending on the load conditions, there may be additional delay until the voltage at the PIO reaches a new logical level.

If one is communicating with both channels, the Interleave Control Bit IC controls when data is sampled and when data arrives at the PIO pins. There is an asynchronous mode (IC = 0) and a synchronous mode (IC = 1). For the asynchronous mode, both channels are accessed in an alternating way. For the synchronous mode, both channels are accessed simultaneously.

When reading in the asynchronous mode each channel is sampled alternately at the start of each Read Time Slot, beginning with channel A. The logic level detected at the PIO is immediately transmitted to the master during the same time slot. When reading in the synchronous mode, both channels will be sampled at the same time; the data bit from channel A will be sent to the master immediately during the same time slot while the data bit from channel B follows with the next time slot which does not sample the PIOs. Both channels will be sampled again with the time slot that follows the transmission of the data bit from PIO–B (Figure 9b).

When writing in the asynchronous mode, each channel will change its status independently of the other. The change of status occurs with the same timing relations as for communication with one channel. However, every second write time slot addresses the same channel. The first time slot is directed to channel A, the second to channel B, the next to channel A and so on. As a consequence, in asynchronous mode both PIOs can never change their status at the same time. When writing in the synchronous mode, both channels operate together. After the new values for both channels have arrived at the DS2407 the change of status at both channels occurs with the same timing relations as for communication with one channel. As with the asynchronous mode, every second write time slot contains data for the same channel. The first time slot addresses channel A, the second channel B and so on. Depending on the data values, in the synchronous mode both PIOs can change their status at the same time (Figure 9c). In any of these cases, the information of channel A and channel B will appear alternating on the 1–Wire line, always starting with channel A. By varying the idle–time between time slots on the 1–Wire line one has full control over the time points of sampling and the waveforms generated at the PIO–pins when writing to the device.

The TOG bit of Channel Control Byte 1 specifies if one is always reading or writing (TOG = 0) or if one is going to change from reading to writing or vice versa after every data byte that has been sent to or received from the DS2407 (TOG = 1). When accessing one channel, one byte is equivalent to eight reads from or writes to the selected PIO pin. When accessing two channels, one byte is equivalent to four reads or writes from/to each channel.

The initial mode (reading or writing) for accessing the PIO channels is specified in the IM bit. For reading, IM has to be set to 1, for writing IM needs to be 0. If the TOG bit is set to 0, the device will always read or write as specified by the IM bit. If TOG is 1, the device will use the setting of IM for the first byte to be transmitted and will alternate between reading and writing after every byte. Figure 7c illustrates the effect of TOG and IM for one–channel as well as for two–channel operation.

Bit 7 of the Channel Control Byte 1 allows resetting of the activity latch of each channel. The activity latch is set with the first negative or positive edge detected on its associated PIO channel. Both activity latches are cleared simultaneously if bit 7 of the Channel Control Byte 1 is 1. The activity latches are not changed if this bit is 0.

Channel Control Byte 1 also controls the internal CRC generator to safeguard data transmission between the bus master and the DS2407 for channel access. It does not affect reading from or writing to the memory sections of the DS2407. The CRC control bits (bit 0 and bit 1) can be set to create and protect data packets that have the size of 8 bytes or 32 bytes. If desired, the device can safeguard even single bytes by a 16–bit CRC. This setting, however, is recommended only if the data is limited to one byte since it would reduce the sampling rate to one third of the maximum possible value.

The CRC control codes are as follows:

CRC1	CRC0	
0	0	CRC disabled (no CRC at all)
0	1	CRC after every byte
1	0	CRC after 8 bytes (status page size)
1	1	CRC after 32 bytes (data page size)

The CRC provides a high level of data safeguarding and is more efficient for verification than “read after write”. A detailed description of CRCs is found in the “Book of DS19xx iButton Standards”. If the CRC is disabled, the CRC–related sections in the flow chart are skipped.

Channel Control Byte 2 is reserved for future development. The bus master should always send an FFh for the second Channel Control Byte.

The Channel Info byte (Figure 8) which the bus master receives after the Channel Control bytes have been transmitted indicates the status of the channel flip–flops, the PIO pins, the activity latches as well as the availability of channel B and external power supply. Reading 0 for both the channel flip–flop and the sensed level indicates that the output transistor of the PIO is pulling the node low. To be able to read from a PIO channel, the output transistor needs to be non–conducting, which is equivalent to a 1 for the channel flip–flop. Sampling the level of PIO A and B is done at the same time (synchronous) for the Channel Info Byte. If channel B is available, bit 6 of the Channel Info Byte reads 1. For 1–channel versions of the DS2407, the PIO B sensed level, channel flip–flop value, and activity latch value should be ignored. Without an external supply, the supply indication bit (bit 7) reads 0. As long as the voltage applied to the V_{CC} pin is high enough to operate the device this bit will read 1.

CHANNEL CONTROL BYTE 1 Figure 7a

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Activity latch reset	IM	TOG	IC	CHS1	CHS0	CRC1	CRC0

CHANNEL CONTROL BYTE 2 Figure 7b

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
1	1	1	1	1	1	1	1

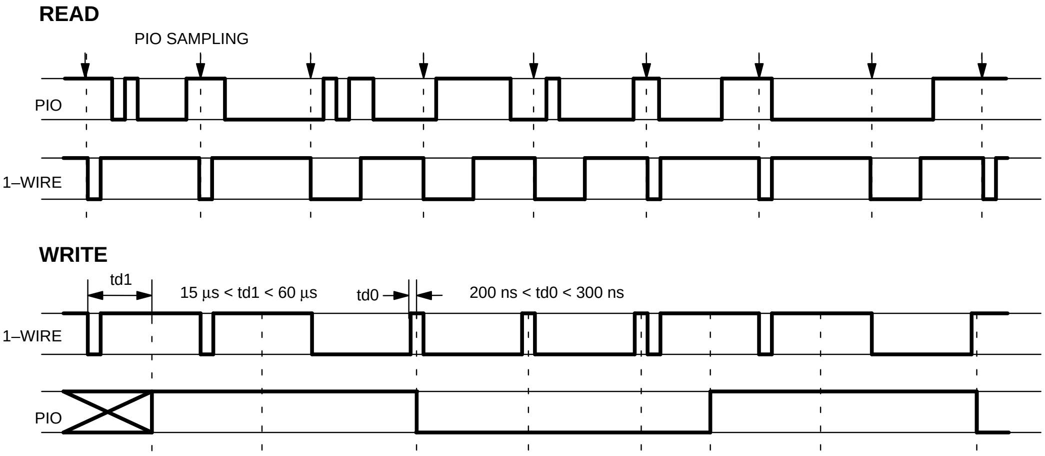
THE EFFECT OF TOGGLE MODE AND INITIAL MODE Figure 7c

TOG	IM	CHANNELS	EFFECT
0	0	one channel	**Write** all bits to the selected channel.
0	1	one channel	**Read** all bits from the selected channel.
1	0	one channel	**Write** eight bits, **read** eight bits, write, read, etc. to/from the selected channel.
1	1	one channel	**Read** eight bits, **write** eight bits, read, write, etc. from/to the selected channel.
0	0	two channels	Repeat: four times (**write** A, **write** b)
0	1	two channels	Repeat: four times (**read** A, **read** B)
1	0	two channels	Four times: (**write** A, **write** B), four times: (**read** A, **read** B), write, read, etc.
1	1	two channels	Four times: (**read** A, **read** B), four times: (**write** A, **write** B), read, write, etc.

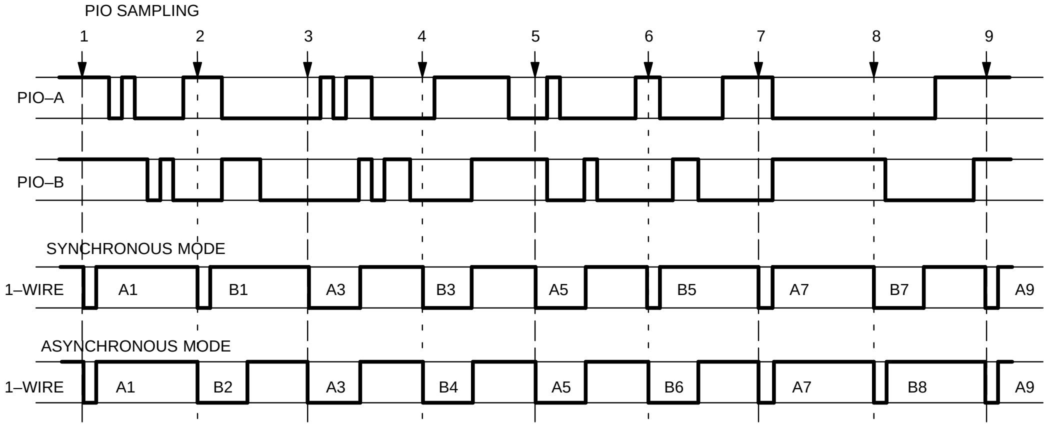
CHANNEL INFO BYTE Figure 8

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Supply Indication 0=no supply	Number of Channels 0=channel A only	PIO–B Activity Latch	PIO–A Activity Latch	PIO–B Sensed Level	PIO–A Sensed Level	PIO–B Channel Flip–Flop Q	PIO–A Channel Flip–Flop Q

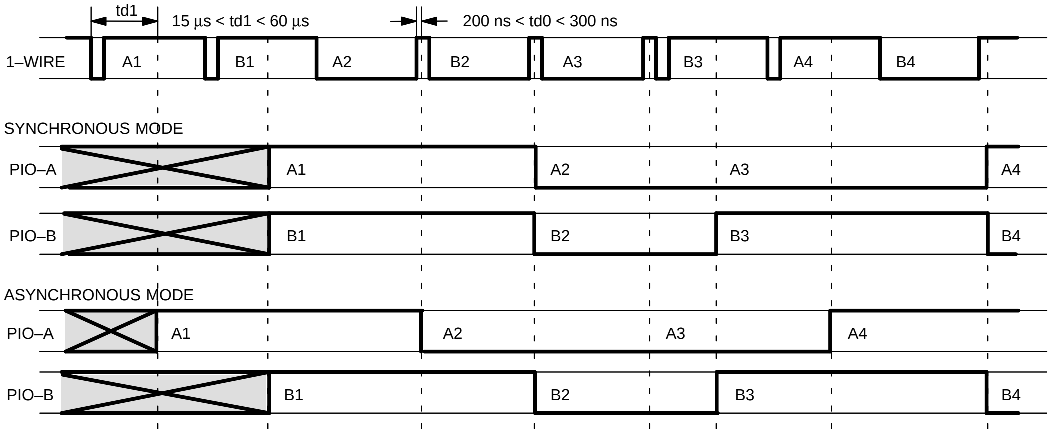
ONE–CHANNEL READ/WRITE Figure 9A


READ
PIO SAMPLING
PIO
1–WIRE
WRITE
td1
15 µs < td1 < 60 µs
td0
200 ns < td0 < 300 ns
1–WIRE
PIO

TWO–CHANNEL READ Figure 9B


PIO SAMPLING
1
2
3
4
5
6
7
8
9
PIO–A
PIO–B
SYNCHRONOUS MODE
1–WIRE
A1
B1
A3
B3
A5
B5
A7
B7
A9
ASYNCHRONOUS MODE
1–WIRE
A1
B2
A3
B4
A5
B6
A7
B8
A9

TWO–CHANNEL WRITE Figure 9C



1–WIRE BUS SYSTEM

The 1–Wire bus is a system which has a single bus master and one or more slaves. In all instances, the DS2407 is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1–Wire signaling (signal type and timing). A 1–Wire protocol defines bus transactions in terms of the bus state during specified time slots that are initiated on the falling edge of sync pulses from the bus master. For a more detailed protocol description, please refer to Chapter 4 of the Book of DS19xx iButton Standards.

HARDWARE CONFIGURATION

The 1–Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1–Wire bus must have an open drain connection or 3–state outputs. The DS2407 is an open drain part with an internal circuit equivalent to that shown in Figure 10. The bus master can be the same equivalent circuit. If a bidirectional pin is not available, separate output and input pins can be tied together.

The bus master requires a pull–up resistor at the master end of the bus, with the bus master circuit equivalent to the one shown in Figures 11a and 11b. The value of the pull–up resistor should be approximately 5kΩ for short line lengths. The interface between bus master and 1–Wire bus may be reduced to a single pull–up resistor (open drain master) or two resistors plus transistor (TTL–type master) if the EPROM section of the DS2407 is already programmed before the final installation.

A multidrop bus consists of a 1–Wire bus with multiple slaves attached. The 1–Wire bus has a maximum data rate of 16.3k bits per second. If the bus master is also required to perform programming of the EPROM portions of the DS2407, a programming supply capable of delivering up to 10 milliamps at 12 volts for 480 µs is required. Non–EPROM devices cannot be present during programming. The idle state for the 1–Wire bus is high. If, for any reason, a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 120 µs, one or more of the devices on the bus may be reset. If the 1–Wire bus remains low for more than 5 ms and the DS2407 is not powered externally it may lose its current status and switch off both PIOs.

TRANSACTION SEQUENCE

The sequence for accessing the DS2407 via the 1–Wire port is as follows:

- Initialization
- ROM Function Command
- Memory Function Command
- Read Memory/Write Memory or Channel Access

INITIALIZATION

All transactions on the 1–Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by a presence pulse(s) transmitted by the slave(s).

The presence pulse lets the bus master know that the DS2407 is on the bus and is ready to operate. For more details, see the “1–Wire Signaling” section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the five ROM function commands. All ROM function commands are eight bits long. A list of these commands follows (refer to flowchart in Figure 12):

Read ROM [33h]

This command allows the bus master to read the DS2407’s 8–bit family code, unique 48–bit serial number, and 8–bit CRC. This command can be used only if there is a single DS2407 on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired–AND result).

Match ROM [55h]

The match ROM command, followed by a 64–bit ROM sequence, allows the bus master to address a specific DS2407 on a multidrop bus. Only the DS2407 that exactly matches the 64–bit ROM sequence will respond to the subsequent memory function command. All slaves that do not match the 64–bit ROM sequence will wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

Skip ROM [CCh]

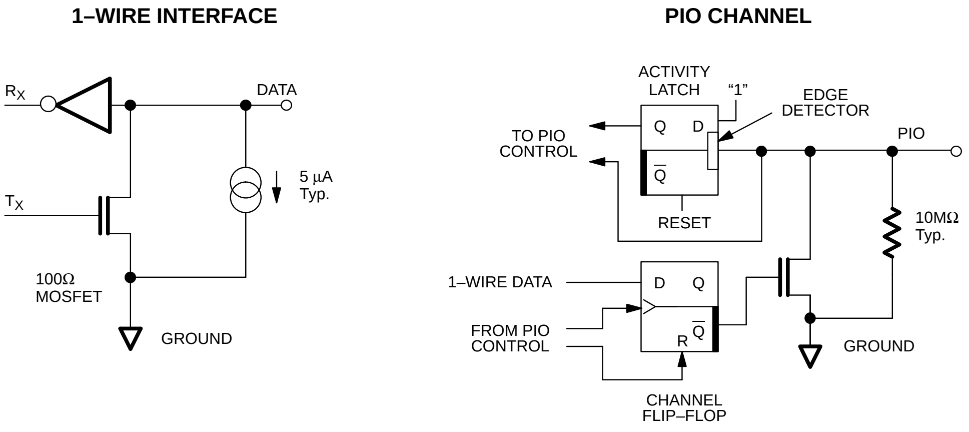
This command can save time in a single drop bus system by allowing the bus master to access the memory functions without providing the 64–bit ROM code. If more than one slave is present on the bus and a read command is issued following the Skip ROM command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pull–downs will produce a wired–AND result).

Search ROM [F0h]

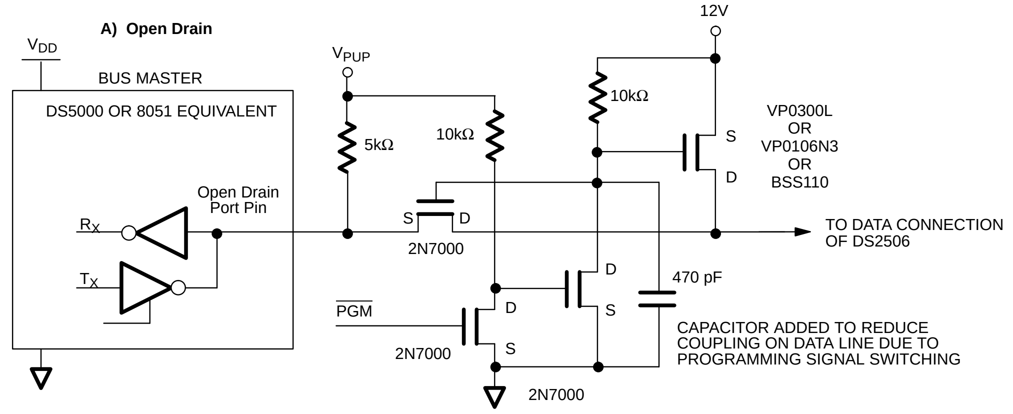
When a system is initially interrogated, the bus master may not know the number of devices on the 1–Wire bus or their 64–bit ROM codes. The Search ROM command allows the bus master to use a process of elimination to identify the 64–bit ROM codes of all slave devices on the bus. This process of elimination involves repeated application of a simple three–step procedure where the bus master starts by reading a bit position in the 64–bit ROM, followed by reading the complement of that bit position, and finally writing to all the devices still involved in the search the desired logic value for that bit position. A detailed example and a flowchart for the search algorithm can be found in the “Book of DS19xx iButton Standards.”

After one complete pass, the bus master knows the contents of the 64–bit ROM in one device. Subsequent passes will reveal the total number of devices and their individual ROM codes. In addition, after each complete pass of the search that successfully determines the 64–bit ROM for a specific device on the multidrop bus, that particular device can be individually accessed as if a Match ROM had been issued since all other devices will have dropped out of the search process and are waiting for a reset pulse.

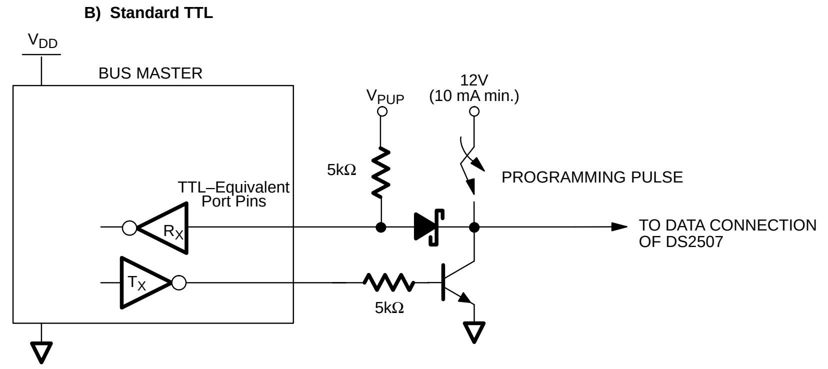
DS2407 EQUIVALENT CIRCUIT Figure 10


1–WIRE INTERFACE
PIO CHANNEL
RX
DATA
5 µA
Typ.
TX
100Ω
MOSFET
GROUND
ACTIVITY
LATCH
"1"
EDGE
DETECTOR
TO PIO
CONTROL
Q
D
Q
PIO
RESET
10MΩ
Typ.
1–WIRE DATA
D
Q
FROM PIO
CONTROL
R
Q
GROUND
CHANNEL
FLIP–FLOP

BUS MASTER CIRCUIT Figure 11

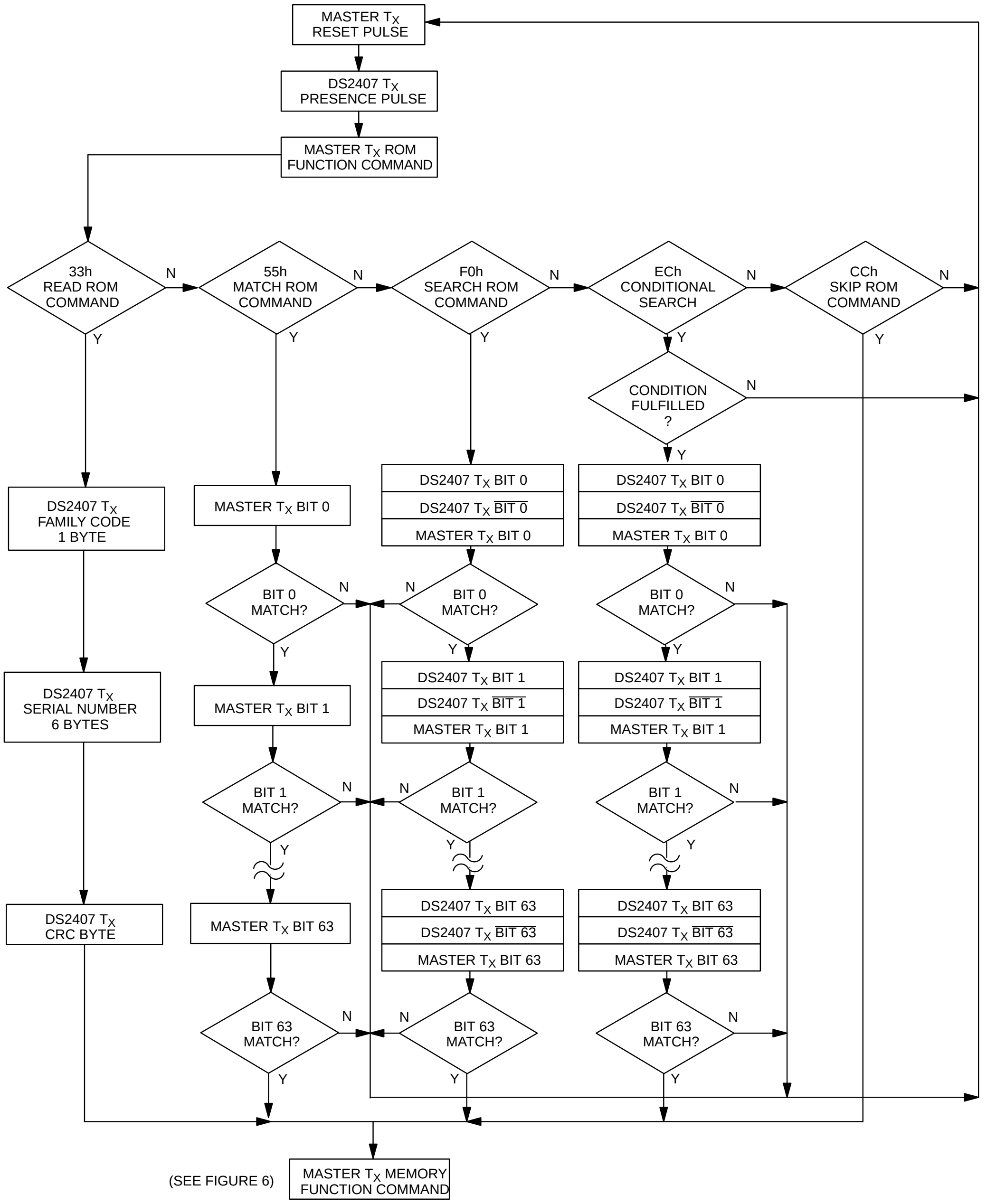

A) Open Drain
VDD
BUS MASTER
DS5000 OR 8051 EQUIVALENT
Open Drain
Port Pin
RX
TX
VPUP
5kΩ
10kΩ
S
D
2N7000
PGM
D
S
2N7000
12V
10kΩ
VP0300L
OR
VP0106N3
OR
BSS110
S
D
TO DATA CONNECTION
OF DS2506
D
S
470 pF
CAPACITOR ADDED TO REDUCE
COUPLING ON DATA LINE DUE TO
PROGRAMMING SIGNAL SWITCHING
2N7000

The interface is reduced to the 5kΩ pull–up resistor if one does not intend to program the EPROM cells.


B) Standard TTL
VDD
BUS MASTER
TTL–Equivalent
Port Pins
RX
TX
VPUP
5kΩ
12V
(10 mA min.)
PROGRAMMING PULSE
TO DATA CONNECTION
OF DS2507
5kΩ

The diode and Programming Pulse circuit are not required if one does not intend to program the EPROM cells.

ROM FUNCTIONS FLOW CHART Figure 12


MASTER T_X RESET PULSE
DS2407 T_X PRESENCE PULSE
MASTER T_X ROM FUNCTION COMMAND
33h READ ROM COMMAND
55h MATCH ROM COMMAND
F0h SEARCH ROM COMMAND
ECh CONDITIONAL SEARCH
CCh SKIP ROM COMMAND
CONDITION FULFILLED ?
DS2407 T_X FAMILY CODE 1 BYTE
DS2407 T_X SERIAL NUMBER 6 BYTES
DS2407 T_X CRC BYTE
MASTER T_X BIT 0
MASTER T_X BIT 1
MASTER T_X BIT 63
DS2407 T_X BIT 0
DS2407 T_X $\overline{\text{BIT 0}}$
DS2407 T_X BIT 1
DS2407 T_X $\overline{\text{BIT 1}}$
DS2407 T_X BIT 63
DS2407 T_X $\overline{\text{BIT 63}}$
BIT 0 MATCH?
BIT 1 MATCH?
BIT 63 MATCH?
Y
N
(SEE FIGURE 6)
MASTER T_X MEMORY FUNCTION COMMAND

Conditional Search ROM [ECh]

The Conditional Search ROM command operates similarly to the Search ROM command except that only devices fulfilling the specified condition will participate in the search. The condition is specified by the bit functions CSS0 to CSS4 in Status Memory location 7. The power–on default settings of these bits are stored in EPROM in Status Memory location 6. If this EPROM byte is not programmed, all CSS bits will be 1s. The Conditional Search ROM provides an efficient means for the bus master to determine devices in a multidrop system that have to signal a status change, e.g. the opening of a window in a building control application. After each pass of the Conditional Search that successfully determined the 64–bit ROM for a specific device on the multidrop bus, that particular device can be individually accessed as if a Match ROM had been issued since all other devices will have dropped out of the search process and are waiting for a reset pulse.

For the conditional search, one can specify the polarity (HIGH or LOW; CSS0), the source (PIO–pin, channel flip flop or activity latch; CSS1, CSS2) and the channel of interest (A, B or the logical OR of A, B; CSS3, CSS4). Figure 13 shows a table of all qualifying conditions and the required settings for CSS0 to CSS4.

The activity latch (Figure 10) captures an event for interrogation by the bus master at a later time. In this way, the bus master needs not to poll devices continuously. The activity latch is cleared to 0 when the device powers up and is set to 1 with the first negative or positive edge detected on the associated PIO channel. The activity latch can also be cleared by writing a 1 into bit 7 of the Channel Control Byte 1. When using the activity latch the output transistor of the selected channel should be non–conducting. Otherwise signals applied to the PIO pin will be shorted to ground by the low impedance of the output transistor.

The channel of interest is specified by the Channel Select bits CSS3 and CSS4. The sampling of the source within the selected channel will take place on completion of the Conditional Search command byte. The Channel selection codes are as follows:

CSS4,	CSS3	Channel Selection
0	0	neither channel selected
0	1	channel A only
1	0	channel B only
1	1	channel A OR channel B

If both CSS3 and CSS4 are 1, the logical values of the selected signal source of both channels are ORed and the result is compared to specified polarity. If, for example, the specified polarity is 0, the signal source of both channels must be 0 to allow the device to respond to the Conditional Search. If both CSS3 and CSS4 are 0 neither channel is selected. Under this condition the device will always respond to the Conditional Search if the polarity bit CSS0 is 0, disregarding the status of the selected source. If neither channel is selected and CSS0 = 1, the device will ignore the Conditional Search but will respond to the regular Search ROM command.

The source selection for the Conditional Search is done through the Source Select bits CSS1 and CSS2. The codes for these bits are as follows:

CSS2,	CSS1	Source Selection
0	0	Hidden Mode
0	1	Activity Latch
1	0	channel flip flop
1	1	PIO Status

Setting both CSS1 and CSS2 to 0 will put the device into a “Hidden Mode” where it keeps its status but only responds to the Match ROM (always) and Conditional Search command (only if the polarity bit CSS0 is set to 1). While in “Hidden Mode” the device will never give a Presence Pulse. When powering up into the “Hidden Mode”, i.e., when bits 1 and 2 of status byte 6 have been programmed to 0, the device will give one Presence Pulse for every power–up sequence. If the device is in Hidden Mode and the polarity bit is set to 0, the device will not participate in the Conditional Search. As long as the device is not programmed to power–up into “Hidden Mode” the “Hidden Mode” can always be ended by a power–on reset. Otherwise the only way to get the device out of “Hidden Mode” is by remembering and matching its 64–bit registration number and setting CSS1 or CSS2 to 1.

The Conditional Search Polarity is specified by CSS0. If CSS0 is 0, the DS2407 will respond to a Conditional Search command if the status of the selected source for the specified channel is a logic 0. If CSS0 is set to 1, the source level needs to be a logic 1.

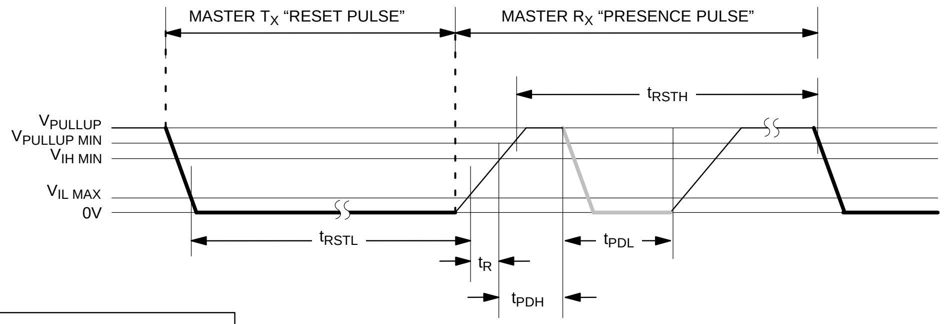
For 1–channel versions of the DS2407 the channel B input will always be a logic 0 level. CSS4 should not be set to 1 therefore to avoid unwanted influence from channel B. The bus master can determine the availability of channel B from bit 6 of the Channel Info byte.

The power–on default settings for the conditional search become valid after the device has received any ROM function command byte, even an invalid one, and can be modified by writing to the appropriate Status Memory location. As long as the device remains powered up, the modified search conditions are available for use at any time.

QUALIFYING CONDITIONS FOR CONDITIONAL SEARCH Figure 13

DESCRIPTION		CONDITIONAL SEARCH SELECT CODE				
		CHANNEL SELECT		SOURCE SELECT		POLARITY
CONDITION	CHANNEL	CSS4	CSS3	CSS2	CSS1	CSS0
Hidden Mode	neither one	don’t care		0	0	1
Unconditional	neither one	0	0	at least one of these bits needs to be 1		0
Activity Latch = 0	A	0	1	0	1	0
Activity Latch = 1	A	0	1	0	1	1
Channel FF = 0 (transistor on)	A	0	1	1	0	0
Channel FF = 1 (transistor off)	A	0	1	1	0	1
PIO Low	A	0	1	1	1	0
PIO High	A	0	1	1	1	1
Activity Latch = 0	B	1	0	0	1	0
Activity Latch = 1	B	1	0	0	1	1
Channel FF = 0 (transistor on)	B	1	0	1	0	0
Channel FF = 1 (transistor off)	B	1	0	1	0	1
PIO Low	B	1	0	1	1	0
PIO High	B	1	0	1	1	1
Activity Latch = 0	A or B	1	1	0	1	0
Activity Latch = 1	A or B	1	1	0	1	1
Channel FF = 0 (transistor on)	A or B	1	1	1	0	0
Channel FF = 1 (transistor off)	A or B	1	1	1	0	1
PIO Low	A or B	1	1	1	1	0
PIO High	A or B	1	1	1	1	1

INITIALIZATION PROCEDURE “RESET AND PRESENCE PULSES” Figure 14

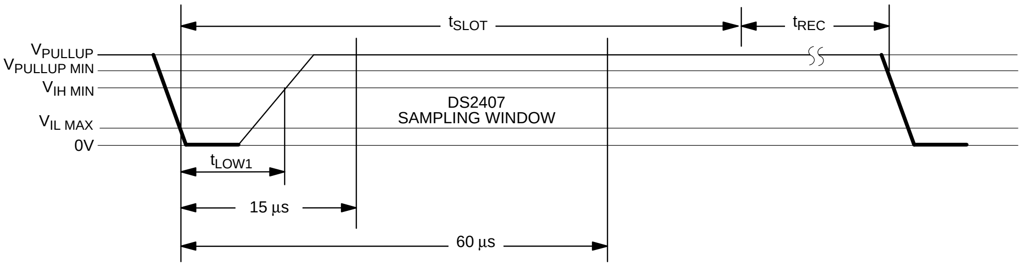

MASTER T_X “RESET PULSE”
MASTER R_X “PRESENCE PULSE”
t_RSTH
V_PULLUP
V_PULLUP MIN
V_IH MIN
V_IL MAX
0V
t_RSTL
t_R
t_PDL
t_PDH
RESISTOR
MASTER
DS2407

$480\ \mu s \le t_{RSTL} < \infty$ *
$480\ \mu s \le t_{RSTH} < \infty$ (includes recovery time)
$15\ \mu s \le t_{PDH} < 60\ \mu s$
$60\ \mu s \le t_{PDL} < 240\ \mu s$

* In order not to mask interrupt signalling by other devices on the 1–Wire bus, $t_{RSTL} + t_R$ should always be less than 960 µs. t_{RSTL} should be limited to maximum 5 ms. Otherwise the DS2407 may perform a power–on reset cycle.

READ/WRITE TIMING DIAGRAM Figure 15

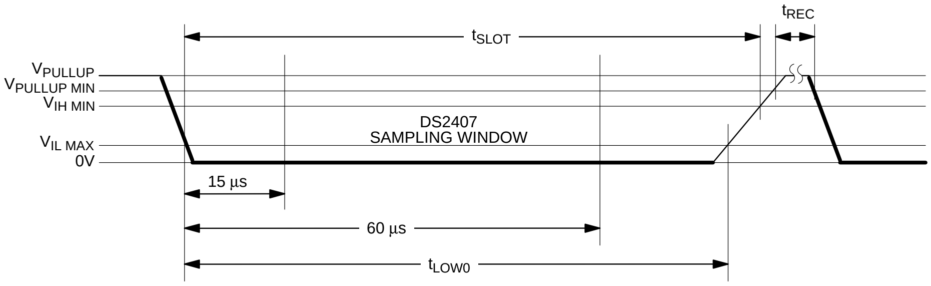
Write–one Time Slot


t_SLOT
t_REC
V_PULLUP
V_PULLUP MIN
V_IH MIN
V_IL MAX
0V
DS2407
SAMPLING WINDOW
t_LOW1
15 µs
60 µs
RESISTOR
MASTER
DS2407

$60\ \mu s \le t_{SLOT} < 120\ \mu s$
$1\ \mu s \le t_{LOW1} < 15\ \mu s$
$1\ \mu s \le t_{REC} < \infty$

READ/WRITE TIMING DIAGRAM Figure 15 (cont'd)

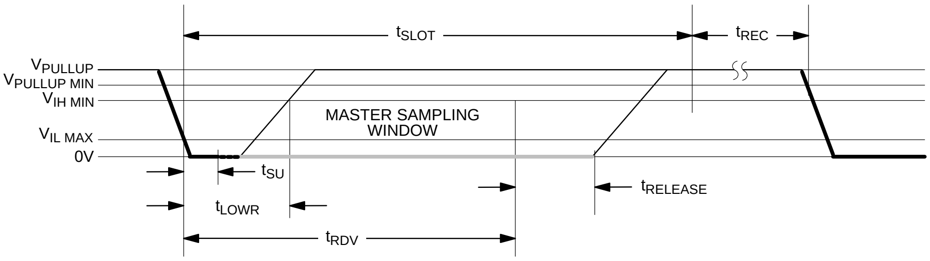
Write–zero Time Slot

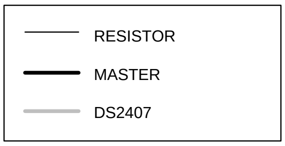

t_{REC}
t_{SLOT}
V_{PULLUP}
$V_{PULLUP\ MIN}$
$V_{IH\ MIN}$
$V_{IL\ MAX}$
0V
DS2407
SAMPLING WINDOW
15 µs
60 µs
t_{LOW0}

$60\ \mu s \leq t_{LOW0} < t_{SLOT} < 120\ \mu s$

$1\ \mu s \leq t_{REC} < \infty$

Read–data Time Slot


t_{SLOT}
t_{REC}
V_{PULLUP}
$V_{PULLUP\ MIN}$
$V_{IH\ MIN}$
$V_{IL\ MAX}$
0V
MASTER SAMPLING
WINDOW
t_{SU}
t_{LOWR}
$t_{RELEASE}$
t_{RDV}


RESISTOR
MASTER
DS2407

$60\ \mu s \leq t_{SLOT} < 120\ \mu s$

$1\ \mu s \leq t_{LOWR} < 15\ \mu s$

$0 \leq t_{RELEASE} < 45\ \mu s$

$1\ \mu s \leq t_{REC} < \infty$

$t_{RDV} = 15\ \mu s$

$t_{SU} < 1\ \mu s$

1–WIRE SIGNALING

The DS2407 requires strict protocols to insure data integrity. The protocol consists of five types of signaling on one line: Reset Sequence with Reset Pulse and Presence Pulse, Write 0, Write 1, Read Data and Program Pulse. All these signals except presence pulse are initiated by the bus master. The initialization sequence required to begin any communication with the DS2407 is shown in Figure 14. A reset pulse followed by a presence pulse indicates the DS2407 is ready to accept a ROM command. The bus master transmits (TX) a reset pulse (t_{RSTL}, minimum 480 µs). The bus master then releases the line and goes into receive mode (RX). The 1–Wire bus is pulled to a high state via the pull–up resistor. After detecting the rising edge on the data pin, the DS2407 waits (t_{PDH}, 15–60 µs) and then transmits the presence pulse (t_{PDL}, 60–240 µs). If the device is programmed to power–up into the “Hidden Mode”, the presence pulse will be observed only once during the power–up phase. With every subsequent reset pulse no presence pulse will be transmitted.

READ/WRITE TIME SLOTS

The definitions of write and read time slots are illustrated in Figure 15. All time slots are initiated by the master driving the data line low. The falling edge of the data line synchronizes the DS2407 to the master by triggering a delay circuit in the DS2407. During write time slots, the delay circuit determines when the DS2407 will sample the data line. For a read data time slot, if a "0" is to be transmitted, the delay circuit determines how long the DS2407 will hold the data line low overriding the 1 generated by the master. If the data bit is an "1", the device will leave the read data time slot unchanged.

PROGRAM PULSE

To copy data from the 8–bit scratchpad to the EPROM Data or Status Memory, a program pulse of 12 volts is applied to the data line after the bus master has confirmed that the CRC for the current byte is correct. During programming, the bus master controls the transition from a state where the data line is idling high via the pull–up resistor to a state where the data line is actively driven to a programming voltage of 12 volts providing a minimum of 10 mA of current to the DS2407. This programming voltage (Figure 16) should be applied for 480 µs, after which the bus master should return the data line to an idle high state controlled by the pull–up resistor. Note that due to the high voltage programming requirements for any 1–Wire EPROM device, it is not possible to multi–drop non–EPROM based 1–Wire devices (e.g. DS1990A, DS1992) with the DS2407 during programming. An internal diode within the non–EPROM based 1–Wire devices will attempt to clamp the data line at approximately 8 volts and could potentially damage these DS199x devices.

CRC GENERATION

With the DS2407 there are two different types of CRCs (Cyclic Redundancy Checks). One CRC is an 8–bit type and is stored in the most significant byte of the 64–bit ROM. The bus master can compute a CRC value from the first 56 bits of the 64–bit ROM and compare it to the value stored within the DS2407 to determine if the ROM data has been received error–free by the bus master. The equivalent polynomial function of this CRC is: $X^8 + X^5 + X^4 + 1$. This 8–bit CRC is received in the true (non–inverted) form when reading the ROM of the DS2407. It is computed at the factory and lasered into the ROM.

The other CRC is a 16–bit type, generated according to the standardized CRC16–polynomial function $X^{16} + X^{15} + X^2 + 1$. This CRC is used for error detection when reading Data Memory, Status Memory or when communicating with PIO channels. It is the same type of CRC as is used with NVRAM based iButtons for error detection within the iButton Extended File Structure. In contrast to the 8–bit CRC, the 16–bit CRC is always returned in the complemented (inverted) form. A CRC–generator inside the DS2407 chip (Figure 17) will calculate a new 16–bit CRC at every situation shown in the command flow chart of Figure 6.

The DS2407 provides this CRC–value to the bus master to validate the transfer of command, address, and data to and from the bus master. When reading the data memory of the DS2407 with the Read Memory command, the 16–bit CRC is only transmitted at the end of the memory. This CRC is generated by clearing the CRC generator, shifting in the command, low address, high address and every data byte starting at the first addressed memory location and continuing until the end of the implemented data memory is reached.

When reading the Status Memory with the Read Status command, the 16–bit CRC is transmitted at the end of the 8 byte page of the Status Memory. The 16–bit CRC will be generated by clearing the CRC generator, shifting in the command byte, low address, high address and the data bytes beginning at the first addressed memory location and continuing until the last byte of the EPROM Status Memory is reached.

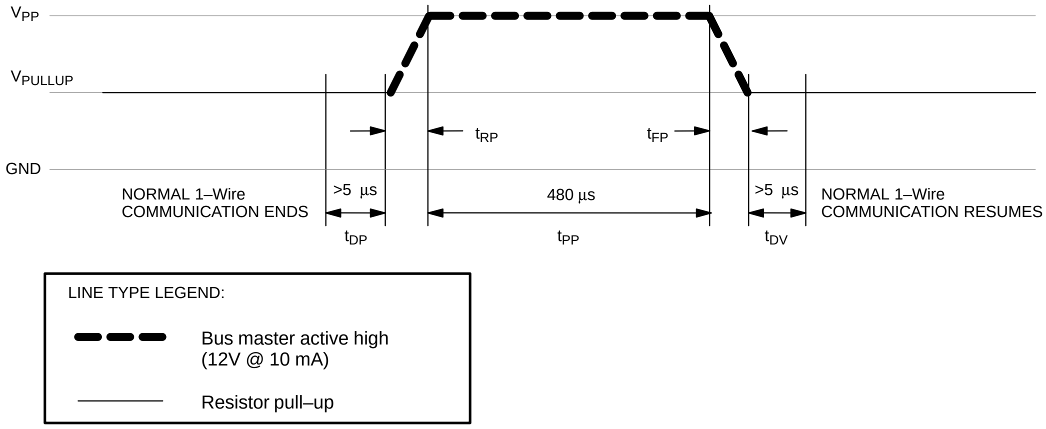
When reading the data memory of the DS2407 with the Extended Read Memory command, there are two situations where a 16–bit CRC is transmitted. One 16–bit CRC follows each Redirection Byte, another 16–bit CRC is received after the last byte of a memory data page is read. The CRC at the end of the memory page is always the result of clearing the CRC generator and shifting in the data bytes beginning at the first addressed memory location of the EPROM data page until the last byte of this page. With the initial pass through the Extended Read Memory flow chart the 16–bit CRC value is the result of shifting the command byte into the cleared CRC generator, followed by the two address bytes and the Redirection Byte. Subsequent passes through the Extended Read Memory flow chart will generate a 16–bit CRC that is the result of clearing the CRC generator and then shifting in only the Redirection Byte.

When writing to the DS2407 (either data memory or Status Memory), the bus master receives a 16–bit CRC to verify that the data transfer was correct before applying the programming pulse. With the initial pass through the Write Memory/Status flow chart the 16–bit CRC will be generated by clearing the CRC–generator, shifting in the command, low address, high address and the data byte. Subsequent passes through the Write Memory/Status flow chart due to the DS2407 automatically incrementing its address counter will generate a 16–bit CRC that is the result of loading (not shifting) the new (incremented) address into the CRC generator and then shifting in the new data byte.

When communicating with a PIO channel using the Channel Access command, one can select if and how often a 16–bit CRC will be added to the data stream. This CRC selection is specified in the Channel Control byte 1 and may be different every time the Channel Access command is issued by the bus master. Depending on the CRC selection, the device can generate a CRC after every byte that follows the Channel Info byte, after each block of eight bytes or after each block of 32 bytes. If the CRC is enabled, with the initial pass through the Channel Access flow chart the 16–bit CRC will be generated by clearing the CRC–generator, shifting in the command, Channel Control Bytes 1 and 2, Channel Info Byte and the specified amount of data bytes (1, 8 or 32). Subsequent passes through the Channel Access flow chart will generate a 16–bit CRC that is the result of clearing the CRC generator and then shifting in the new data bytes. This algorithm is valid for all accesses to the PIO channels, continuous reading or writing as well as toggling between read and write.

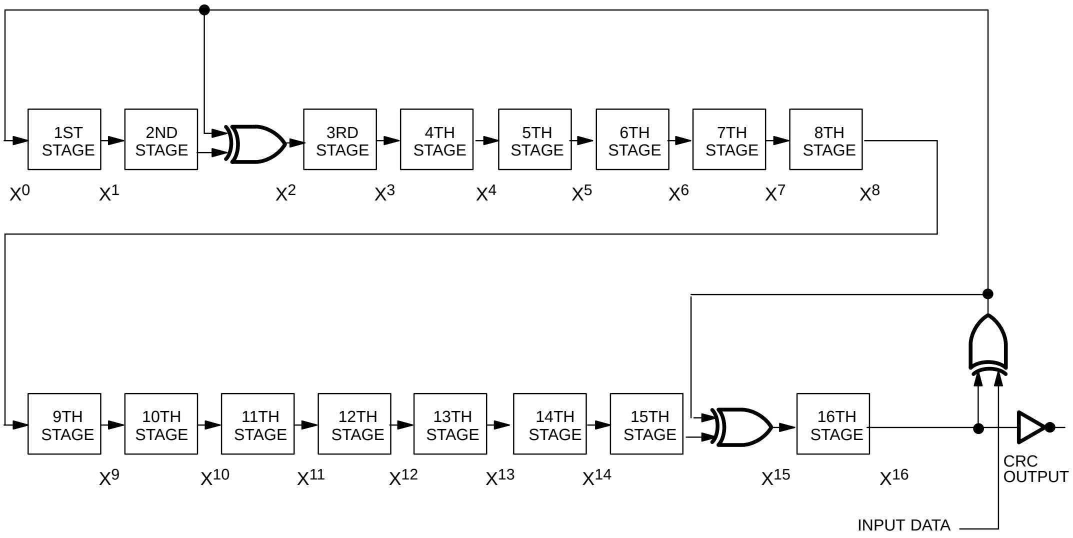
The comparison of CRC values and decision to continue with an operation are determined entirely by the bus master. There is no circuitry on the DS2407 that prevents a command sequence from proceeding if the CRC stored in or calculated by the DS2407 does not match the value generated by the bus master. For more details on generating CRC values including example implementations in both hardware and software, see the “Book of DS19xx iButton Standards”.

PROGRAM PULSE TIMING DIAGRAM Figure 16



CRC–16 HARDWARE DESCRIPTION AND POLYNOMIAL Figure 17

POLYNOMIAL = $X^{16} + X^{15} + X^2 + 1$


1ST STAGE
2ND STAGE
3RD STAGE
4TH STAGE
5TH STAGE
6TH STAGE
7TH STAGE
8TH STAGE
X0
X1
X2
X3
X4
X5
X6
X7
X8
9TH STAGE
10TH STAGE
11TH STAGE
12TH STAGE
13TH STAGE
14TH STAGE
15TH STAGE
16TH STAGE
X9
X10
X11
X12
X13
X14
X15
X16
CRC OUTPUT
INPUT DATA

ABSOLUTE MAXIMUM RATINGS*

Voltage on DATA or PIO–A to Ground	–0.5V to +13.0V
Voltage on V_{CC} or PIO–B to Ground	–0.5V to +6.5V
Operating Temperature	–40°C to +85°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS DATA PIN

(V_{PUP}=2.8V to 6.0V; –40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.2			V	1, 6
Logic 0	V_{IL}	–0.3		+0.8	V	1, 13
Output Logic Low @ 4 mA	V_{OL}			0.4	V	1
Output Logic High	V_{OH}		V_{PUP}	6.0	V	1, 2
Input Load Current	I_L		5		µA	3, 14
Programming Voltage @ 10 mA	V_{PP}	11.5		12.0	V	

DC ELECTRICAL CHARACTERISTICS PIO PINS

(V_{PUP}=2.8V to 6.0V; –40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1 (A)	V_{IHA}	2.2		12	V	1, 6, 16
Logic 0 (A)	V_{ILA}	–0.3		+0.6	V	1
Output Sink Current @ 0.4V (A)	I_{SA}	See graph on page 31				11, 12, 15
Output Logic High (A)	V_{OHA}		V_{PUPA}	12.0	V	1, 2
Logic 1 (B)	V_{IHB}	2.2		6	V	1, 6, 16
Logic 0 (B)	V_{ILB}	–0.3		+0.4	V	1
Output Sink Current @ 0.4V (B)	I_{SB}	See graph on page 31				
Output Logic High (B)	V_{OHB}		V_{PUPB}	6.0	V	1, 2
Input Resistance	R_I	7	10	13	MΩ	9

DC ELECTRICAL CHARACTERISTICS V_{CC}

(V_{PUP}=2.8V to 6.0V; –40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IHC}	2.8		6	V	1, 10
Logic 0	V_{ILC}	–0.3		+0.8	V	1
Input Current	I_{CC}			4.0	µA	3

CAPACITANCE

(t_A=25°C)

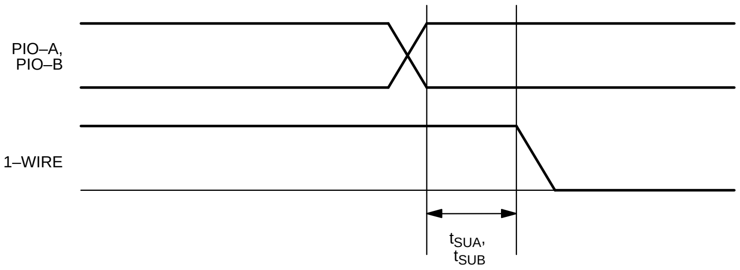
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Capacitance DATA Pin	C_D			800	pF	7
Capacitance PIO–A Pin	C_A		100		pF	
Capacitance PIO–B Pin	C_B		25		pF	
Capacitance V_{CC} Pin	C_C		10		pF	

AC ELECTRICAL CHARACTERISTICS

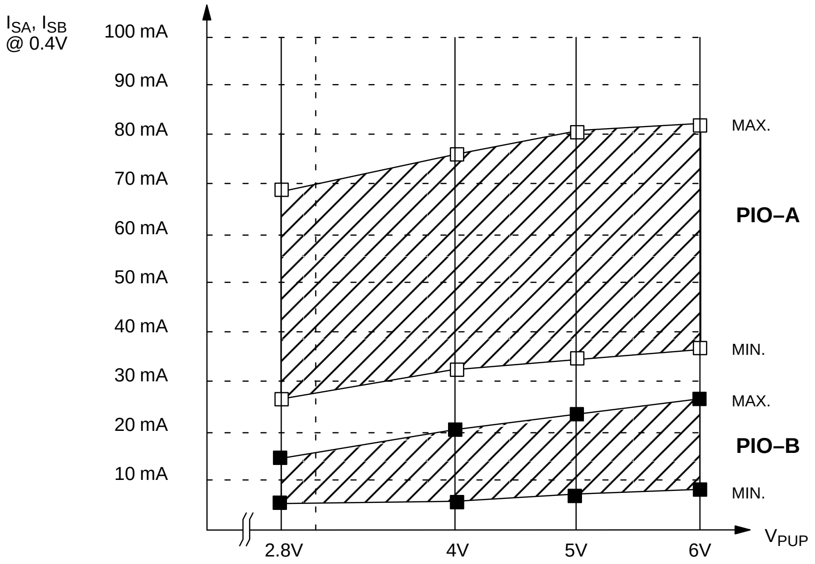
(V_{PUP}=2.8V to 6.0V; –40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	
Write 0 Low Time	t_{LOW0}	60		120	µs	
Read Data Valid	t_{RDV}	exactly 15			µs	
Release Time	$t_{RELEASE}$	0	15	45	µs	
Read Data Setup DATA	t_{SU}			1	µs	5
Recovery Time	t_{REC}	1			µs	
Reset Time High	t_{RSTH}	480			µs	4
Reset Time Low	t_{RSTL}	480		5000	µs	8
Presence Detect High	t_{PDHIGH}	15		60	µs	
Presence Detect Low	t_{PDLOW}	60		240	µs	
Read Data Setup PIO–A	t_{SUA}	500			ns	
Read Data Setup PIO–B	t_{SUB}	500			ns	
Delay to Program	t_{DP}	5			µs	
Delay to Verify	t_{DV}	5			µs	
Program Pulse Width	t_{PP}	480			µs	
Program Voltage Rise Time	t_{RP}	0.5		5.0	µs	
Program Voltage Fall Time	t_{FP}	0.5		5.0	µs	

DEFINITION OF PIO READ DATA SETUP TIME



PIO SINK CURRENT



NOTES:

1. All voltages are referenced to ground.
2. V_{PUP}, V_{PUPA}, V_{PUPB} = external pull–up voltage.
3. Input load is to ground.
4. An additional reset or communication sequence cannot begin until the reset high time has expired.
5. Read data setup time refers to the time the host must pull the 1–Wire bus low to read a bit. Data is guaranteed to be valid within 1 µs of this falling edge and will remain valid for 14 µs minimum (15 µs total from falling edge on 1–Wire bus).
6. V_{IH} is a function of the chip–internal supply voltage. This voltage is determined by either the external pull–up resistor and V_{PUP} or the V_{CC} supply, whichever is higher.
7. Capacitance on the data pin could be 800 pF when power is first applied. If a 5kΩ resistor is used to pull up the data line to V_{PUP}, 5 µs after power has been applied the parasite capacitance will not affect normal communications.
8. t_{RSTL} should be limited to maximum 5 ms. Otherwise the DS2407 may perform a power–on reset.
9. Input resistance is to ground.
10. V_{CC} must be at least 4.0V if it is to be connected during a programming pulse.
11. If the current at PIO–A reaches 200 mA the gate voltage of the output transistor will be reduced to limit the sink current to 200 mA. The user–supplied circuitry should limit the current flow through the PIO–transistor to no more than 100 mA. Otherwise the DS2407 may be damaged.
12. PIO–A has a controlled turn–on output. The indicated currents are DC values. At V_{PUP} = 4.0V or higher the sink current typically reaches 80% of its DC value 1 µs after turning on the transistor.
13. Under certain low voltage conditions V_{ILMAX} may have to be reduced to as much as 0.5V to always guarantee a presence pulse.
14. The input load current may be as high as 100 µA after a power–on reset until a memory function command byte has been sent as well as during the execution of a ROM function command.
15. If the device is disconnected from the 1–Wire bus (data pin floating) channel A may lose its output status even if V_{CC} is connected. A resistor of approximately 100 kΩ between V_{CC} and data will maintain the status of channel A.
16. Without V_{CC} supply, V_{IH} for either PIO pin should always be greater than or equal to V_{PUP} –0.3V.