

# DSP56004 DSP56004ROM

## SYMPHONY™ AUDIO DSP FAMILY 24-BIT DIGITAL SIGNAL PROCESSORS

Motorola designed the Symphony™ family of high-performance, programmable Digital Signal Processors (DSPs) to support a variety of digital audio applications, including Dolby ProLogic, ATRAC, and Lucasfilm Home THX processing. Software for these applications is licensed by Motorola for integration into products like audio/video receivers, televisions, and automotive sound systems with such user-developed features as digital equalization and sound field processing. The DSP56004 is an MPU-style general purpose DSP, composed of an efficient 24-bit Digital Signal Processor core, program and data memories, various peripherals optimized for audio, and support circuitry. As illustrated in **Figure 1**, the DSP56000 core family compatible DSP is fed by program memory, two independent data RAMs and two data ROMs, a Serial Audio Interface (SAI), Serial Host Interface (SHI), External Memory Interface (EMI), dedicated I/O lines, on-chip Phase Lock Loop (PLL), and On-Chip Emulation (OnCE™) port.

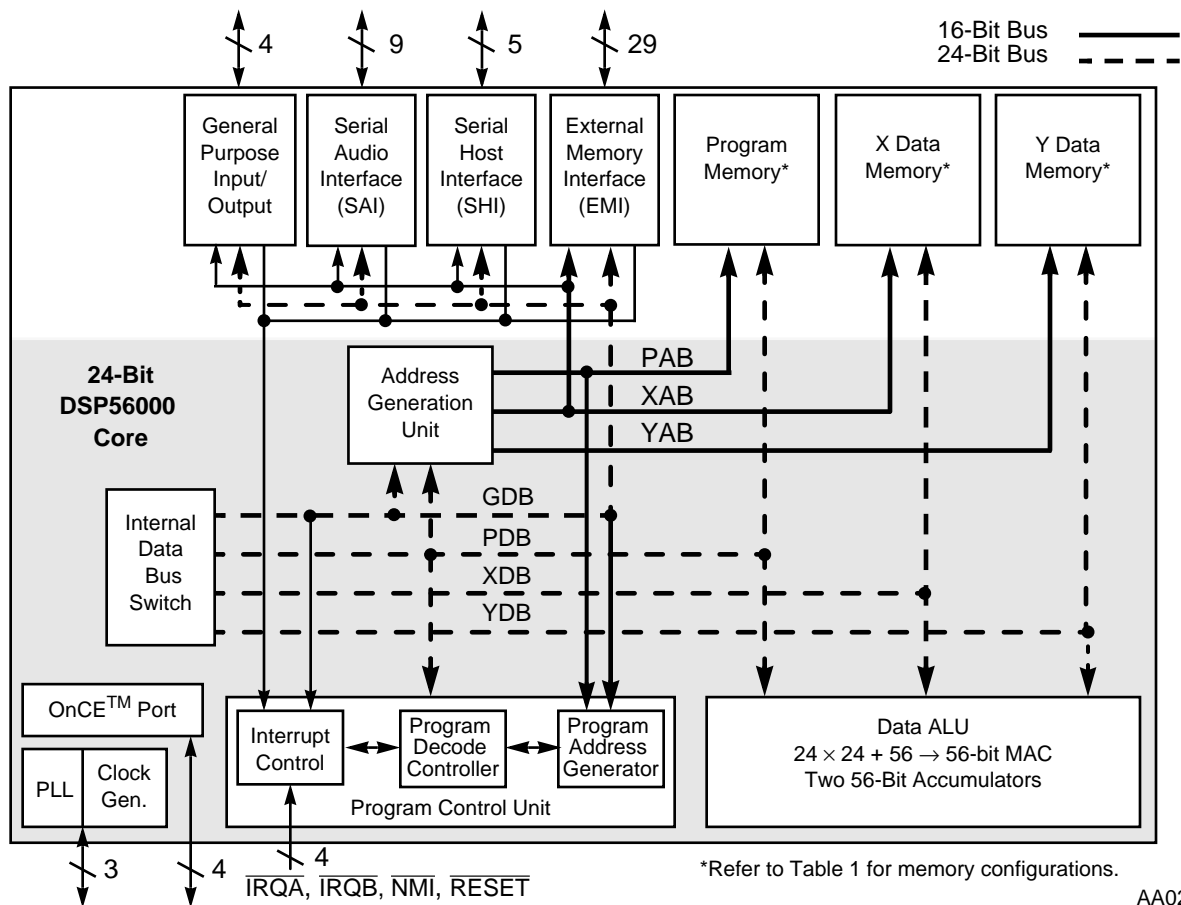


Figure 1 DSP56004 Block Diagram

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**Data Sheet Conventions**

This data sheet uses the following conventions:

- OVERBAR**      Used to indicate a signal that is active when pulled low (For example, the  $\overline{\text{RESET}}$  pin is active when low.)
- “asserted”      Means that a high true (active high) signal is high or that a low true (active low) signal is low
- “deasserted”    Means that a high true (active high) signal is low or that a low true (active low) signal is high

Examples:	Signal/Symbol	Logic State	Signal State	Voltage
	$\overline{\text{PIN}}$	True	Asserted	$V_{\text{IL}}/V_{\text{OL}}$
	$\overline{\text{PIN}}$	False	Deasserted	$V_{\text{IH}}/V_{\text{OH}}$
	PIN	True	Asserted	$V_{\text{IH}}/V_{\text{OH}}$
	PIN	False	Deasserted	$V_{\text{IL}}/V_{\text{OL}}$

Note: Values for  $V_{\text{IL}}$ ,  $V_{\text{OL}}$ ,  $V_{\text{IH}}$ , and  $V_{\text{OH}}$  are defined by individual product specifications.

## FEATURES

### Digital Signal Processing Core

- Efficient, object code compatible with the 24-bit DSP56000 core engine
- Up to 40.5 Million Instructions Per Second (MIPS)—24.7 ns instruction cycle at 81 MHz; up to 324 Million Operations Per Second (MOPS) at 81 MHz
- Highly parallel instruction set with unique DSP addressing modes
- Two 56-bit accumulators including extension byte
- Parallel  $24 \times 24$ -bit multiply-accumulate in 1 instruction cycle (2 clock cycles)
- Double precision  $48 \times 48$ -bit multiply with 96-bit result in 6 instruction cycles
- 56-bit addition/subtraction in 1 instruction cycle
- Fractional and integer arithmetic with support for multiprecision arithmetic
- Hardware support for block floating-point Fast Fourier Transforms (FFT)
- Hardware nested DO loops
- Zero-overhead fast interrupts (2 instruction cycles)
- Four 24-bit internal data buses and three 16-bit internal address buses for simultaneous accesses to one program and two data memories
- Fabricated in high-density CMOS

### Memory

- On-chip modified Harvard architecture which permits simultaneous accesses to program and two data memories
- Bootstrap loading from Serial Host Interface or External Memory Interface

**Table 1** Memory Configuration (Word width is 24 bits)

Part Type	Program		X Data		Y Data		Boot-strap ROM
	ROM	RAM	ROM	RAM	ROM	RAM	
DSP56004 <sup>1</sup>	None	512	256	256	256	256	64
DSP56004ROM <sup>2</sup>	2560	256	256	256	256	256	64

Note: 1. X data ROM is programmed with  $\log_2 x$  and  $2^x$  tables; Y data ROM is programmed with a sine table.  
 2. These ROMs may be factory programmed with data/program provided by the application developer.

## Peripheral and Support Circuits

- Serial Audio Interface (SAI) includes two receivers and three transmitters, master or slave capability, implementation of I<sup>2</sup>S, Sony, and Matsushita audio protocols; and two sets of SAI interrupt vectors
- Serial Host Interface (SHI) features single master capability, 10-word receive FIFO, and support for 8-, 16-, and 24-bit words
- External Memory Interface (EMI), implemented as a peripheral supporting:
  - Page-mode DRAMs (one or two chips): 64 K × 4, 256 K × 4, and 4 M × 4 bits
  - SRAMs (one to four): 256 K × 8 bits
  - Data bus may be 4 or 8 bits wide
  - Data words may be 8, 12, 16, 20, or 24 bits wide
- Four dedicated, independent, programmable General Purpose Input/Output (GPIO) lines
- On-chip peripheral registers memory mapped in data memory space
- Three external interrupt request pins
- On-Chip Emulation (OnCE) port for unobtrusive, processor speed-independent debugging
- Software-programmable, Phase Lock Loop-based (PLL) frequency synthesizer for the core clock
- Power-saving Wait and Stop modes
- Fully static, HCMOS design for operating frequencies down to dc
- 80-pin plastic Quad Flat Pack surface-mount package; 14 × 14 × 2.20 mm (2.15–2.45 mm range); 0.65 mm lead pitch
- Complete pinout compatibility between DSP56004, DSP56004ROM, DSP56007, and DSP56009 for easy upgrades
- 5 V power supply

## PRODUCT DOCUMENTATION

**Table 2** lists the documents that provide a complete description of the DSP56004 and are required to design properly with the part. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, a Motorola Literature Distribution Center, or through the Motorola DSP home page on the Internet (the source for the latest information).

**Table 2** DSP56004 Documentation

Document Name	Description of Content	Order Number
DSP56000 Family Manual	DSP56000 core family architecture and the 24-bit core processor and instruction set	DSP56KFAMUM/AD
DSP56004 User's Manual	Memory, peripherals, and interfaces	DSP56004UM/AD
DSP56004 Technical Data	Electrical and timing specifications, and pin and package descriptions	DSP56004/D





## SECTION 1

## SIGNAL/CONNECTION DESCRIPTIONS

## SIGNAL GROUPINGS

The DSP56004 input and output signals are organized into the nine functional groups, as shown in **Table 1-1**. The individual signals are illustrated in **Figure 1-1**.

**Table 1-1** DSP56004 Functional Group Signal Allocations

Functional Group	Number of Signals	Detailed Description
Power ( $V_{CC}$ )	9	<b>Table 1-2</b>
Ground (GND)	13	<b>Table 1-3</b>
Phase Lock Loop (PLL)	3	<b>Table 1-4</b>
External Memory Interface (EMI)	29	<b>Table 1-5 and Table 1-6</b>
Interrupt and Mode Control	4	<b>Table 1-7</b>
Serial Host Interface (SHI)	5	<b>Table 1-8</b>
Serial Audio Interface (SAI)	9	<b>Table 1-9 and Table 1-10</b>
General Purpose Input/Output (GPIO)	4	<b>Table 1-11</b>
On-Chip Emulation (OnCE) port	4	<b>Table 1-12</b>
Total	80	

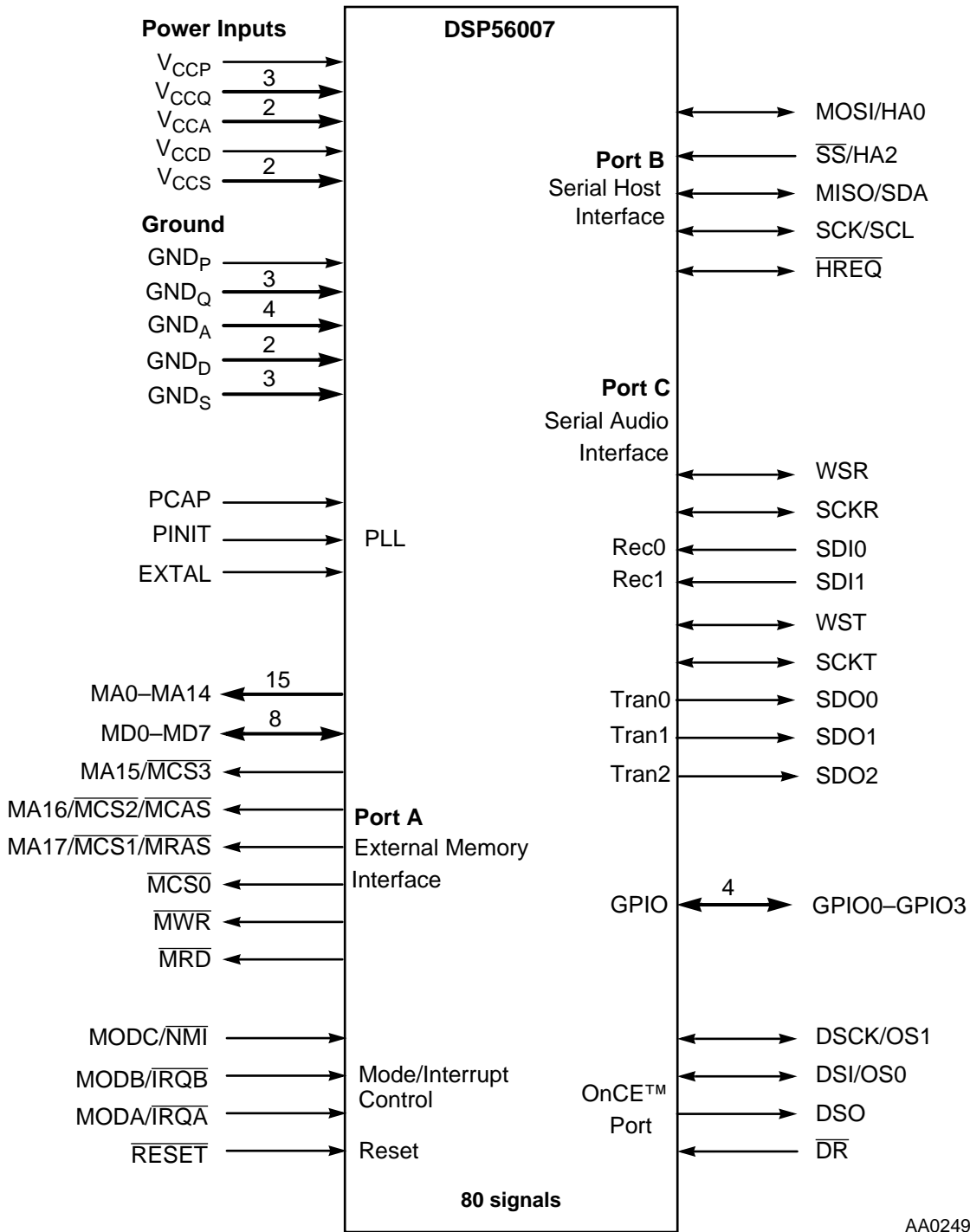


Figure 1-1 DSP56004 Signals



## POWER

Table 1-2 Power Inputs

Power Name	Description
V <sub>CCP</sub>	<b>PLL Power</b> —V <sub>CCP</sub> provides isolated power for the Phase Lock Loop (PLL). The voltage should be well-regulated and the input should be provided with an extremely low impedance path to the V <sub>CC</sub> power rail.
V <sub>CCQ</sub>	<b>Quiet Power</b> —V <sub>CCQ</sub> provides isolated power for the internal processing logic. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors.
V <sub>CCA</sub>	<b>Address Bus Power</b> —V <sub>CCA</sub> provides isolated power for sections of the address bus I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors.
V <sub>CCD</sub>	<b>Data Bus Power</b> —V <sub>CCD</sub> provides isolated power for sections of the data bus I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors.
V <sub>CCS</sub>	<b>Serial Interface Power</b> —V <sub>CCS</sub> provides isolated power for the SHI and SAI. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors.

## GROUND

Table 1-3 Grounds

Ground Name	Description
GND <sub>P</sub>	<b>PLL Ground</b> —GND <sub>P</sub> is ground dedicated for PLL use. The connection should be provided with an extremely low-impedance path to ground. V <sub>CCP</sub> should be bypassed to GND <sub>P</sub> by a 0.47 μF capacitor located as close as possible to the chip package.
GND <sub>Q</sub>	<b>Quiet Ground</b> —GND <sub>Q</sub> provides isolated ground for the internal processing logic. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.
GND <sub>A</sub>	<b>Address Bus Ground</b> —GND <sub>A</sub> provides isolated ground for sections of the address bus I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.
GND <sub>D</sub>	<b>Data Bus Ground</b> —GND <sub>D</sub> provides isolated ground for sections of the data bus I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.
GND <sub>S</sub>	<b>Serial Interface Ground</b> —GND <sub>S</sub> provides isolated ground for the SHI and SAI. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.

## CLOCK AND PLL SIGNALS

**Note:** While the PLL on this DSP is identical to the PLL described in the *DSP56000 Family Manual*, two of the signals have not been implemented externally. Specifically, there is no PLOCK signal or CKOUT signal available. Therefore, the internal clock is not directly accessible and there is no external indication that the PLL is locked. These signals were omitted to reduce the number of pins and allow this DSP to be put in a smaller, less expensive package.

**Table 1-4** Clock and PLL Signals

Signal Name	Signal Type	State during Reset	Signal Description
EXTAL	Input	Input	<b>External Clock/Crystal</b> —This input should be connected to an external clock source. If the PLL is enabled, this signal is internally connected to the on-chip PLL. The PLL can multiply the frequency on the EXTAL pin to generate the internal DSP clock. The PLL output is divided by two to produce a four-phase instruction cycle clock, with the minimum instruction time being two PLL output clock periods. If the PLL is disabled, EXTAL is divided by two to produce the four-phase instruction cycle clock.
PCAP	Input	Input	<b>PLL Filter Capacitor</b> —This input is used to connect a high-quality (high “Q” factor) external capacitor needed for the PLL filter. The capacitor should be as close as possible to the DSP with heavy, short traces connecting one terminal of the capacitor to PCAP and the other terminal to $V_{CCP}$ . The required capacitor value is specified in <b>Table 2-6</b> on page 2-6.  <b>Note:</b> When short lock time is critical, low dielectric absorption capacitors such as polystyrene, polypropylene, or teflon are recommended.  If the PLL is not used (i.e., it remains disabled at all times), there is no need to connect a capacitor to the PCAP pin. It may remain unconnected, or be tied to either $V_{CC}$ or GND.
PINIT	Input	Input	<b>PLL Initialization (PINIT)</b> —During the assertion of hardware reset, the value on the PINIT line is written into the PEN bit of the PCTL register. When set, the PEN bit enables the PLL by causing it to derive the internal clocks from the PLL voltage controlled oscillator output. When the bit is cleared, the PLL is disabled and the DSP’s internal clocks are derived from the clock connected to the EXTAL signal. After hardware $\overline{\text{RESET}}$ is deasserted, the PINIT signal is ignored.

**EXTERNAL MEMORY INTERFACE (EMI)**

**Table 1-5 External Memory Interface (EMI) Signals**

Signal Name	Signal Type	State during Reset	Signal Description
MA0–MA14	Output	<b>Table 1-6</b>	<b>Memory Address Lines 0–14</b> —The MA0–MA10 lines provide the multiplexed row/column addresses for DRAM accesses. Lines MA0–MA14 provide the non-multiplexed address lines 0–14 for SRAM accesses.
MA15	Output	<b>Table 1-6</b>	<b>Memory Address Line 15 (MA15)</b> —This line functions as the non-multiplexed address line 15.
$\overline{\text{MCS3}}$			<b>Memory Chip Select 3 (<math>\overline{\text{MCS3}}</math>)</b> —For SRAM accesses, this line functions as memory chip select 3.
MA16	Output	<b>Table 1-6</b>	<b>Memory Address Line 16 (MA16)</b> —This line functions as the non-multiplexed address line 16 or as memory chip select 2 for SRAM accesses.
$\overline{\text{MCS2}}$			<b>Memory Chip Select 2 (<math>\overline{\text{MCS2}}</math>)</b> —For SRAM access, this line functions as memory chip select 2.
$\overline{\text{MCAS}}$			<b>Memory Column Address Strobe (<math>\overline{\text{MCAS}}</math>)</b> —This line functions as the Memory Column Address Strobe ( $\overline{\text{MCAS}}$ ) during DRAM accesses.
MA17	Output	<b>Table 1-6</b>	<b>Memory Address Line 17 (MA17)</b> —This line functions as the non-multiplexed address line 17.
$\overline{\text{MCS1}}$			<b>Memory Chip Select 1 (MCS1)</b> —This line functions as chip select 1 for SRAM accesses.
$\overline{\text{MRAS}}$			<b>Memory Row Address Strobe (<math>\overline{\text{MRAS}}</math>)</b> —This line also functions as the Memory Row Address Strobe during DRAM accesses.
$\overline{\text{MCS0}}$	Output	<b>Table 1-6</b>	<b>Memory Chip Select 0</b> —This line functions as memory chip select 0 for SRAM accesses.
$\overline{\text{MWR}}$	Output	<b>Table 1-6</b>	<b>Memory Write Strobe</b> —This line is asserted when writing to external memory.
$\overline{\text{MRD}}$	Output	<b>Table 1-6</b>	<b>Memory Read Strobe</b> —This line is asserted when reading external memory.

**Table 1-5** External Memory Interface (EMI) Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
MD0–MD7	Bidi-rectional	Tri-stated	<b>Data Bus</b> —These signals provide the bidirectional data bus for EMI accesses. They are inputs during reads from external memory, outputs during writes to external memory, and tri-stated if no external access is taking place. If the data bus width is defined as four bits wide, only signals MD0–MD3 are active, while signals MD4–MD7 remain tri-stated. While tri-stated, MD0–MD7 are disconnected from the pins and do not require external pull-ups.

**Table 1-6** EMI States during Reset and Stop States

Signal	Operating Mode			
	Hardware Reset	Software Reset	Individual Reset	Stop Mode
MA0–MA14	Driven High	Previous State	Previous State	Previous State
MA15	Driven High	Driven High	Previous State	Previous State
MCS3	Driven High	Driven High	Driven High	Driven High
MA16	Driven High	Driven High	Previous State	Previous State
MCS2	Driven High	Driven High	Driven High	Driven High
MCAS: DRAM refresh disabled DRAM refresh enabled	Driven High Driven High	Driven High Driven High	Driven High Driven Low	Driven High Driven High
MA17	Driven High	Driven High	Previous State	Previous State
$\overline{\text{MCS1}}$	Driven High	Driven High	Driven High	Driven High
$\overline{\text{MRAS}}$ : DRAM refresh disabled DRAM refresh enabled	Driven High Driven High	Driven High Driven High	Driven High Driven Low	Driven High Driven High
$\overline{\text{MCS0}}$	Driven High	Driven High	Driven High	Driven High
$\overline{\text{MWR}}$	Driven High	Driven High	Driven High	Driven High
$\overline{\text{MRD}}$	Driven High	Driven High	Driven High	Driven High

## INTERRUPT AND MODE CONTROL

The interrupt and mode control signals select the DSP's operating mode as it comes out of hardware reset and receives interrupt requests from external sources after reset.

**Table 1-7** Interrupt and Mode Control Signals

Signal Name	Signal Type	State during Reset	Signal Description
MODA	Input	Input (MODA)	<p><b>Mode Select A</b>—This input signal has three functions:</p> <ul style="list-style-type: none"> <li>to work with the MODB and MODC signals to select the DSP's initial operating mode,</li> <li>to allow an external device to request a DSP interrupt after internal synchronization, and</li> <li>to turn on the internal clock generator when the DSP is in the Stop processing state, causing the DSP to resume processing.</li> </ul> <p>MODA is read and internally latched in the DSP when the processor exits the Reset state. The logic state present on the MODA, MODB, and MODC pins selects the initial DSP operating mode. Several clock cycles after leaving the Reset state, the MODA signal changes to the external interrupt request <math>\overline{IRQA}</math>. The DSP operating mode can be changed by software after reset.</p>
$\overline{IRQA}$			<p><b>External Interrupt Request A (<math>\overline{IRQA}</math>)</b>—The <math>\overline{IRQA}</math> input is a synchronized external interrupt request. It may be programmed to be level-sensitive or negative-edge-triggered. When the signal is edge-triggered, triggering occurs at a voltage level and is not directly related to the fall time of the interrupt signal. However, as the fall time of the interrupt signal increases, the probability that noise on <math>\overline{IRQA}</math> will generate multiple interrupts also increases.</p> <p>While the DSP is in the Stop mode, asserting <math>\overline{IRQA}</math> gates on the oscillator and, after a clock stabilization delay, enables clocks to the processor and peripherals. Hardware reset causes this input to function as MODA.</p>

**Table 1-7** Interrupt and Mode Control Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
MODB	Input	Input (MODB)	<p><b>Mode Select B</b>—This input signal has two functions:</p> <ul style="list-style-type: none"> <li>to work with the MODA and MODC signals to select the DSP's initial operating mode, and</li> <li>to allow an external device to request a DSP interrupt after internal synchronization.</li> </ul> <p>MODB is read and internally latched in the DSP when the processor exits the Reset state. The logic state present on the MODA, MODB, and MODC pins selects the initial DSP operating mode. Several clock cycles after leaving the Reset state, the MODB signal changes to the external interrupt request <math>\overline{\text{IRQB}}</math>. The DSP operating mode can be changed by software after reset.</p>
$\overline{\text{IRQB}}$			<p><b>External Interrupt Request B (<math>\overline{\text{IRQB}}</math>)</b>—The <math>\overline{\text{IRQB}}</math> input is a synchronized external interrupt request. It may be programmed to be level-sensitive or negative-edge-triggered. When the signal is edge-triggered, triggering occurs at a voltage level and is not directly related to the fall time of the interrupt signal. However, as the fall time of the interrupt signal increases, the probability that noise on <math>\overline{\text{IRQB}}</math> will generate multiple interrupts also increases. Hardware reset causes this input to function as MODB.</p>

Table 1-7 Interrupt and Mode Control Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
MODC	Input, edge-triggered	Input (MODC)	<p><b>Mode Select C</b>—This input signal has two functions:</p> <ul style="list-style-type: none"> <li>to work with the MODA and MODB signals to select the DSP's initial operating mode, and</li> <li>to allow an external device to request a DSP interrupt after internal synchronization.</li> </ul> <p>MODC is read and internally latched in the DSP when the processor exits the Reset state. The logic state present on the MODA, MODB, and MODC pins selects the initial DSP operating mode. Several clock cycles after leaving the Reset state, the MODC signal changes to the Non-Maskable Interrupt request, <math>\overline{\text{NMI}}</math>. The DSP operating mode can be changed by software after reset.</p>
$\overline{\text{NMI}}$			<p><b>Non-Maskable Interrupt Request</b>—The <math>\overline{\text{NMI}}</math> input is a negative-edge-triggered external interrupt request. This is a level 3 interrupt that can not be masked out. Triggering occurs at a voltage level and is not directly related to the fall time of the interrupt signal. However, as the fall time of the interrupt signal increases, the probability that noise on <math>\overline{\text{NMI}}</math> will generate multiple interrupts also increases. Hardware reset causes this input to function as MODC.</p>
$\overline{\text{RESET}}$	input	active	<p><b><math>\overline{\text{RESET}}</math></b>—This input causes a direct hardware reset of the processor. When <math>\overline{\text{RESET}}</math> is asserted, the DSP is initialized and placed in the Reset state. A Schmitt-trigger input is used for noise immunity. When the reset signal is deasserted, the initial DSP operating mode is latched from the MODA, MODB, and MODC signals. The DSP also samples the PINIT signal and writes its status into the PEN bit of the PLL Control Register. When the DSP comes out of the Reset state, deassertion occurs at a voltage level and is not directly related to the rise time of the <math>\overline{\text{RESET}}</math> signal. However, the probability that noise on <math>\overline{\text{RESET}}</math> will generate multiple resets increases with increasing rise time of the <math>\overline{\text{RESET}}</math> signal.</p> <p>For proper hardware reset to occur, the clock must be active, since a number of clock ticks are required for proper propagation of the hardware Reset state.</p>

**SERIAL HOST INTERFACE (SHI)**

The Serial Host Interface (SHI) has five I/O signals, which may be configured to operate in either SPI or I<sup>2</sup>C mode. **Table 1-8** lists the SHI signals.

**Table 1-8** Serial Host Interface (SHI) signals

Signal Name	Signal Type	State during Reset	Signal Description
SCK	Input or Output	Tri-stated	<b>SPI Serial Clock (SCK)</b> —The SCK signal is an output when the SPI is configured as a master, and a Schmitt-trigger input when the SPI is configured as a slave. When the SPI is configured as a master, the SCK signal is derived from the internal SHI clock generator. When the SPI is configured as a slave, the SCK signal is an input, and the clock signal from the external master synchronizes the data transfer. The SCK signal is ignored by the SPI if it is defined as a slave and the Slave Select ( $\overline{SS}$ ) signal is not asserted. In both the master and slave SPI devices, data is shifted on one edge of the SCK signal and is sampled on the opposite edge where data is stable. Edge polarity is determined by the SPI transfer protocol.
SCL	Input or Output		<b>I<sup>2</sup>C Serial Clock (SCL)</b> —SCL carries the clock for bus transactions in the I <sup>2</sup> C mode. SCL is a Schmitt-trigger input when configured as a slave, and an open-drain output when configured as a master. SCL should be connected to V <sub>CC</sub> through a pull-up resistor. The maximum allowed internally generated bit clock frequency is $F_{osc}/4$ for the SPI mode and $F_{osc}/6$ for the I <sup>2</sup> C mode where $F_{osc}$ is the clock on EXTAL. The maximum allowed externally generated bit clock frequency is $F_{osc}/3$ for the SPI mode and $F_{osc}/5$ for the I <sup>2</sup> C mode. This signal is tri-stated during hardware reset, software reset, or individual reset (no need for external pull-up in this state).

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Table 1-8 Serial Host Interface (SHI) signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
MISO	Input or Output	Tri-stated	<b>SPI Master-In-Slave-Out (MISO)</b> —When the SPI is configured as a master, MISO is the master data input line. The MISO signal is used in conjunction with the MOSI signal for transmitting and receiving serial data. This signal is a Schmitt-trigger input when configured for the SPI Master mode, an output when configured for the SPI Slave mode, and tri-stated if configured for the SPI Slave mode when $\overline{SS}$ is deasserted.
SDA	Input or Output	Tri-stated	<b>I<sup>2</sup>C Serial Data and Acknowledge (SDA)</b> —In I <sup>2</sup> C mode, SDA is a Schmitt-trigger input when receiving and an open-drain output when transmitting. SDA should be connected to V <sub>CC</sub> through a pull-up resistor. SDA carries the data for I <sup>2</sup> C transactions. The data in SDA must be stable during the high period of SCL. The data in SDA is only allowed to change when SCL is low. When the bus is free, SDA is high. The SDA line is only allowed to change during the time SCL is high in the case of Start and Stop events. A high-to-low transition of the SDA line while SCL is high is a unique situation, and is defined as the Start event. A low-to-high transition of SDA while SCL is high is a unique situation, and is defined as the Stop event.  <b>Note:</b> This line is tri-stated during hardware reset, software reset, or individual reset (no need for external pull-up in this state).
MOSI	Input or Output	Tri-stated	<b>SPI Master-Out-Slave-In (MOSI)</b> —When the SPI is configured as a master, MOSI is the master data output line. The MOSI signal is used in conjunction with the MISO signal for transmitting and receiving serial data. MOSI is the slave data input line when the SPI is configured as a slave. This signal is a Schmitt-trigger input when configured for the SPI Slave mode.
HA0	Input	Tri-stated	<b>I<sup>2</sup>C Slave Address 0 (HA0)</b> —This signal uses a Schmitt-trigger input when configured for the I <sup>2</sup> C mode. When configured for I <sup>2</sup> C Slave mode, the HA0 signal is used to form the slave device address. HA0 is ignored when the SHI is configured for the I <sup>2</sup> C Master mode.  <b>Note:</b> This signal is tri-stated during hardware reset, software reset, or individual reset (no need for external pull-up in this state).

**Table 1-8** Serial Host Interface (SHI) signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
$\overline{SS}$	Input	Tri-stated	<p><b>SPI Slave Select (<math>\overline{SS}</math>)</b>—This signal is an active low Schmitt-trigger input when configured for the SPI mode. When configured for the SPI Slave mode, this signal is used to enable the SPI slave for transfer. When configured for the SPI Master mode, this signal should be kept deasserted. If it is asserted while configured as SPI master, a bus error condition will be flagged.</p>
HA2	Input	Tri-stated	<p><b>I<sup>2</sup>C Slave Address 2 (HA2)</b>—This signal uses a Schmitt-trigger input when configured for the I<sup>2</sup>C mode. When configured for the I<sup>2</sup>C Slave mode, the HA2 signal is used to form the slave device address. HA2 is ignored in the I<sup>2</sup>C Master mode. If <math>\overline{SS}</math> is deasserted, the SHI ignores SCK clocks and keeps the MISO output signal in the high-impedance state.</p> <p><b>Note:</b> This signal is tri-stated during hardware reset, software reset, or individual reset (no need for external pull-up in this state).</p>
$\overline{HREQ}$	Input or Output	Tri-stated	<p><b>Host Request</b>—This signal is an active low Schmitt-trigger input when configured for the Master mode, but an active low output when configured for the Slave mode. When configured for the Slave mode, <math>\overline{HREQ}</math> is asserted to indicate that the SHI is ready for the next data word transfer and deasserted at the first clock pulse of the new data word transfer. When configured for the Master mode, <math>\overline{HREQ}</math> is an input and when asserted by the external slave device, it will trigger the start of the data word transfer by the master. After finishing the data word transfer, the master will await the next assertion of <math>\overline{HREQ}</math> to proceed to the next transfer.</p> <p><b>Note:</b> This signal is tri-stated during hardware, software, individual reset, or when the HREQ[1:0] bits (in the HCSR) are cleared (no need for external pull-up in this state).</p>

## SERIAL AUDIO INTERFACE (SAI)

The SAI is composed of separate receiver and transmitter sections.

### SAI Receiver Section

**Table 1-9** Serial Audio Interface (SAI) Receiver signals

Signal Name	Signal Type	State during Reset	Signal Description
SDI0	Input	Tri-stated	<p><b>Serial Data Input 0</b>—While in the high impedance state, the internal input buffer is disconnected from the pin and no external pull-up is necessary. SDI0 is the serial data input for receiver 0.</p> <p><b>Note:</b> This signal is high impedance during hardware or software reset, while receiver 0 is disabled (R0EN = 0), or while the DSP is in the Stop state.</p>
SDI1	Input	Tri-stated	<p><b>Serial Data Input 1</b>—While in the high impedance state, the internal input buffer is disconnected from the pin and no external pull-up is necessary. SDI1 is the serial data input for receiver 1.</p> <p><b>Note:</b> This signal is high impedance during hardware or software reset, while receiver 1 is disabled (R1EN = 0), or while the DSP is in the Stop state.</p>
SCKR	Input or Output	Tri-stated	<p><b>Receive Serial Clock</b>—SCKR is an output if the receiver section is programmed as a master, and a Schmitt-trigger input if programmed as a slave. While in the high impedance state, the internal input buffer is disconnected from the pin and no external pull-up is necessary.</p> <p><b>Note:</b> SCKR is high impedance if all receivers are disabled (individual reset) and during hardware or software reset, or while the DSP is in the Stop state.</p>

**Table 1-9** Serial Audio Interface (SAI) Receiver signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
WSR	Input or Output	Tri-stated	<p><b>Word Select Receive (WSR)</b>—WSR is an output if the receiver section is configured as a master, and a Schmitt-trigger input if configured as a slave. WSR is used to synchronize the data word and to select the left/right portion of the data sample.</p> <p><b>Note:</b> WSR is high impedance if all receivers are disabled (individual reset), during hardware reset, during software reset, or while the DSP is in the Stop state. While in the high impedance state, the internal input buffer is disconnected from the signal and no external pull-up is necessary.</p>

**SAI Transmitter Section**

**Table 1-10** Serial Audio Interface (SAI) Transmitter signals

Signal Name	Signal Type	State during Reset	Signal Description
SDO0	Output	Driven High	<b>Serial Data Output 0 (SDO0)</b> —SDO0 is the serial output for transmitter 0. SDO0 is driven high if transmitter 0 is disabled, during individual reset, hardware reset, and software reset, or when the DSP is in the Stop state.
SDO1	Output	Driven High	<b>Serial Data Output 1 (SDO1)</b> —SDO1 is the serial output for transmitter 1. SDO1 is driven high if transmitter 1 is disabled, during individual reset, hardware reset and software reset, or when the DSP is in the Stop state.
SDO2	Output	Driven High	<b>Serial Data Output 2 (SDO2)</b> —SDO2 is the serial output for transmitter 2. SDO2 is driven high if transmitter 2 is disabled, during individual reset, hardware reset and software reset, or when the DSP is in the Stop state.
SCKT	Input or Output	Tri-stated	<p><b>Serial Clock Transmit (SCKT)</b>—This signal provides the clock for the SAI. SCKT can be an output if the transmit section is configured as a master, or a Schmitt-trigger input if the transmit section is configured as a slave. When the SCKT is an output, it provides an internally generated SAI transmit clock to external circuitry. When the SCKT is an input, it allows external circuitry to clock data out of the SAI.</p> <p><b>Note:</b> SCKT is high impedance if all transmitters are disabled (individual reset), during hardware reset, software reset, or while the DSP is in the Stop state. While in the high impedance state, the internal input buffer is disconnected from the pin and no external pull-up is necessary.</p>
WST	Input or Output	Tri-stated	<p><b>Word Select Transmit (WST)</b>—WST is an output if the transmit section is programmed as a master, and a Schmitt-trigger input if it is programmed as a slave. WST is used to synchronize the data word and select the left/right portion of the data sample.</p> <p><b>Note:</b> WST is high impedance if all transmitters are disabled (individual reset), during hardware or software reset, or while the DSP is in the Stop state. While in the high impedance state, the internal input buffer is disconnected from the pin and no external pull-up is necessary.</p>

GENERAL PURPOSE I/O

Table 1-11 General Purpose I/O (GPIO) Signals

Signal Name	Signal Type	State during Reset	Signal Description
GPIO0–GPIO3	Standard Output, Open-drain Output, or Input	Disconnected	<p>GPIO lines can be used for control and handshake functions between the DSP and external circuitry. Each GPIO line can be configured individually as disconnected, open-drain output, standard output, or an input.</p> <p><b>Note:</b> Hardware reset or software reset configures all the GPIO lines as disconnected (external circuitry connected to these pins may need pull-ups until the pins are configured for operation).</p>

ON-CHIP EMULATION (OnCE™) PORT

There are four signals associated with the OnCE port controller and its serial interface.

Table 1-12 On-Chip Emulation Port Signals

Signal Name	Signal Type	State during Reset	Signal Description
DSI	Input	Output, Driven Low	<p><b>Debug Serial Input (DSI)</b>—The DSI signal is the signal through which serial data or commands are provided to the OnCE port controller. The data received on the DSI signal will be recognized only when the DSP has entered the Debug mode of operation. Data must have valid TTL logic levels before the serial clock falling edge. Data is always shifted into the OnCE port Most Significant Bit (MSB) first.</p>
OS0	Output		<p><b>Operating Status 0 (OS0)</b>—When the DSP is not in the Debug mode, the OS0 signal provides information about the DSP status if it is an output and used in conjunction with the OS1 signal. When switching from output to input, the signal is tri-stated.</p> <p><b>Note:</b> If the OnCE port is in use, an external pull-down resistor should be attached to the DSI/OS0 signal. If the OnCE port is not in use, the resistor is not required.</p>

**Table 1-12** On-Chip Emulation Port Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
DSCK	Input	Output, Driven Low	<p><b>Debug Serial Clock (DSCK)</b>—The DSCK/OS1 signal, when an input, is the signal through which the serial clock is supplied to the OnCE port. The serial clock provides pulses required to shift data into and out of the OnCE port. Data is clocked into the OnCE port on the falling edge and is clocked out of the OnCE port on the rising edge.</p> <p><b>Operating Status 1 (OS1)</b>—If the OS1 signal is an output and used in conjunction with the OS0 signal, it provides information about the DSP status when the DSP is not in the Debug mode. The debug serial clock frequency must be no greater than 1/8 of the processor clock frequency. The signal is tri-stated when it is changing from input to output.</p> <p><b>Note:</b> If the OnCE port is in use, an external pull-down resistor should be attached to the DSCK/OS1 pin. If the OnCE port is not in use, the resistor is not required.</p>
OS1	Output		
DSO	Output	Driven High	<p><b>Debug Serial Output (DSO)</b>—The DSO line provides the data contained in one of the OnCE port controller registers as specified by the last command received from the command controller. The Most Significant Bit (MSB) of the data word is always shifted out of the OnCE port first. Data is clocked out of the OnCE port on the rising edge of DSCK.</p> <p>The DSO line also provides acknowledge pulses to the external command controller. When the DSP enters the Debug mode, the DSO line will be pulsed low to indicate that the OnCE port is waiting for commands. After receiving a read command, the DSO line will be pulsed low to indicate that the requested data is available and the OnCE port is ready to receive clock pulses in order to deliver the data. After receiving a write command, the DSO line will be pulsed low to indicate that the OnCE port is ready to receive the data to be written; after the data is written, another acknowledge pulse will be provided.</p> <p><b>Note:</b> During hardware reset and when idle, the DSO line is held high.</p>

**Table 1-12** On-Chip Emulation Port Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
$\overline{DR}$	Input	Input	<p><b>Debug Request (<math>\overline{DR}</math>)</b>—The debug request input provides a means of entering the Debug mode of operation. This signal, when asserted (pulled low), will cause the DSP to finish the current instruction being executed, to save the instruction pipeline information, to enter the Debug mode, and to wait for commands to be entered from the debug serial input line. While the DSP is in the Debug mode, the user can reset the OnCE port controller by asserting <math>\overline{DR}</math>, waiting for an acknowledge pulse on DSO, and then deasserting <math>\overline{DR}</math>. It may be necessary to reset the OnCE port controller in cases where synchronization between the OnCE port controller and external circuitry is lost. Asserting <math>\overline{DR}</math> when the DSP is in the Wait or the Stop mode, and keeping it asserted until an acknowledge pulse in the DSP is produced, puts the DSP into the Debug mode. After receiving the acknowledge pulse, <math>\overline{DR}</math> must be deasserted before sending the first OnCE port command. For more information, see Methods Of Entering The Debug Mode in the <i>DSP56000 Family Manual</i>.</p> <p><b>Note:</b> If the OnCE port is not in use, an external pull-up resistor should be attached to the DR line.</p>





## SECTION 2

# SPECIFICATIONS

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### INTRODUCTION

The DSP56004 is fabricated in high density CMOS with Transistor-Transistor Logic (TTL) compatible inputs and outputs.

### MAXIMUM RATINGS

#### CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ).

**Note:** In the calculation of timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a “maximum” value for a specification will never occur in the same device that has a “minimum” value for another specification; adding a maximum to a minimum represents a condition that can never exist.

**Thermal characteristics**

**Table 2-1** Maximum Ratings (GND = 0 V<sub>dc</sub>)

Rating	Symbol	Value	Unit
Supply Voltage	V <sub>CC</sub>	-0.3 to +7.0	V
All Input Voltages: <ul style="list-style-type: none"> <li>• 50 and 66 MHz</li> <li>• 81 MHz</li> </ul>	V <sub>IN</sub>	(GND - 0.5) to (V <sub>CC</sub> + 0.5) (GND - 0.25) to (V <sub>CC</sub> + 0.25)	V
Current Drain per Pin excluding V <sub>CC</sub> and GND	I	10	mA
Operating Temperature Range: <ul style="list-style-type: none"> <li>• 50 and 66 MHz</li> <li>• 81 MHz</li> </ul>	T <sub>J</sub>	-40 to +125 -40 to +120	°C °C
Storage Temperature	T <sub>STG</sub>	-55 to +125	°C

## THERMAL CHARACTERISTICS

**Table 2-2** Thermal Characteristics

Characteristic	Symbol	QFP Value <sup>3</sup>	QFP Value <sup>4</sup>	Unit
Junction-to-ambient thermal resistance <sup>1</sup>	R <sub>θJA</sub> or θ <sub>JA</sub>	70.4	45.1	°C/W
Junction-to-case thermal resistance <sup>2</sup>	R <sub>θJC</sub> or θ <sub>JC</sub>	16.4	—	°C/W
Thermal characterization parameter	Ψ <sub>JT</sub>	3.2	—	°C/W
Notes: 1. Junction-to-ambient thermal resistance is based on measurements on a horizontal-single-sided Printed Circuit Board per SEMI G38-87 in natural convection. (SEMI is Semiconductor Equipment and Materials International, 805 East Middlefield Rd., Mountain View, CA 94043, (415) 964-5111) 2. Junction-to-case thermal resistance is based on measurements using a cold plate per SEMI G30-88, with the exception that the cold plate temperature is used for the case temperature. 3. These are measured values. See note 1 for test board conditions. 4. These are measured values; testing is not complete. Values were measured on a non-standard four-layer thermal test board (two internal planes) at one watt in a horizontal configuration.				

## DC ELECTRICAL CHARACTERISTICS

Table 2-3 DC Electrical Characteristics

Characteristics	Symbol	50 MHz			66 MHz			81 MHz			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Supply voltage	V <sub>CC</sub>	4.5	5.0	5.5	4.5	5.0	5.5	4.75	5.0	5.25	V
Input high voltage											
• EXTAL	V <sub>IHC</sub>	4.0	—	V <sub>CC</sub>	4.0	—	V <sub>CC</sub>	4.0	—	V <sub>CC</sub>	V
• RESET	V <sub>IHR</sub>	2.5	—	V <sub>CC</sub>	2.5	—	V <sub>CC</sub>	2.5	—	V <sub>CC</sub>	V
• MODA, MODB, MODC	V <sub>IHM</sub>	3.5	—	V <sub>CC</sub>	3.5	—	V <sub>CC</sub>	3.5	—	V <sub>CC</sub>	V
• SHI inputs <sup>1</sup>	V <sub>IHS</sub>	0.7 × V <sub>CC</sub>	—	V <sub>CC</sub>	0.7 × V <sub>CC</sub>	—	V <sub>CC</sub>	0.7 × V <sub>CC</sub>	—	V <sub>CC</sub>	V
• All other inputs	V <sub>IH</sub>	2.0	—	V <sub>CC</sub>	2.0	—	V <sub>CC</sub>	2.0	—	V <sub>CC</sub>	V
Input low voltage											
• EXTAL	V <sub>ILC</sub>	-0.5	—	0.6	-0.5	—	0.6	-0.25	—	0.6	V
• MODA, MODB, MODC	V <sub>ILM</sub>	-0.5	—	2.0	-0.5	—	2.0	-0.25	—	2.0	V
• SHI inputs <sup>1</sup>	V <sub>ILS</sub>	-0.5	—	0.3 × V <sub>CC</sub>	-0.5	—	0.3 × V <sub>CC</sub>	-0.25	—	0.3 × V <sub>CC</sub>	V
• All other inputs	V <sub>IL</sub>	-0.5	—	0.8	-0.5	—	0.8	-0.25	—	0.8	V
Input leakage current	I <sub>IN</sub>										
• EXTAL, RESET, MODA, MODB, MODC, DR		-1	—	1	-1	—	1	-1	—	1	μA
• Other Input Pins (@ 2.4 V/0.4 V)		-10	—	10	-10	—	10	-10	—	10	μA
High impedance (off-state) input current (@ 2.4 V / 0.4 V)	I <sub>TSI</sub>	-10	—	10	-10	—	10	-10	—	10	μA
Output high voltage (I <sub>OH</sub> = -0.4 mA)	V <sub>OH</sub>	2.4	—	—	2.4	—	—	2.4	—	—	V
Output low voltage (I <sub>OL</sub> = 3.2 mA) SCK/SCL I <sub>OL</sub> = 6.7 mA MISO/SDA I <sub>OL</sub> = 6.7 mA HREQ I <sub>OL</sub> = 6.7 mA	V <sub>OL</sub>	—	—	0.4	—	—	0.4	—	—	0.4	V
Internal Supply Current											
• Normal mode	I <sub>CCI</sub>	—	75	105 <sup>4</sup>	—	103	130 <sup>4</sup>	—	120	155 <sup>4</sup>	mA
• Wait mode	I <sub>CCW</sub>	—	14	25	—	18	30	—	20	30	mA
• Stop mode <sup>2</sup>	I <sub>CCS</sub>	—	5	110	—	5	110	—	5	110	μA

**Table 2-3** DC Electrical Characteristics

Characteristics	Symbol	50 MHz			66 MHz			81 MHz			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
PLL supply current		—	0.7	1.1	—	1.0	1.5	—	1.2	2.0	mA
Input capacitance <sup>3</sup>	C <sub>IN</sub>	—	10	—	—	10	—	—	10	—	pF

Notes:

1. The SHI inputs are: MOSI/HA0,  $\overline{SS}$ /HA2, MISO/SDA, SCK/SCL, and  $\overline{HREQ}$ .
2. In order to obtain these results, all inputs must be terminated (i.e., not allowed to float). PLL signals are disabled during Stop state.
3. Periodically sampled and not 100% tested
4. Maximum values are derived using the methodology described in **Section 4**. Actual maximums are application dependent and may vary widely from these numbers.

## AC ELECTRICAL CHARACTERISTICS

The timing waveforms in the AC Electrical Characteristics are tested with a  $V_{IL}$  maximum of 0.5 V and a  $V_{IH}$  minimum of 2.4 V for all pins, except EXTAL,  $\overline{RESET}$ , MODA, MODB, MODC, and SHI pins (MOSI/HA0,  $\overline{SS}$ /HA2, MISO/SDA, SCK/SCL,  $\overline{HREQ}$ ). These pins are tested using the input levels set forth in the DC Electrical Characteristics. AC timing specifications that are referenced to a device input signal are measured in production with respect to the 50% point of the respective input signal's transition. DSP56004 output levels are measured with the production test machine  $V_{OL}$  and  $V_{OH}$  reference levels set at 0.8 V and 2.0 V, respectively.

All output delays are given for a 50 pF load unless otherwise specified.

For load capacitance greater than 50 pF, the drive capability of the output pins typically decreases linearly:

1. At 1.5 ns per 10 pF of additional capacitance at all output pins except MOSI/HA0, MISO/SDA, SCK/SCL,  $\overline{HREQ}$
2. At 1.0 ns per 10 pF of additional capacitance at output pins MOSI/HA0, MISO/SDA, SCK/SCL,  $\overline{HREQ}$  (in SPI mode only)

## INTERNAL CLOCKS

For each occurrence of  $T_H$ ,  $T_L$ ,  $T_C$  or  $I_{CYC}$ , substitute with the numbers in Table 2-4.

**Table 2-4** Internal Clocks

Characteristics	Symbol	Expression	
		Minimum	Maximum
Internal Operation Frequency	f		
Internal Clock High Period • with PLL disabled • with PLL enabled and $MF \leq 4$ • with PLL enabled and $MF > 4$	$T_H$ $ET_H$	$0.48 \times T_C$ $0.467 \times T_C$	$0.52 \times T_C$ $0.533 \times T_C$
Internal Clock Low Period • with PLL disabled • with PLL enabled and $MF \leq 4$ • with PLL enabled and $MF > 4$	$T_L$ $ET_L$	$0.48 \times T_C$ $0.467 \times T_C$	$0.52 \times T_C$ $0.533 \times T_C$
Internal Clock Cycle Time	$T_C$	$(DF / MF) \times ET_C$	
Instruction Cycle Time	$I_{CYC}$	$2 \times T_C$	

## EXTERNAL CLOCK (EXTAL PIN)

The DSP56004 system clock is externally supplied via the EXTAL pin. Timings shown in this document are valid for clock rise and fall times of 3 ns maximum.

**Table 2-5** External Clock (EXTAL Pin)

No.	Characteristics	Sym.	50 MHz		66 MHz		81 MHz		Unit
			Min	Max	Min	Max	Min	Max	
	Frequency of External Clock (EXTAL Pin)	Ef	0	50	0	66	0	81	MHz
1	External Clock Input High—EXTAL Pin <sup>1</sup> • with PLL disabled (46.7%–53.3% duty cycle) • with PLL enabled (42.5%–57.5% duty cycle)	$ET_H$	9.3	$\infty$	7.1	$\infty$	5.8	$\infty$	ns
			8.5	235500	6.4	235500	5.2	235500	ns
2	External Clock Input Low—EXTAL Pin <sup>1</sup> • with PLL disabled (46.7%–53.3% duty cycle) • with PLL enabled (42.5%–57.5% duty cycle)	$ET_L$	9.3	$\infty$	7.1	$\infty$	5.8	$\infty$	ns
			8.5	235500	6.4	235500	5.2	235500	ns

Table 2-5 External Clock (EXTAL Pin) (Continued)

No.	Characteristics	Sym.	50 MHz		66 MHz		81 MHz		Unit
			Min	Max	Min	Max	Min	Max	
3	External Clock Cycle Time <sup>1</sup> • with PLL disabled • with PLL enabled	ET <sub>C</sub>	20	∞	15.15	∞	12.3	∞	ns
			20	409600	15.15	409600	12.3	409600	ns
4	Instruction Cycle Time = I <sub>cyc</sub> = 2 × T <sub>C</sub> <sup>1</sup> • with PLL disabled • with PLL enabled	I <sub>CYC</sub>	40	∞	30.3	∞	24.7	∞	ns
			40	819200	30.3	819200	24.7	819200	ns

Note: 1. External Clock Input High and External Clock Input Low are measured at 50% of the input transition.

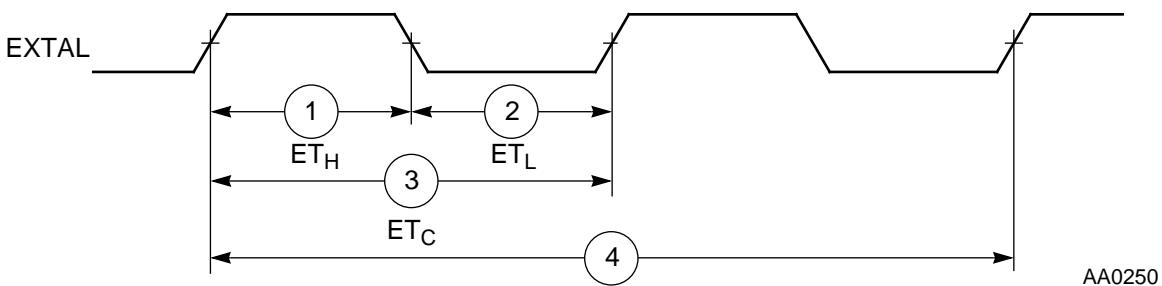


Figure 2-1 External Clock Timing

PHASE LOCK LOOP (PLL) CHARACTERISTICS

Table 2-6 Phase Lock Loop (PLL) Characteristics

Characteristics	Expression	Min	Max	Unit
VCO frequency when PLL enabled	MF × Ef	10	f <sup>1</sup>	MHz
PLL external capacitor (PCAP pin to V <sub>CCP</sub> )	MF × C <sub>PCAP</sub> <sup>1</sup> @ MF ≤ 4 @ MF > 4	MF × 340 MF × 380	MF × 480 MF × 970	pF pF

Note: 1. C<sub>pcap</sub> is the value of the PLL capacitor (connected between PCAP pin and V<sub>CCP</sub>) for MF = 1. The recommended value for C<sub>pcap</sub> is 400 pF for MF ≤ 4 and 540 pF for MF > 4. The maximum VCO frequency is limited to the internal operation frequency, defined in Table 2-4.

RESET, STOP, MODE SELECT, AND INTERRUPT TIMING

Table 2-7 Reset, Stop, Mode Select, and Interrupt Timing ( $C_L = 50 \text{ pF} + 2 \text{ TTL Loads}$ )

No.	Characteristics	All frequencies		Unit
		Min	Max	
10	Minimum $\overline{\text{RESET}}$ assertion width: <ul style="list-style-type: none"> <li>• PLL disabled</li> <li>• PLL enabled<sup>1</sup></li> </ul>	$25 \times T_C$	—	ns
		$2500 \times ET_C$	—	ns
14	Mode Select Setup Time	21	—	ns
15	Mode Select Hold Time	0	—	ns
16	Minimum Edge-triggered Interrupt Request Assertion Width	13	—	ns
16a	Minimum Edge-triggered Interrupt Request Deassertation Width	13	—	ns
18	Delay from $\overline{\text{IRQA}}$ , $\overline{\text{IRQB}}$ , $\overline{\text{NMI}}$ Assertion to GPIO Valid Caused by First Interrupt Instruction Execution	$12 \times T_C + T_H$	—	ns
22	Delay from General Purpose Output Valid to Interrupt Request Deassertation for Level Sensitive Fast Interrupts—If Second Interrupt Instruction is: <sup>2</sup> <ul style="list-style-type: none"> <li>• Single Cycle</li> <li>• Two Cycles</li> </ul>		$T_L - 31$	ns
			$(2 \times T_C) + T_L - 31$	ns
25	Duration of $\overline{\text{IRQA}}$ Assertion for Recovery from Stop State	12	—	ns
27	Duration for Level Sensitive $\overline{\text{IRQA}}$ Assertion to ensure interrupt service (when exiting “Stop”) <ul style="list-style-type: none"> <li>• Stable External Clock, OMR Bit 6 = 1</li> <li>• Stable External Clock, PCTL Bit 17 = 1</li> </ul>	$6 \times T_C + T_L$	—	ns
		12	—	ns

Note: 1. This timing requirement is sensitive to the quality of the external PLL capacitor connected to the PCAP pin. For capacitor values  $\leq 2 \text{ nF}$ , asserting  $\overline{\text{RESET}}$  according to this timing requirement will ensure proper processor initialization for capacitors with a  $\Delta C/C < 0.5\%$ . (This is typical for ceramic capacitors.) For capacitor values  $> 2 \text{ nF}$ , asserting  $\overline{\text{RESET}}$  according to this timing requirement will ensure proper processor initialization for capacitors with a  $\Delta C/C < 0.01\%$ . (This is typical for Teflon, polystyrene, and polypropylene capacitors.) However, capacitors with values  $> 2 \text{ nF}$  with a  $\Delta C/C > 0.01\%$  may require longer  $\overline{\text{RESET}}$  assertion to ensure proper initialization.

2. When using fast interrupts and  $\overline{\text{IRQA}}$  and  $\overline{\text{IRQB}}$  are defined as level-sensitive, then timing 22 applies to prevent multiple interrupt service. To avoid these timing restrictions, the Negative Edge-triggered mode is recommended when using fast interrupts. Long interrupts are recommended when using Level-sensitive mode.

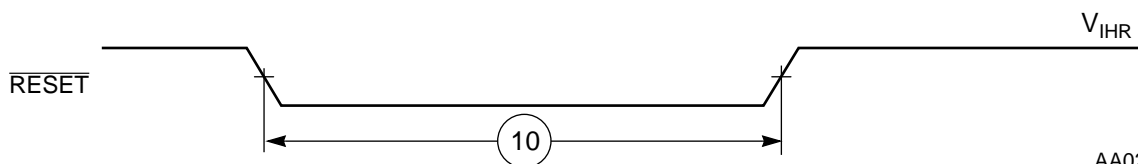
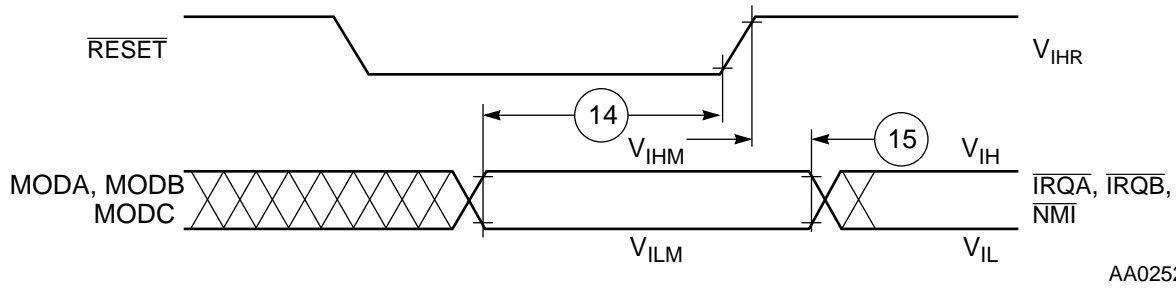
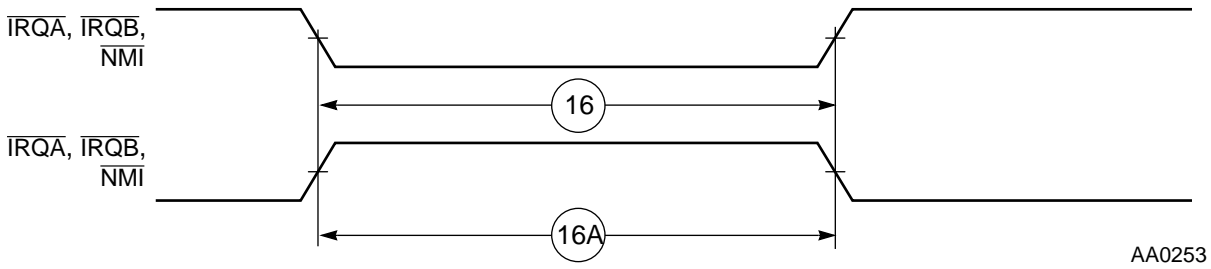


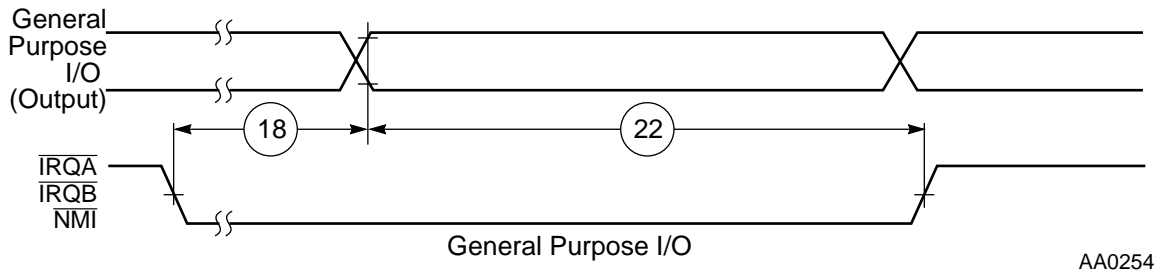
Figure 2-2 Reset Timing



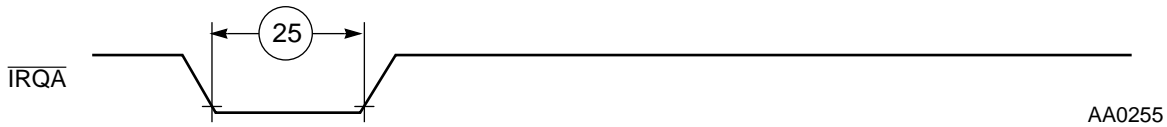
**Figure 2-3** Operating Mode Select Timing



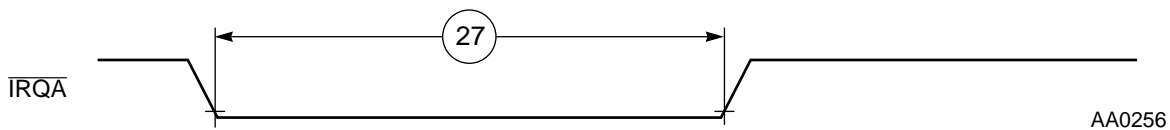
**Figure 2-4** External Interrupt Timing (Negative Edge-triggered)



**Figure 2-5** External Level-sensitive Fast Interrupt Timing



**Figure 2-6** Recovery from Stop State Using  $\overline{\text{IRQA}}$



**Figure 2-7** Recovery from Stop State Using  $\overline{\text{IRQA}}$  Interrupt Service



**EXTERNAL MEMORY INTERFACE (EMI) DRAM TIMING**

( $C_L = 50 \text{ pF} + 2 \text{ TTL Loads}$ )

**Table 2-8** External Memory Interface (EMI) DRAM Timing

No.	Characteristics	Symbol	Timing Mode	Expression	50 MHz		66 MHz		81 MHz		Unit
					Min	Max	Min	Max	Min	Max	
41	Page Mode Cycle Time	$t_{PC}$	slow	$4 \times T_C$	80	—	61	—	49.4	—	ns
			fast	$3 \times T_C$	60	—	46	—	37.0	—	ns
42	$\overline{RAS}$ or $\overline{RD}$ Assertion to Data Valid	$t_{RAC}, t_{GA}$	slow	$7 \times T_C - 16$	—	124	—	90	—	70.4	ns
			fast	$5 \times T_C - 16$	—	84	—	60	—	45.7	ns
43	$\overline{CAS}$ Assertion to Data Valid	$t_{CAC}$	slow	$3 \times T_C - 10$	—	50	—	35	—	27.0	ns
			fast	$2 \times T_C - 10$	—	30	—	20	—	14.7	ns
44	Column Address Valid to Data Valid	$t_{AA}$	slow	$3 \times T_C + T_L - 7$	—	63	—	46	—	36.2	ns
			fast	$2 \times T_C + T_L - 7$	—	43	—	30	—	23.8	ns
45	$\overline{CAS}$ Assertion to Data Active	$t_{CLZ}$		0	0	—	0	—	0	—	ns
46	$\overline{RAS}$ Assertion Pulse Width <sup>1</sup> (Page Mode Access Only)	$t_{RASP}$	slow	$3 \times T_C - 11 + n \times 4 \times T_C$	209	—	156	—	125	—	ns
			fast	$2 \times T_C - 11 + n \times 3 \times T_C$	149	—	110	—	87.8	—	ns
47	$\overline{RAS}$ Assertion Pulse Width (Single Access Only)	$t_{RAS}$	slow	$7 \times T_C - 11$	129	—	95	—	75.4	—	ns
			fast	$5 \times T_C - 11$	89	—	65	—	50.8	—	ns
48	$\overline{RAS}$ or $\overline{CAS}$ Deassertion to $\overline{RAS}$ Assertion	$t_{RP}, t_{CRP}$	slow	$5 \times T_C - 5$	95	—	70	—	56.7	—	ns
			fast	$3 \times T_C - 5$	55	—	40	—	32.0	—	ns
49	$\overline{CAS}$ Assertion Pulse Width	$t_{CAS}$	slow	$3 \times T_C - 10$	50	—	35	—	27.0	—	ns
			fast	$2 \times T_C - 10$	30	—	20	—	14.7	—	ns
50	Last $\overline{CAS}$ Assertion to $\overline{RAS}$ Deassertion (Page Mode Access Only)	$t_{RSH}$	slow	$3 \times T_C - 15$	45	—	30	—	22.0	—	ns
			fast	$2 \times T_C - 15$	25	—	15	—	9.7	—	ns
51	$\overline{RAS}$ or $\overline{WR}$ Assertion to $\overline{CAS}$ Deassertion	$t_{CSH}, t_{CWL}$	slow	$7 \times T_C - 15$	125	—	91	—	71.4	—	ns
			fast	$5 \times T_C - 15$	85	—	61	—	46.7	—	ns
52	$\overline{RAS}$ Assertion to $\overline{CAS}$ Assertion	$t_{RCD}$	slow	$4 \times T_C - 13$	67	—	47	—	36.4	—	ns
			fast	$3 \times T_C - 13$	47	—	32	—	24	—	ns
53	$\overline{RAS}$ Assertion to Column Address Valid	$t_{RAD}$	slow	$3 \times T_C + T_H - 13$	57	—	40	—	30.2	—	ns
			fast	$2 \times T_C + T_H - 13$	37	—	25	—	17.9	—	ns

## Specifications

### External Memory Interface (EMI) DRAM Timing

**Table 2-8** External Memory Interface (EMI) DRAM Timing (Continued)

No.	Characteristics	Symbol	Timing Mode	Expression	50 MHz		66 MHz		81 MHz		Unit
					Min	Max	Min	Max	Min	Max	
54	$\overline{\text{CAS}}$ Deassertion Pulse Width (Page Mode Access Only)	$t_{\text{CP}}$		$T_{\text{C}} - 5$	15	—	10	—	7.3	—	ns
55	Row Address Valid to RAS Assertion (Row Address Setup Time)	$t_{\text{ASR}}$		$T_{\text{L}} - 6$	4	—	2	—	0.2	—	ns
56	RAS Assertion to ROW Address Not Valid (Row Address Hold Time)	$t_{\text{RAH}}$	slow	$3 \times T_{\text{C}} + T_{\text{H}} - 14$	56	—	39	—	29.2	—	ns
			fast	$2 \times T_{\text{C}} + T_{\text{H}} - 14$	36	—	24	—	16.9	—	ns
57	Column Address Valid to CAS Assertion (Column Address Setup Time)	$t_{\text{ASC}}$		$T_{\text{L}} - 6$	4	—	2	—	0.2	—	ns
58	CAS Assertion to Column Address Not Valid (Column Address Hold Time)	$t_{\text{CAH}}$	slow	$3 \times T_{\text{C}} + T_{\text{H}} - 14$	56	—	39	—	29.2	—	ns
			fast	$2 \times T_{\text{C}} + T_{\text{H}} - 14$	36	—	24	—	16.9	—	ns
59	Last $\overline{\text{CAS}}$ Assertion to Column Address Not Valid (Column Address Hold Time)	$t_{\text{CAH}}$	slow	$7 \times T_{\text{C}} + T_{\text{H}} - 14$	136	—	100	—	78.6	—	ns
			fast	$4 \times T_{\text{C}} + T_{\text{H}} - 14$	76	—	54	—	41.6	—	ns
60	$\overline{\text{RAS}}$ Assertion to Column Address Not Valid	$t_{\text{AR}}$	slow	$7 \times T_{\text{C}} + T_{\text{H}} - 14$	136	—	100	—	78.6	—	ns
			fast	$5 \times T_{\text{C}} + T_{\text{H}} - 14$	96	—	69	—	53.9	—	ns
61	Column Address Valid to $\overline{\text{RAS}}$ Deassertion	$t_{\text{RAL}}$	slow	$3 \times T_{\text{C}} + T_{\text{L}} - 7$	63	—	46	—	36.2	—	ns
			fast	$2 \times T_{\text{C}} + T_{\text{L}} - 7$	43	—	30	—	23.9	—	ns
62	$\overline{\text{CAS}}$ , $\overline{\text{RAS}}$ , $\overline{\text{RD}}$ , or $\overline{\text{WR}}$ Deassertion to $\overline{\text{WR}}$ or $\overline{\text{RD}}$ Assertion	$t_{\text{RCH}}$ , $t_{\text{RRH}}$	slow	$5 \times T_{\text{C}} - 11$	89	—	65	—	50.7	—	ns
			fast	$3 \times T_{\text{C}} - 11$	49	—	35	—	26.0	—	ns
63	$\overline{\text{CAS}}$ or $\overline{\text{RD}}$ Deassertion to Data Not Valid (Data Hold Time)	$t_{\text{OFF}}$ , $t_{\text{GZ}}$		0	0	—	0	—	0	—	ns
64	Random Read or Write Cycle Time (Single Access Only)	$t_{\text{RC}}$	slow	$12 \times T_{\text{C}}$	240	—	182	—	148	—	ns
			fast	$8 \times T_{\text{C}}$	160	—	121	—	98.8	—	ns

External Memory Interface (EMI) DRAM Timing

Table 2-8 External Memory Interface (EMI) DRAM Timing (Continued)

No.	Characteristics	Symbol	Timing Mode	Expression	50 MHz		66 MHz		81 MHz		Unit
					Min	Max	Min	Max	Min	Max	
65	$\overline{WR}$ Deassertion to CAS Assertion	$t_{RCS}$	slow	$9 \times T_C - 11$	169	—	125	—	100	—	ns
			fast	$6 \times T_C - 11$	109	—	80	—	63.1	—	ns
66	$\overline{CAS}$ Assertion to $\overline{WR}$ Deassertion	$t_{WCH}$	slow	$3 \times T_C - 13$	47	—	32	—	24	—	ns
			fast	$2 \times T_C - 13$	27	—	17	—	11.7	—	ns
67	Data Valid to $\overline{CAS}$ Assertion (Data Setup Time)	$t_{DS}$		$T_L - 6$	4	—	2	—	0.2	—	ns
68	$\overline{CAS}$ Assertion to Data Not Valid (Data Hold Time)	$t_{DH}$	slow	$3 \times T_C + T_H - 14$	56	—	39	—	29.2	—	ns
			fast	$2 \times T_C + T_H - 14$	36	—	24	—	16.8	—	ns
69	$\overline{RAS}$ Assertion to Data Not Valid	$t_{DHR}$	slow	$7 \times T_C + T_H - 14$	136	—	100	—	78.6	—	ns
			fast	$5 \times T_C + T_H - 14$	96	—	69	—	53.9	—	ns
70	$\overline{WR}$ Assertion to $\overline{CAS}$ Assertion	$t_{WCS}$	slow	$4 \times T_C - 14$	66	—	47	—	35.4	—	ns
			fast	$3 \times T_C - 14$	46	—	31	—	23	—	ns
71	$\overline{WR}$ Assertion Pulse Width (Single Cycle Only)	$t_{WP}$	slow	$7 \times T_C - 9$	131	—	97	—	77.4	—	ns
			fast	$5 \times T_C - 9$	91	—	67	—	52.7	—	ns
72	$\overline{RAS}$ Assertion to $\overline{WR}$ Deassertion (Single Cycle Only)	$t_{WCR}$	slow	$7 \times T_C - 15$	125	—	91	—	71.5	—	ns
			fast	$5 \times T_C - 15$	85	—	61	—	46.7	—	ns
73	$\overline{WR}$ Assertion to Data Active		slow	$3 \times T_C + T_H - 13$	57	—	40	—	30.2	—	ns
			fast	$2 \times T_C + T_H - 13$	37	—	25	—	17.9	—	ns
74	$\overline{RD}$ or $\overline{WR}$ Assertion to $\overline{RAS}$ Deassertion (Single Cycle Only)	$t_{ROH}$ , $t_{RWL}$	slow	$7 \times T_C - 13$	127	—	93	—	73.4	—	ns
			fast	$5 \times T_C - 13$	87	—	63	—	48.7	—	ns

Note: 1. n is the number of successive accesses. n = 2, 3, 4, or 6.

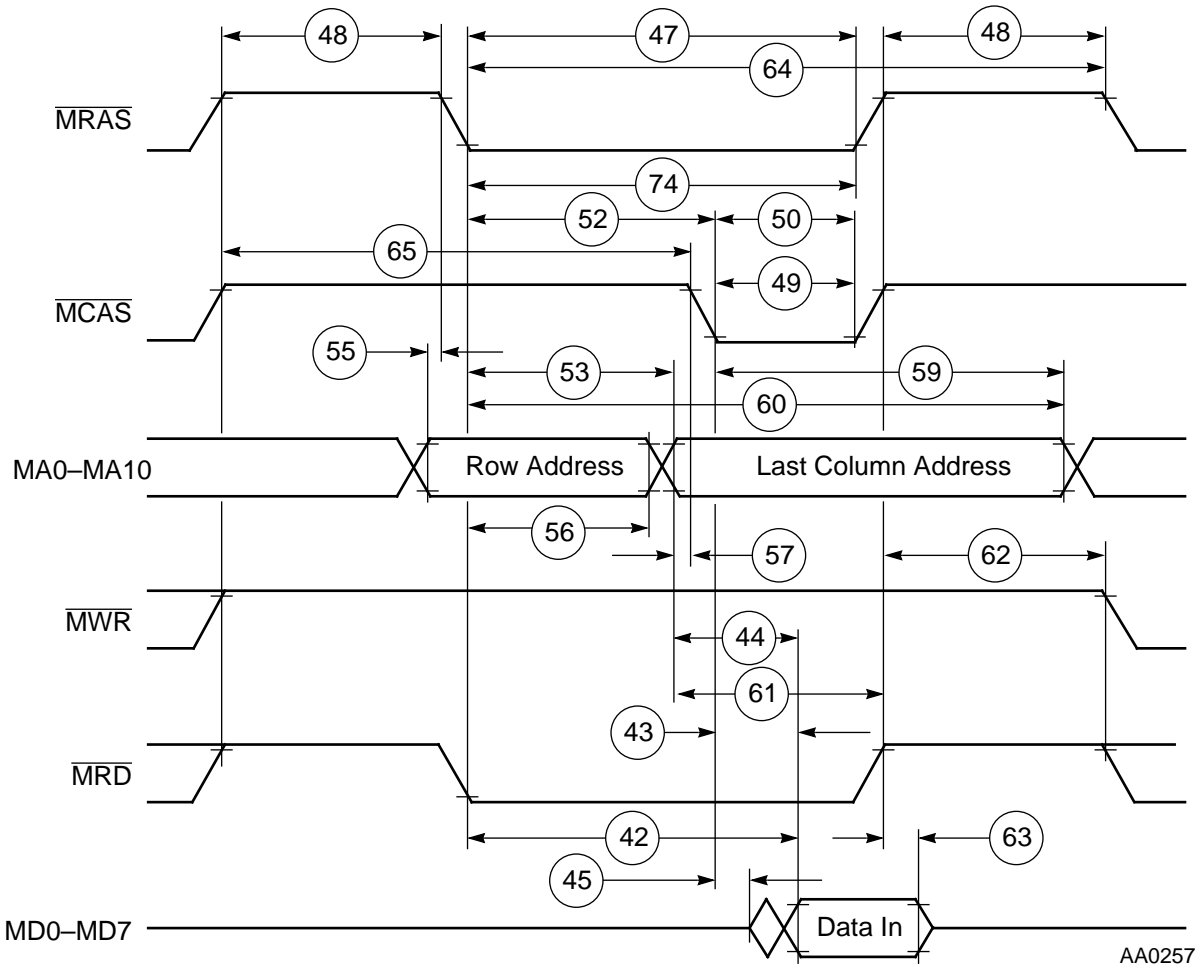
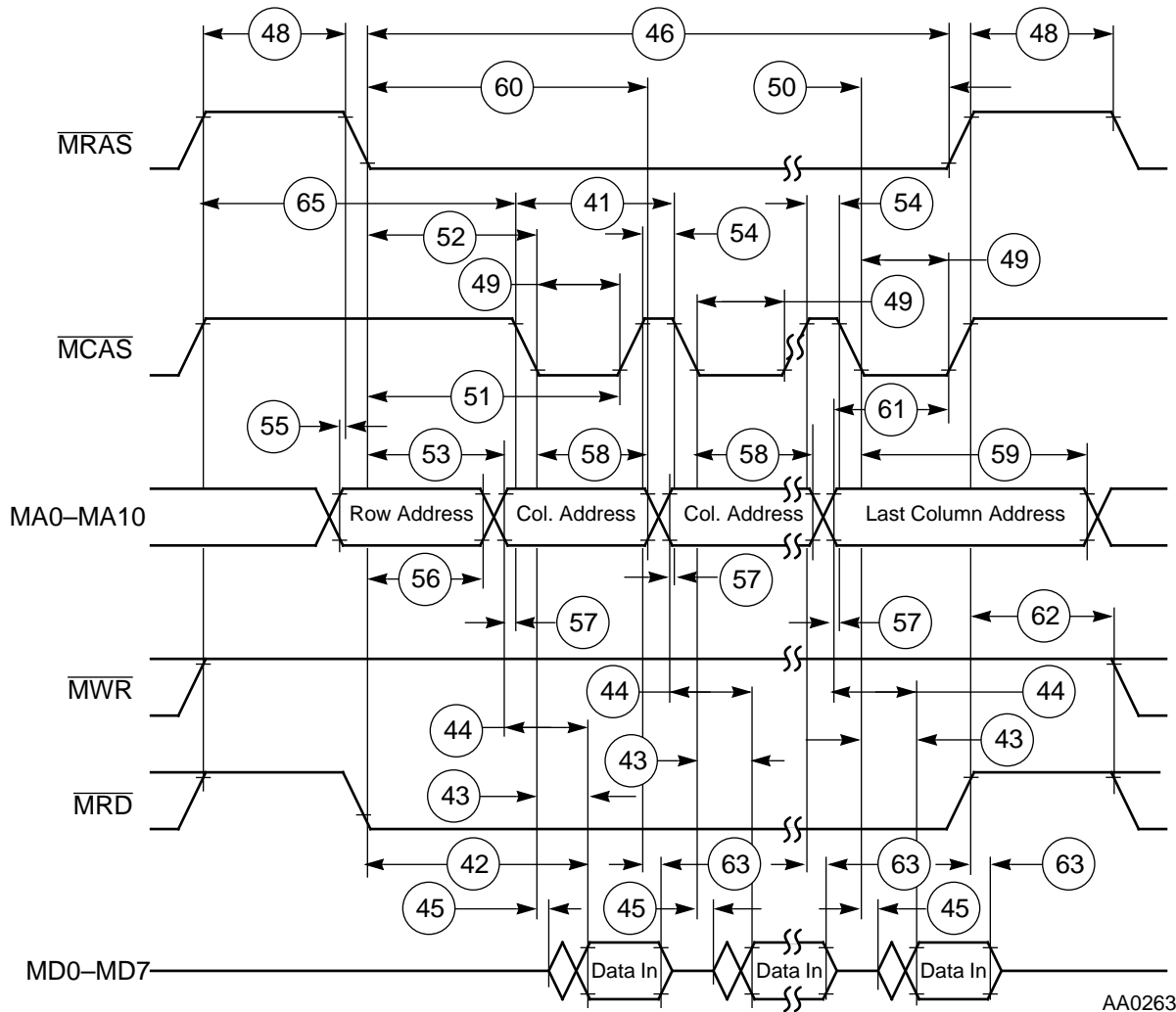
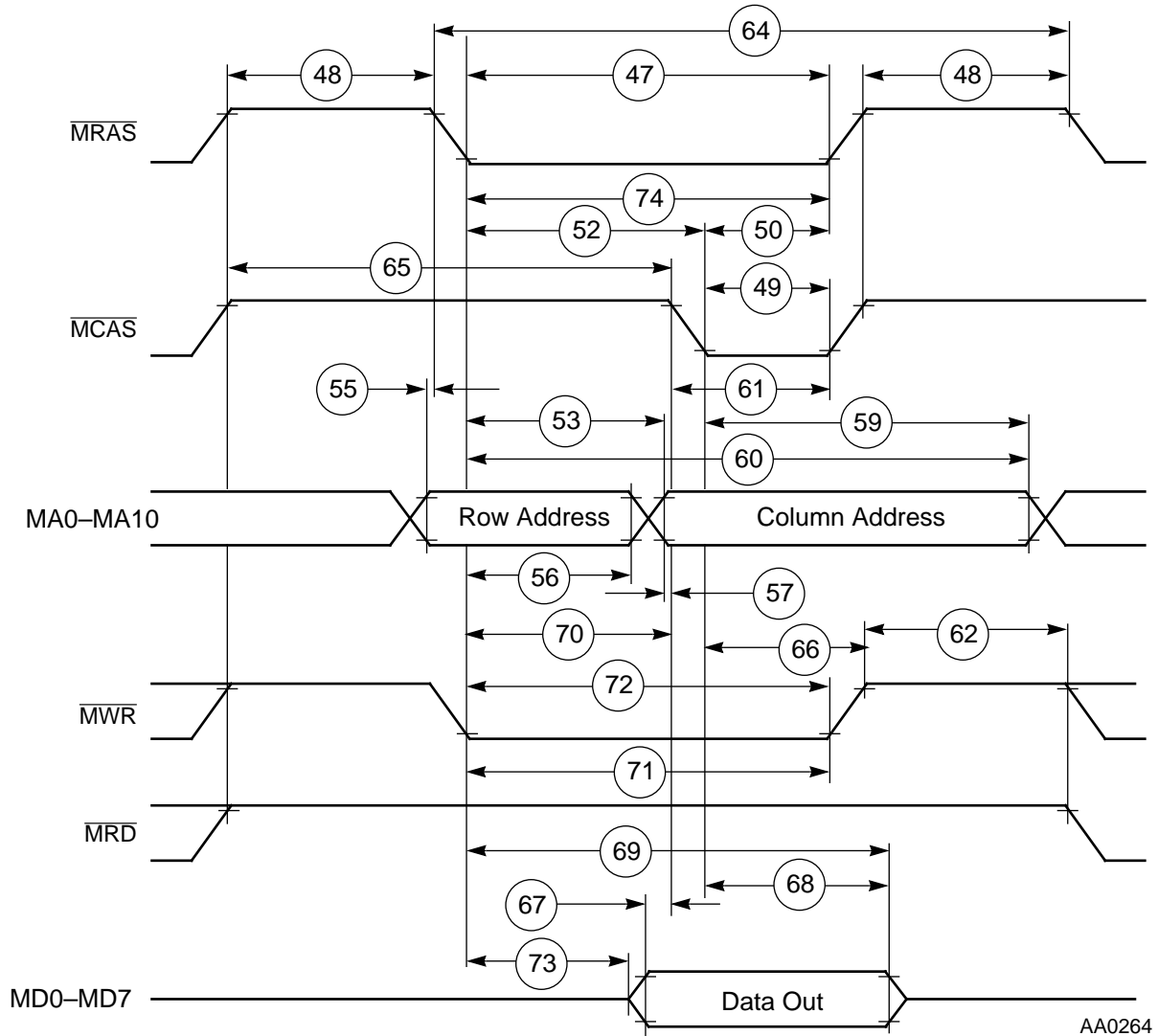


Figure 2-8 DRAM Single Read Cycle



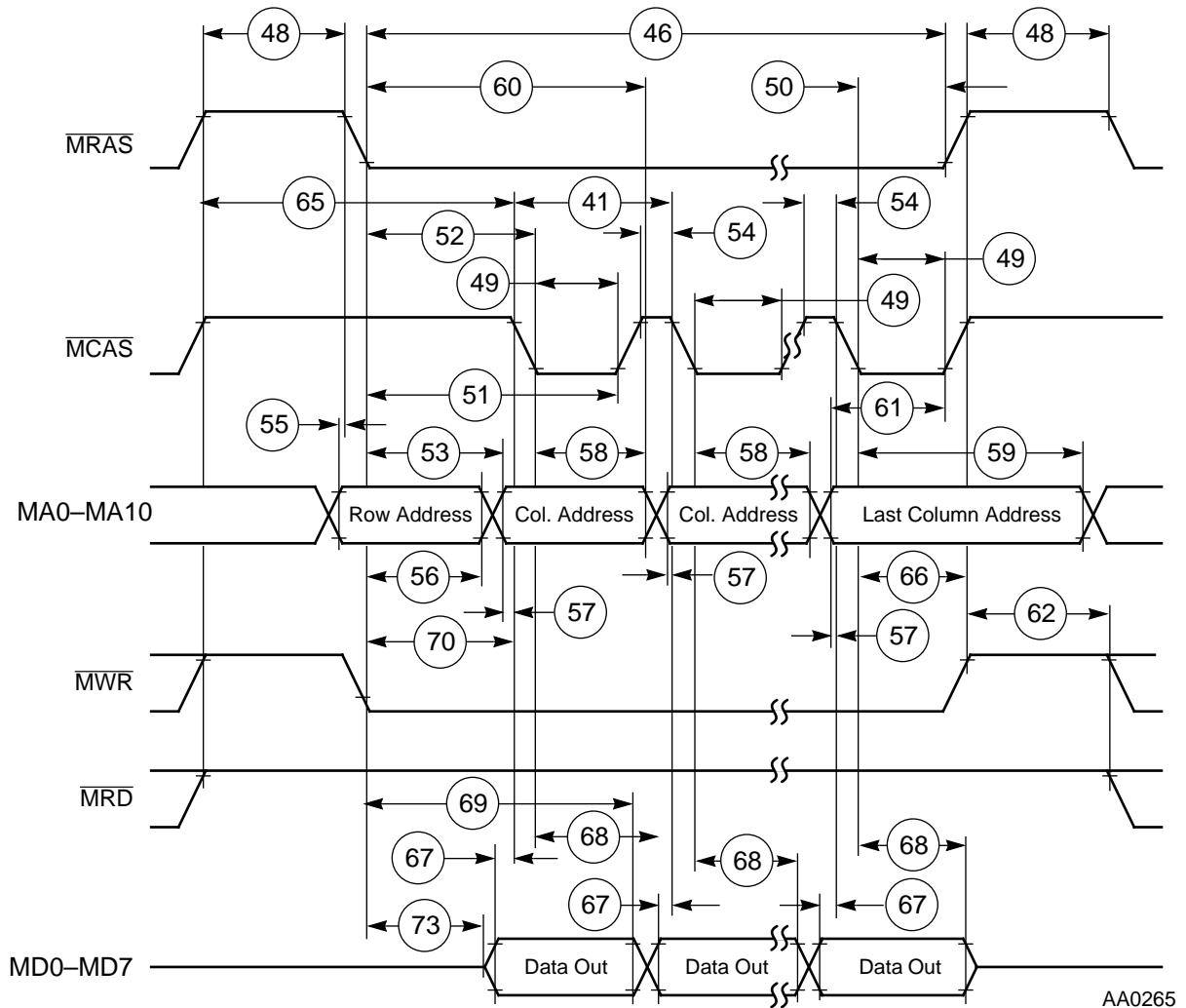
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Figure 2-9 DRAM Page Mode Read Cycle



AA0264

Figure 2-10 DRAM Single Write Cycle



AA0265

Figure 2-11 DRAM Page Mode Write Cycle

**EXTERNAL MEMORY INTERFACE (EMI) DRAM REFRESH TIMING**

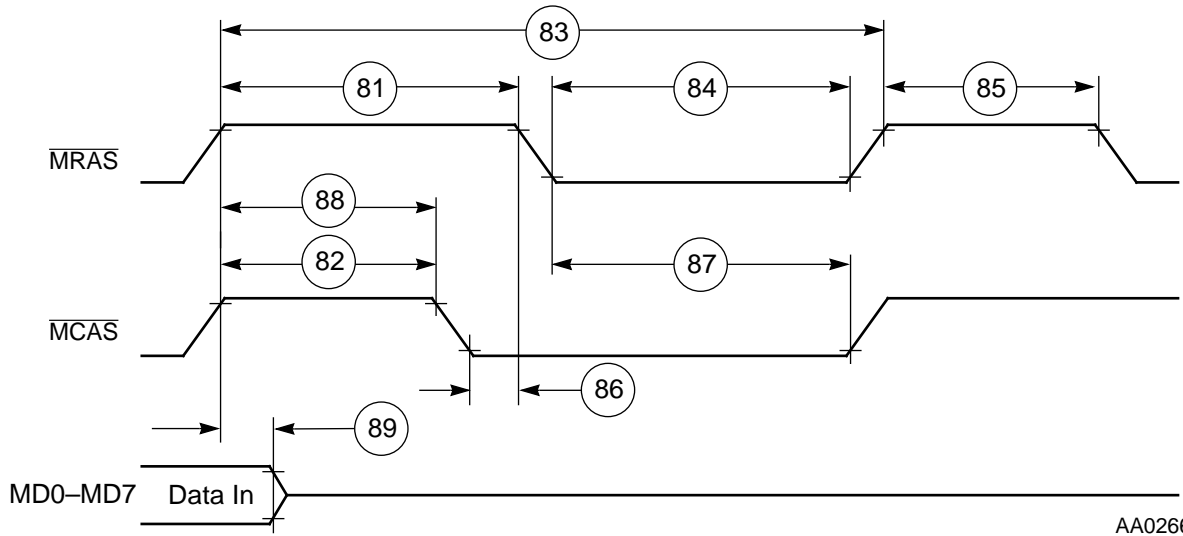
( $C_L = 50 \text{ pF} + 2 \text{ TTL Loads}$ )

**Table 2-9** External Memory Interface (EMI) DRAM Refresh Timing

No.	Characteristics	Sym.	Timing Mode	Exp.	50 MHz		66 MHz		81 MHz		Unit
					Min	Max	Min	Max	Min	Max	
81	$\overline{\text{RAS}}$ Deassertion to $\overline{\text{RAS}}$ Assertion	$t_{\text{RP}}$	slow fast	$6 \times T_C - 7$ $4 \times T_C - 7$	113	—	84	—	67.1	—	ns
					73	—	54	—	42.4	—	ns
82	$\overline{\text{CAS}}$ Deassertion to $\overline{\text{CAS}}$ Assertion	$t_{\text{CPN}}$	slow fast	$5 \times T_C - 7$ $3 \times T_C - 7$	93	—	71	—	54.7	—	ns
					53	—	38	—	30	—	ns
83	Refresh Cycle Time	$t_{\text{RC}}$	slow fast	$12 \times T_C$ $8 \times T_C$	240	—	181.8	—	148.2	—	ns
					160	—	121.2	—	98.8	—	ns
84	$\overline{\text{RAS}}$ Assertion Pulse Width	$t_{\text{RAS}}$	slow fast	$6 \times T_C - 9$ $4 \times T_C - 9$	111	—	81.9	—	65.1	—	ns
					71	—	51.6	—	40.4	—	ns
85	$\overline{\text{RAS}}$ Deassertion to $\overline{\text{RAS}}$ Assertion for Refresh Cycle <sup>1</sup>	$t_{\text{RP}}$	slow fast	$5 \times T_C - 5$ $3 \times T_C - 5$	95	—	70	—	55.7	—	ns
					55	—	40	—	32	—	ns
86	$\overline{\text{CAS}}$ Assertion to $\overline{\text{RAS}}$ Assertion on Refresh Cycle	$t_{\text{CSR}}$		$T_C - 7$	13	—	8	—	5.3	—	ns
87	$\overline{\text{RAS}}$ Assertion to $\overline{\text{CAS}}$ Deassertion on Refresh Cycle	$t_{\text{CHR}}$	slow fast	$6 \times T_C - 15$ $4 \times T_C - 15$	105	—	75.9	—	59.1	—	ns
					65	—	45.6	—	34.4	—	ns
88	$\overline{\text{RAS}}$ Deassertion to $\overline{\text{CAS}}$ Assertion on a Refresh Cycle	$t_{\text{RPC}}$	slow fast	$5 \times T_C - 11$ $3 \times T_C - 11$	89	—	65	—	50.7	—	ns
					49	—	34	—	26	—	ns
89	$\overline{\text{CAS}}$ Deassertion to Data Not Valid	$t_{\text{OFF}}$		0	0	—	0	—	0	—	ns

Note: 1. This happens when a Refresh Cycle is followed by an Access Cycle.





AA0266

Figure 2-12  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  Refresh Cycle

## EXTERNAL MEMORY INTERFACE (EMI) SRAM TIMING

( $C_L = 50 \text{ pF} + 2 \text{ TTL Loads}$ )

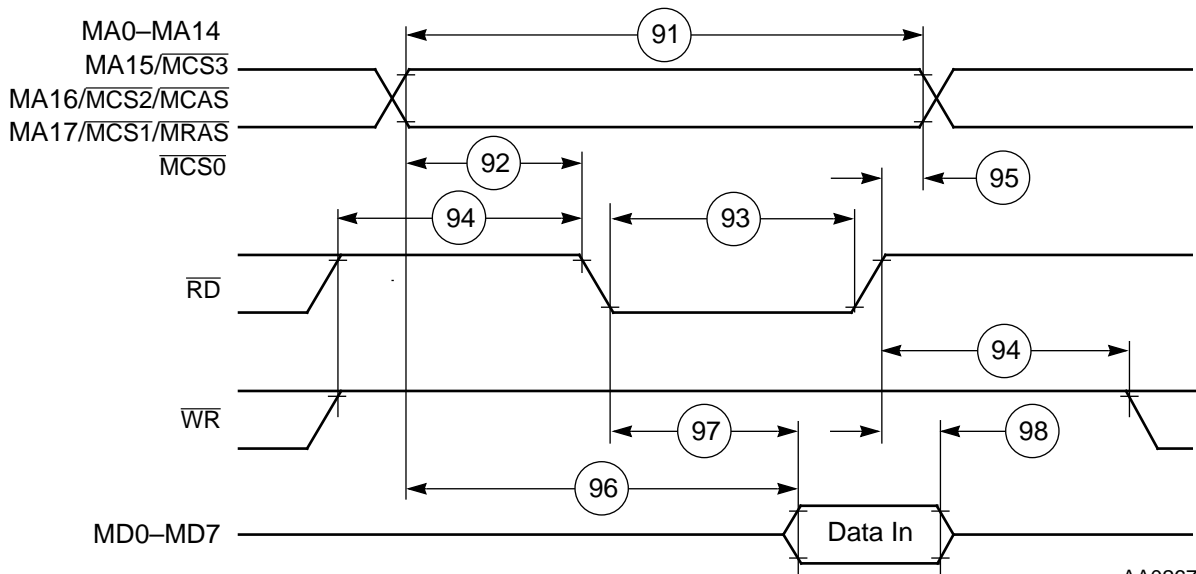
Table 2-10 External Memory Interface (EMI) SRAM Timing

No.	Characteristics	Symbol	Expression	50 MHz		66 MHz		81 MHz		Unit
				Min	Max	Min	Max	Min	Max	
91	Address Valid and $\overline{\text{CS}}$ Assertion Pulse Width	$t_{RC}, t_{WC}$	$4 \times T_C - 11 + W_s \times T_C$	69	—	50	—	38.4	—	ns
92	Address Valid to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ Assertion	$t_{AS}$	$T_C + T_L - 13$	17	—	10	—	5.5	—	ns
93	$\overline{\text{RD}}$ or $\overline{\text{WR}}$ Assertion Pulse Width	$t_{WP}$	$2 \times T_C - 5 + W_s \times T_C$	35	—	23	—	20	—	ns
94	$\overline{\text{RD}}$ or $\overline{\text{WR}}$ Deassertion to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ Assertion	—	$2 \times T_C - 11$	29	—	19	—	13.7	—	ns
95	$\overline{\text{RD}}$ or $\overline{\text{WR}}$ Deassertion to Address not Valid	$t_{WR}$	$T_H - 6$	4	—	2	—	0.2	—	ns
96	Address Valid to Input Data Valid	$t_{AA}, t_{AC}$	$3 \times T_C + T_L - 15 + W_s \times T_C$	—	55	—	38	—	28.2	ns
97	$\overline{\text{RD}}$ Assertion to Input Data Valid	$t_{OE}$	$2 \times T_C - 15 + W_s \times T_C$	—	25	—	15	—	9.7	ns

**Table 2-10** External Memory Interface (EMI) SRAM Timing

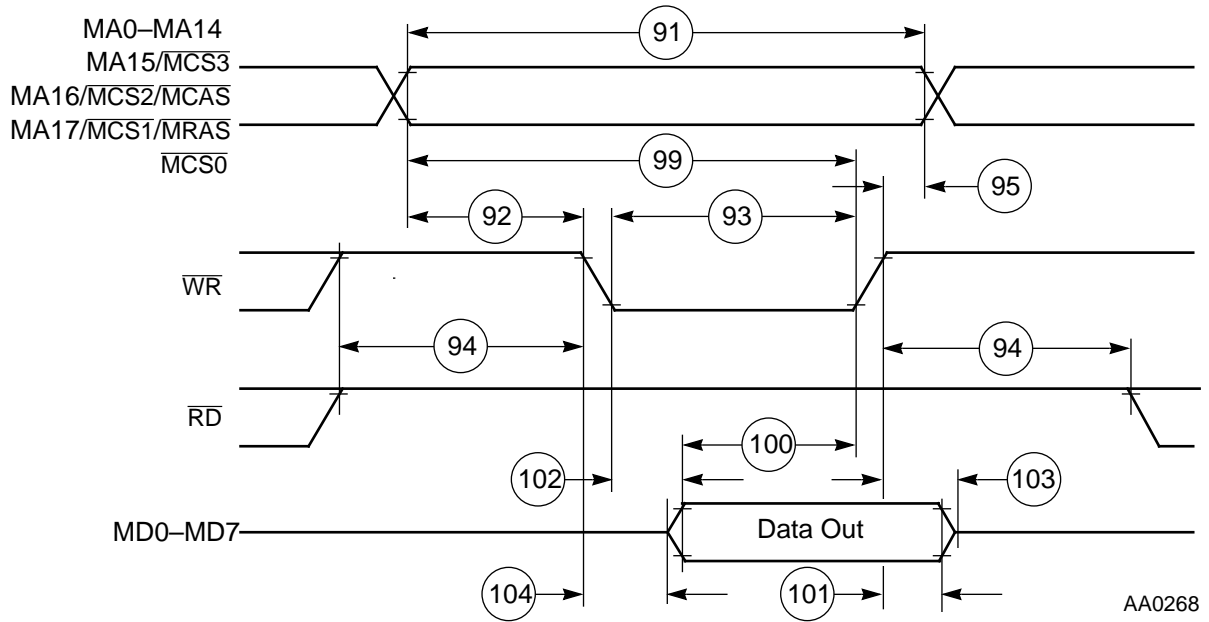
No.	Characteristics	Symbol	Expression	50 MHz		66 MHz		81 MHz		Unit
				Min	Max	Min	Max	Min	Max	
98	$\overline{RD}$ Deassertion to Data Not Valid (Data Hold Time)	$t_{OHZ}$	0	0	—	0	—	0	—	ns
99	Address Valid to $\overline{WR}$ Deassertion	$t_{CW}, t_{AW}$	$3 \times T_C + T_L - 14 + W_s \times T_C$	56	—	39	—	29.2	—	ns
100	Data Setup Time to $\overline{WR}$ Deassertion	$t_{DS} (t_{DW})$	$T_C + T_L - 5 + W_s \times T_C$	25	—	18	—	11.0	—	ns
101	Data Hold Time from $\overline{WR}$ Deassertion	$t_{DH}$	$T_H - 6$	4	—	2	—	0.2	—	ns
102	$\overline{WR}$ Assertion to Data Valid	—	$T_H + 4$	—	14	—	12	—	10.2	ns
103	$\overline{WR}$ Deassertion to Data high impedance <sup>1</sup>	—	$T_H + 10$	—	20	—	18	—	16.2	ns
104	$\overline{WR}$ Assertion to Data Active	—	$T_H - 6$	4	—	2	—	0.2	—	ns

Note: 1. This value is periodically sampled and not 100% tested.



**Figure 2-13** SRAM Read Cycle

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Figure 2-14 SRAM Write Cycle

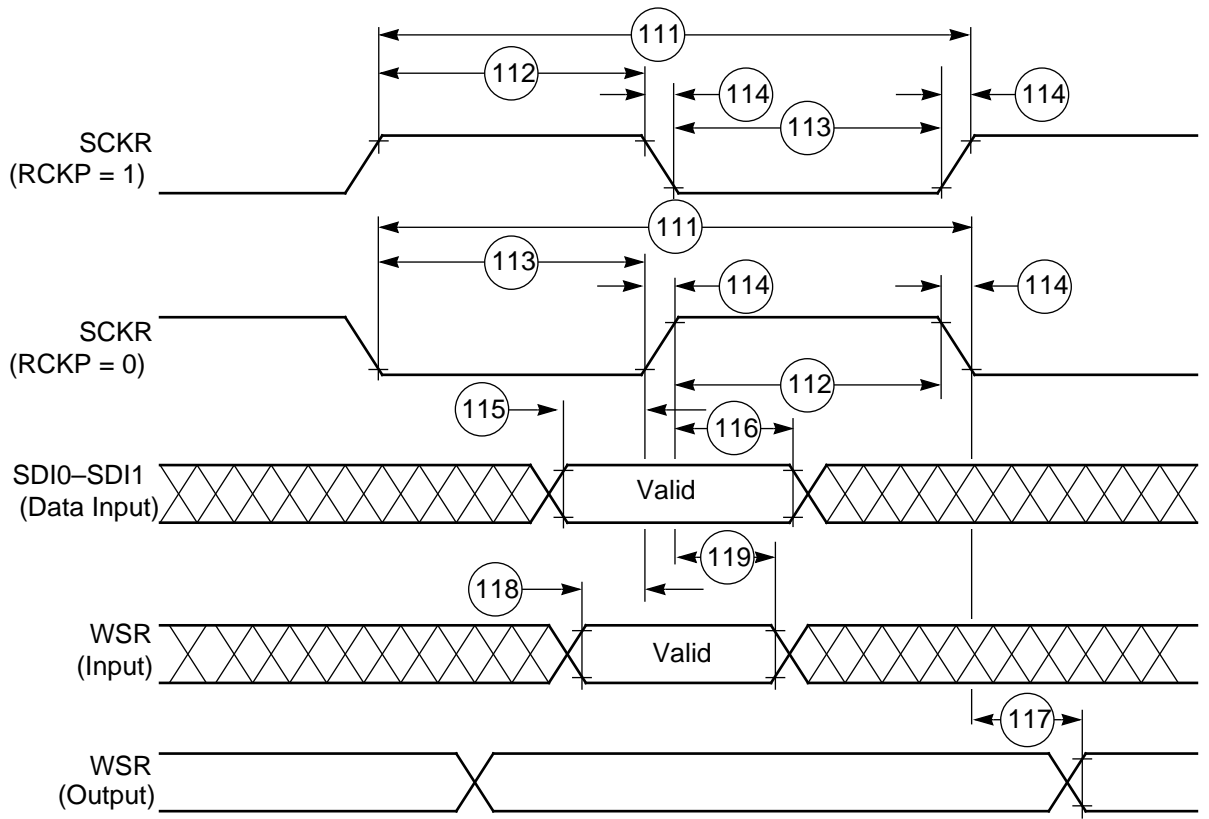
## SERIAL AUDIO INTERFACE (SAI) TIMING

( $C_L = 50 \text{ pF} + 2 \text{ TTL Loads}$ )

**Table 2-11** Serial Audio Interface (SAI) Timing

No.	Characteristics	Mode	Expression	50 MHz		66 MHz		81 MHz		Unit
				Min	Max	Min	Max	Min	Max	
111	Minimum Serial Clock Cycle = $t_{SAICC} \text{ (min)}$	master	$4 \times T_C$	80	—	61	—	49.4	—	ns
		slave	$3 \times T_C + 5$	65	—	51	—	42	—	ns
112	Serial Clock High Period	master	$0.5 \times t_{SAICC} - 8$	32	—	22	—	16.7	—	ns
		slave	$0.35 \times t_{SAICC}$	23	—	18	—	14.7	—	ns
113	Serial Clock Low Period	master	$0.5 \times t_{SAICC} - 8$	32	—	22	—	16.7	—	ns
		slave	$0.35 \times t_{SAICC}$	23	—	18	—	14.7	—	ns
114	Serial Clock Rise/Fall Time	master	8	—	8	—	8	—	8	ns
		slave	$0.15 \times t_{SAICC}$	—	10	—	8	—	6.3	ns
115	Data In Valid to SCKR edge (Data In Set-up Time)	master	26	26	—	26	—	26	—	ns
		slave	4	4	—	4	—	4	—	ns
116	SCKR Edge to Data In Not Valid (Data In Hold Time)	master	0	0	—	0	—	0	—	ns
		slave	14	14	—	14	—	14	—	ns
117	SCKR Edge to Word Select Out Valid (WSR Out Delay Time)	master	20	—	20	—	20	—	20	ns
118	Word Select In Valid to SCKR Edge (WSR In Set-up Time)	slave	12	12	—	12	—	12	—	ns
119	SCKR Edge to Word Select In Not Valid (WSR In Hold Time)	slave	12	12	—	12	—	12	—	ns
121	SCKT Edge to Data Out Valid (Data Out Delay Time)	master	13	—	13	—	13	—	13	ns
		slave <sup>1</sup>	40	—	40	—	40	—	40	ns
		slave <sup>2</sup>	$T_H + 34$	—	44	—	41	—	40.2	ns
122	SCKT Edge to Word Select Out Valid (WST Out Delay Time)	master	19	—	19	—	19	—	19	ns
123	Word Select In Valid to SCKT Edge (WST In Set-up Time)	slave	12	12	—	12	—	12	—	ns
124	SCKT Edge to Word Select In Not Valid (WST In Hold Time)	slave	12	12	—	12	—	12	—	ns

Note: 1. When the Frequency Ratio between Parallel and Serial clocks is 1:4 or greater  
 2. When the Frequency Ratio between Parallel and Serial clocks is 1:3 – 1:4



AA0269

Figure 2-15 SAI Receiver Timing

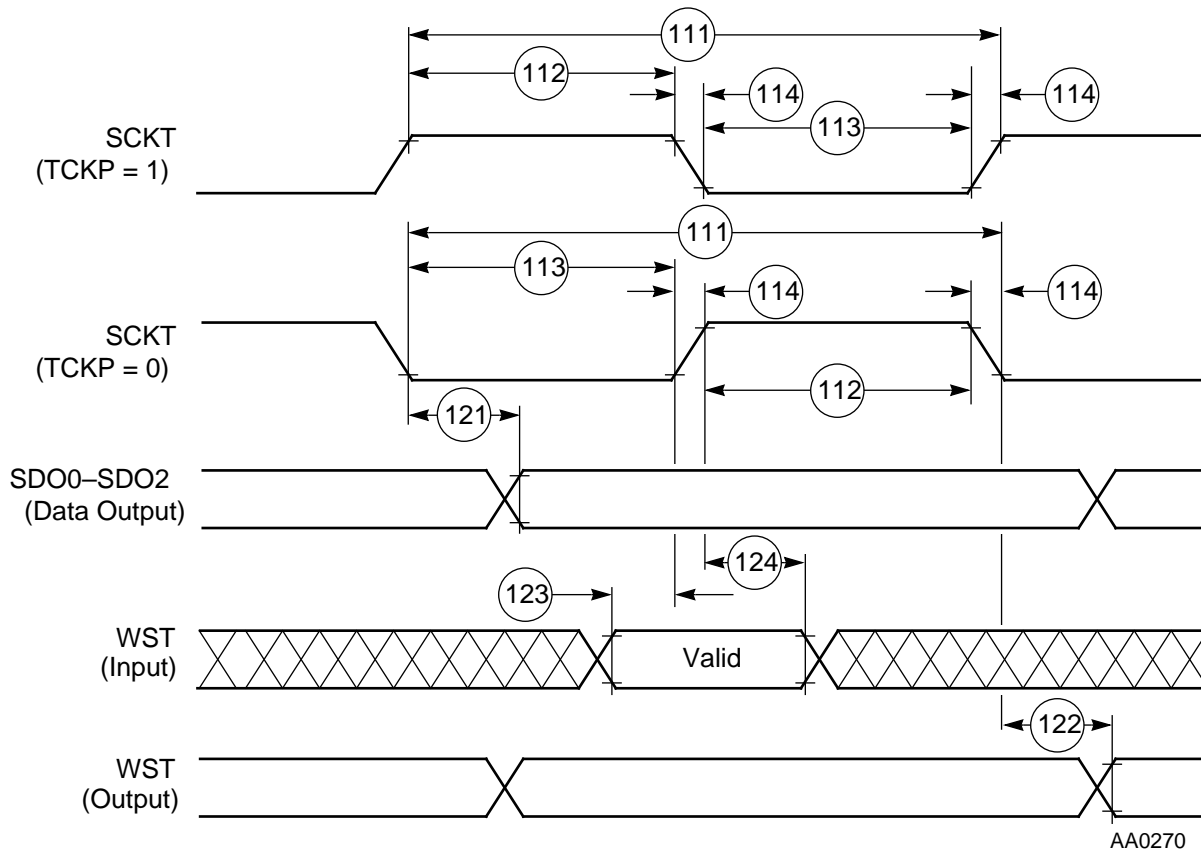


Figure 2-16 SAI Transmitter Timing

**SERIAL HOST INTERFACE (SHI) SPI PROTOCOL TIMING**

$(C_L = 50 \text{ pF}; V_{IHS} = 0.7 \times V_{CC}, V_{ILS} = 0.3 \times V_{CC})$

**Table 2-12** Serial Host Interface (SHI) SPI Protocol Timing

No.	Characteristics	Mode	Filter Mode	Expression	50 MHz		66 MHz		81 MHz		Unit	
					Min	Max	Min	Max	Min	Max		
	Tolerable Spike Width on Clock or Data In		bypassed narrow wide		— — —	0 20 100	— — —	0 20 100	— — —	0 20 100	ns ns ns	
141	Minimum Serial Clock Cycle = $t_{SPICC}(\text{min})$ For frequency below 33 MHz <sup>1</sup> For frequency above 33 MHz <sup>1</sup>	master	bypassed	$4 \times T_C$	—	—	—	—	—	—	ns	
			bypassed narrow wide	$6 \times T_C$ 1000 2000	120 1000 2000	— — —	91 1000 2000	— — —	74.1 1000 2000	— — —	ns ns ns	
	CPHA = 0, CPHA = 1 <sup>2</sup>	slave	bypassed narrow wide	$3 \times T_C$ $3 \times T_C + 25$ $3 \times T_C + 85$	60 85 145	— — —	45 70 130	— — —	37 62 122	— — —	ns ns ns	
			bypassed narrow wide	$3 \times T_C + 79$ $3 \times T_C + 431$ $3 \times T_C + 1022$	139 491 1082	— — —	124 476 1067	— — —	116 468 1059	— — —	ns ns ns	
	142	Serial Clock High Period CPHA = 0, CPHA = 1 <sup>2</sup>	master		$0.5 \times t_{SPICC} - 10$	50	—	35	—	27.0	—	ns
				slave	bypassed narrow wide	$T_C + 8$ $T_C + 31$ $T_C + 43$	28 51 63	— — —	23 46 58	— — —	20.3 43.3 55.3	— — —
		CPHA = 1	slave	bypassed narrow wide	$T_C + T_H + 40$ $T_C + T_H + 216$ $T_C + T_H + 511$	70 246 541	— — —	63 239 534	— — —	58.5 235 530	— — —	ns ns ns
				slave								
slave												
slave												
143	Serial Clock Low Period CPHA = 0, CPHA = 1 <sup>2</sup>	master		$0.5 \times t_{SPICC} - 10$	50	—	35	—	27.0	—	ns	
			slave	bypassed narrow wide	$T_C + 8$ $T_C + 31$ $T_C + 43$	28 51 63	— — —	23 46 58	— — —	20.3 43.3 55.3	— — —	ns ns ns
	CPHA = 1	slave	bypassed narrow wide	$T_C + T_H + 40$ $T_C + T_H + 216$ $T_C + T_H + 511$	70 246 541	— — —	63 239 534	— — —	58.5 235 550	— — —	ns ns ns	
			slave									
			slave									
			slave									
	144	Serial Clock Rise/Fall Time	master		10	—	10	—	10	—	10	ns
			slave		2000	—	2000	—	2000	—	2000	ns

**Table 2-12** Serial Host Interface (SHI) SPI Protocol Timing (Continued)

No.	Characteristics	Mode	Filter Mode	Expression	50 MHz		66 MHz		81 MHz		Unit
					Min	Max	Min	Max	Min	Max	
146	$\overline{SS}$ Assertion to First SCK Edge CPHA = 0	slave	bypassed	$T_C + T_H + 35$	65	—	58	—	53.5	—	ns
			narrow	$T_C + T_H + 35$	65	—	58	—	53.5	—	ns
			wide	$T_C + T_H + 35$	65	—	58	—	53.5	—	ns
	CPHA = 1	slave	bypassed	6	6	—	6	—	6	—	ns
			narrow	0	0	—	0	—	0	—	ns
			wide	0	0	—	0	—	0	—	ns
147	Last SCK Edge to $\overline{SS}$ Not Asserted CPHA = 0 CPHA = 1 <sup>3</sup>	slave	bypassed	$T_C + 6$	26	—	21	—	18.3	—	ns
			narrow	$T_C + 70$	90	—	85	—	82.4	—	ns
			wide	$T_C + 197$	217	—	212	—	209	—	ns
		slave	bypassed	2	2	—	2	—	2	—	ns
			narrow	66	66	—	66	—	66	—	ns
			wide	193	193	—	193	—	193	—	ns
148	Data In Valid to SCK Edge (Data In Set-up Time)	master	bypassed	0	0	—	0	—	0	—	ns
			narrow	$\text{MAX}\{(37 - T_C), 0\}$	17	—	22	—	25	—	ns
		slave	wide	$\text{MAX}\{(52 - T_C), 0\}$	32	—	37	—	40	—	ns
			bypassed	0	0	—	0	—	0	—	ns
			narrow	$\text{MAX}\{(38 - T_C), 0\}$	18	—	23	—	26	—	ns
			wide	$\text{MAX}\{(53 - T_C), 0\}$	33	—	38	—	41	—	ns
149	SCK Edge to Data In Not Valid (Data In Hold Time)	master	bypassed	$2 \times T_C + 17$	57	—	47	—	41.7	—	ns
			narrow	$2 \times T_C + 18$	58	—	48	—	42.7	—	ns
			wide	$2 \times T_C + 28$	68	—	58	—	52.7	—	ns
		slave	bypassed	$2 \times T_C + 17$	57	—	47	—	41.7	—	ns
			narrow	$2 \times T_C + 18$	58	—	48	—	42.7	—	ns
			wide	$2 \times T_C + 28$	68	—	58	—	52.7	—	ns
150	$\overline{SS}$ Assertion to Data Out Active	slave		4	—	4	—	4	—	ns	
151	$\overline{SS}$ Deassertion to Data high impedance <sup>4</sup>	slave		24	—	24	—	24	—	24	ns
152	SCK Edge to Data Out Valid (Data Out Delay Time) CPHA = 0, CPHA = 1 <sup>2</sup>	master	bypassed	41	—	41	—	41	—	41	ns
			narrow	214	—	214	—	214	—	214	ns
			wide	504	—	504	—	504	—	504	ns
		slave	bypassed	41	—	41	—	41	—	41	ns
			narrow	214	—	214	—	214	—	214	ns
			wide	504	—	504	—	504	—	504	ns
	CPHA = 1	slave	bypassed	$T_C + T_H + 40$	—	70	—	63	—	58.5	ns
			narrow	$T_C + T_H + 216$	—	246	—	239	—	235	ns
			wide	$T_C + T_H + 511$	—	541	—	534	—	530	ns



Table 2-12 Serial Host Interface (SHI) SPI Protocol Timing (Continued)

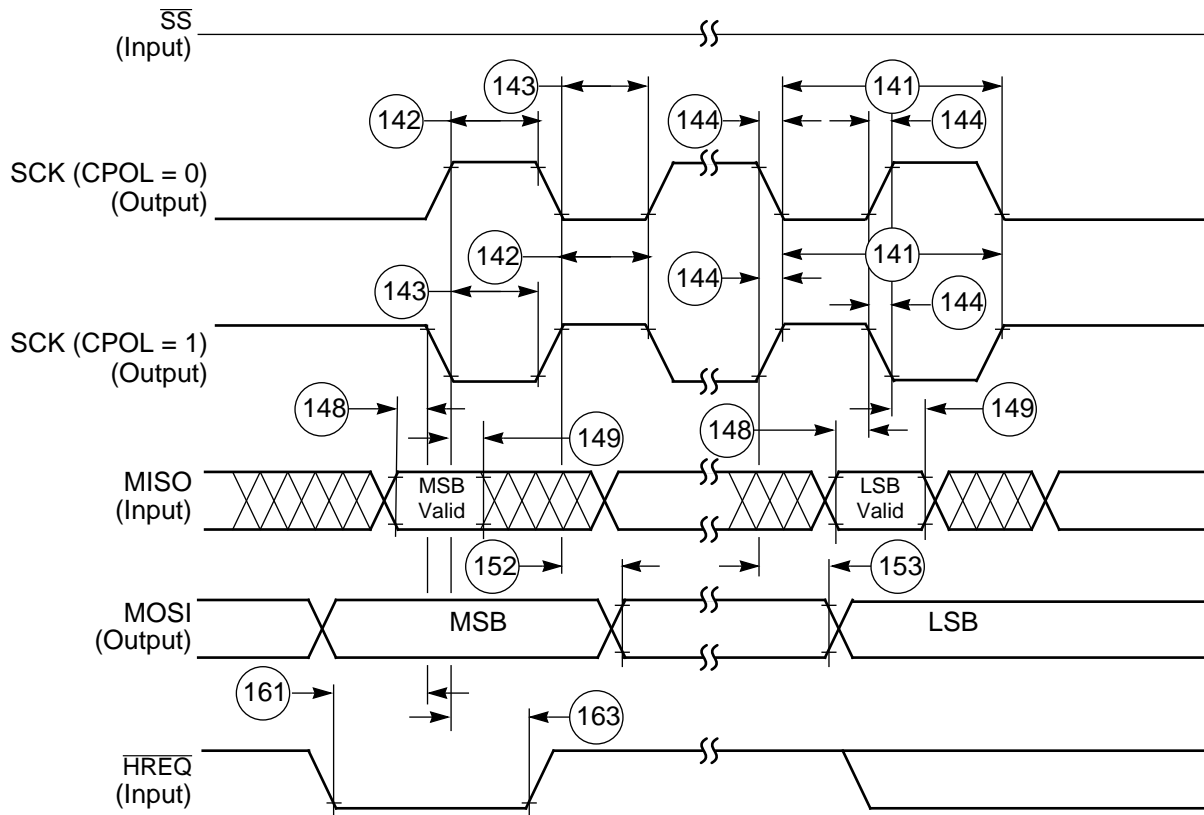
No.	Characteristics	Mode	Filter Mode	Expression	50 MHz		66 MHz		81 MHz		Unit
					Min	Max	Min	Max	Min	Max	
153	SCK Edge to Data Out Not Valid (Data Out Hold Time)	master	bypassed	0	0	—	0	—	0	—	ns
			narrow	57	57	—	57	—	57	—	ns
			wide	163	163	—	163	—	163	—	ns
		slave	bypassed	0	0	—	0	—	0	—	ns
			narrow	57	57	—	57	—	57	—	ns
			wide	163	163	—	163	—	163	—	ns
154	$\overline{SS}$ Assertion to Data Out Valid CPHA = 0	slave		$T_C + T_H + 35$	—	65	—	58	—	53.5	ns
157	First SCK Sampling Edge to HREQ Output Deassertion	slave	bypassed	$3 \times T_C + T_H + 32$	—	102	—	85	—	75	ns
			narrow	$3 \times T_C + T_H + 209$	—	279	—	262	—	252	ns
			wide	$3 \times T_C + T_H + 507$	—	577	—	560	—	550	ns
158	Last SCK Sampling Edge to HREQ Output Not Deasserted CPHA = 1	slave	bypassed	$2 \times T_C + T_H + 6$	56	—	44	—	36.9	—	ns
			narrow	$2 \times T_C + T_H + 63$	113	—	101	—	93.9	—	ns
			wide	$2 \times T_C + T_H + 169$	219	—	207	—	200	—	ns
159	$\overline{SS}$ Deassertion to HREQ Output Not Deasserted CPHA = 0	slave		$2 \times T_C + T_H + 7$	57	—	45	—	37.9	—	ns
160	$\overline{SS}$ Deassertion Pulse Width CPHA = 0	slave		$T_C + 4$	24	—	19	—	16.3	—	ns
161	HREQ In Assertion to First SCK Edge	master		$0.5 \times t_{SPICCC} + 2 \times T_C + 6$	106	—	82	—	67.7	—	ns
162	HREQ In Deassertion to Last SCK Sampling Edge (HREQ In Set-up Time) CPHA = 1	master		0	0	—	0	—	0	—	ns

**Table 2-12** Serial Host Interface (SHI) SPI Protocol Timing (Continued)

No.	Characteristics	Mode	Filter Mode	Expression	50 MHz		66 MHz		81 MHz		Unit
					Min	Max	Min	Max	Min	Max	
163	First SCK Edge to HREQ In Not Asserted (HREQ In Hold Time)	master		0	0	—	0	—	0	—	ns

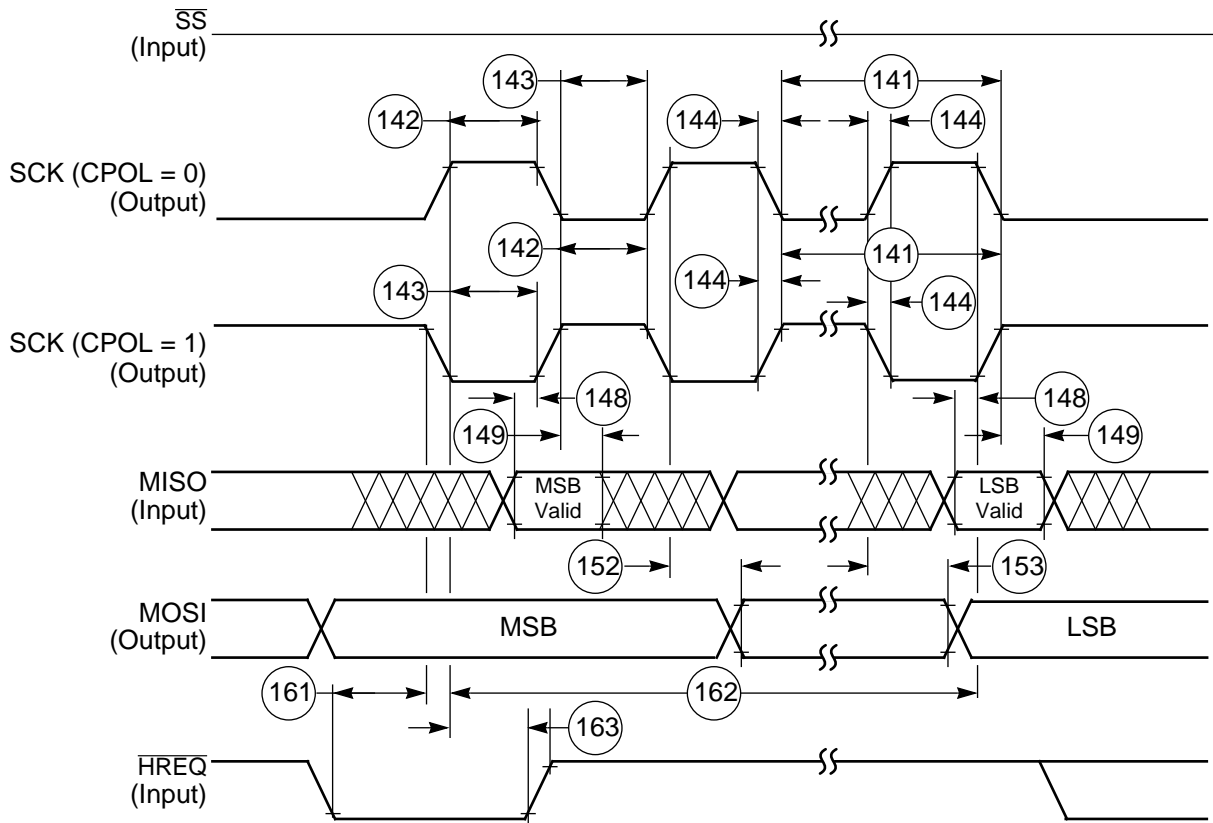
Note:

1. For an Internal Clock frequency below 33 MHz, the minimum permissible Internal Clock to Serial Clock frequency ratio is 4:1. For an Internal Clock frequency above 33 MHz, the minimum permissible Internal Clock to Serial Clock frequency ratio is 6:1.
2. In CPHA = 1 mode, the SPI slave supports data transfers at  $t_{SPICC} = 3 \times T_C$ , if the user assures that the HTX is written at least  $T_C$  ns before the first edge of SCK of each word. In CPHA = 1 mode, the SPI slave supports data transfers at  $t_{SPICC} = 3 \times T_C$ , if the user assures that the HTX is written at least  $T_C$  ns before the first edge of SCK of each word.
3. When CPHA = 1, the  $\overline{SS}$  line may remain active low between successive transfers.
4. Periodically sampled, not 100% tested



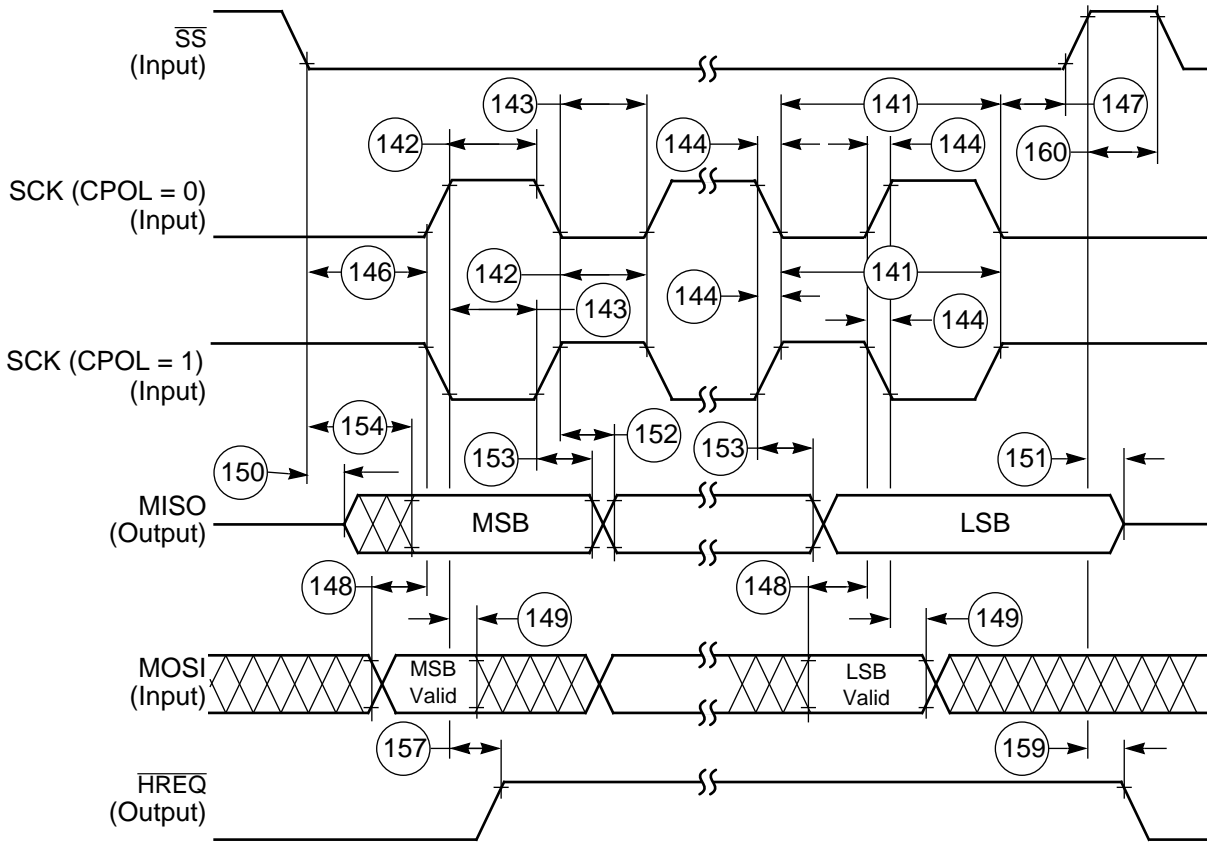
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**Figure 2-17** SPI Master Timing (CPHA = 0)



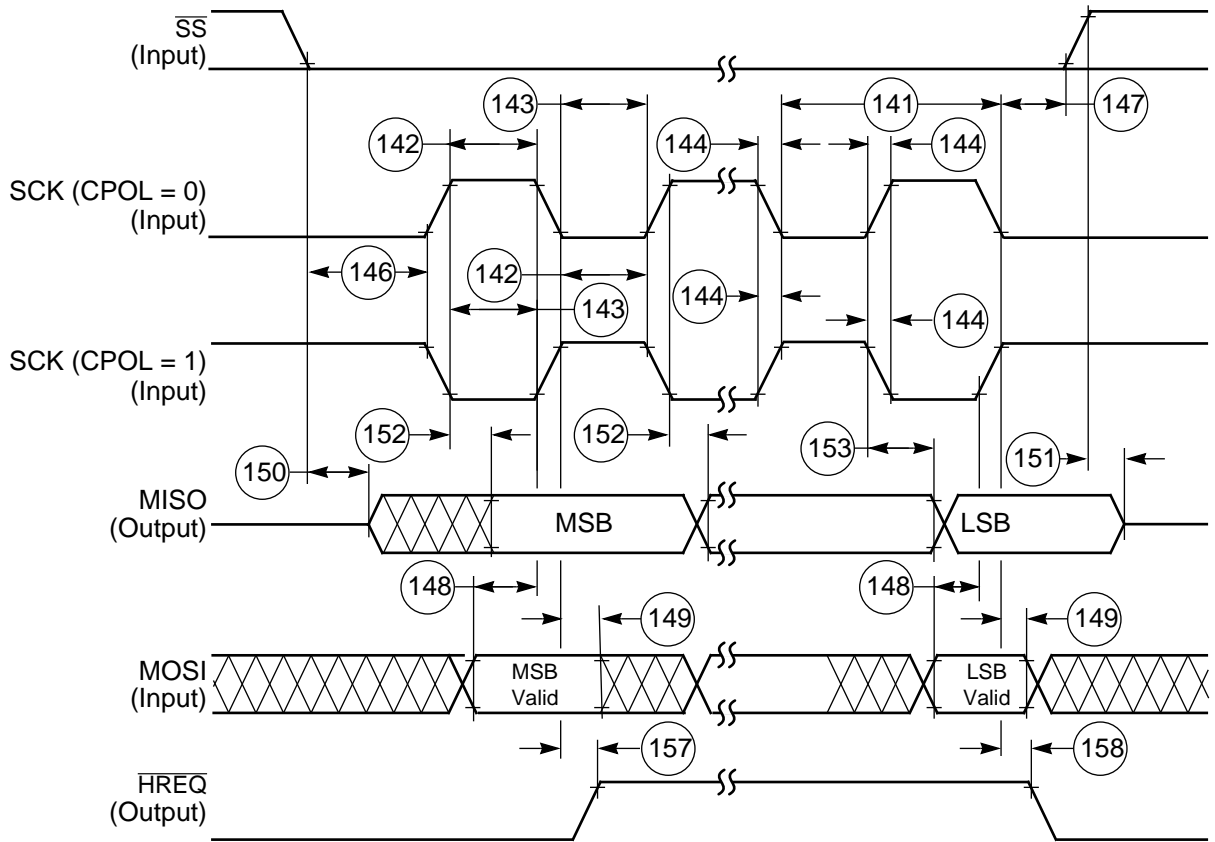
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Figure 2-18 SPI Master Timing (CPHA = 1)



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Figure 2-19 SPI Slave Timing (CPHA = 0)



AA0274

Figure 2-20 SPI Slave Timing (CPHA = 1)

**SERIAL HOST INTERFACE (SHI) I<sup>2</sup>C PROTOCOL TIMING**

$$(V_{IHS} = 0.7 \times V_{CC}, V_{ILS} = 0.3 \times V_{CC})$$

$$(V_{OHS} = 0.8 \times V_{CC}, V_{OLS} = 0.2 \times V_{CC})$$

$$(R_P (\text{min}) = 1.5 \text{ k}\Omega)$$

**Table 2-13** SHI I<sup>2</sup>C Protocol Timing

Standard I <sup>2</sup> C (C <sub>L</sub> = 400 pF, R <sub>P</sub> = 2 kΩ, 100 kHz)					
No.	Characteristics	Symbol	All frequencies		Unit
			Min	Max	
—	Tolerable Spike Width on SCL or SDA Filters Bypassed		—	0	ns
	Narrow Filters Enabled		—	20	ns
	Wide Filters Enabled		—	100	ns
171	Minimum SCL Serial Clock Cycle	t <sub>SCL</sub>	10.0	—	μs
172	Bus Free Time	t <sub>BUF</sub>	4.7	—	μs
173	Start Condition Set-up Time	t <sub>SU;STA</sub>	4.7	—	μs
174	Start Condition Hold Time	t <sub>HD;STA</sub>	4.0	—	μs
175	SCL Low Period	t <sub>LOW</sub>	4.7	—	μs
176	SCL High Period	t <sub>HIGH</sub>	4.0	—	μs
177	SCL and SDA Rise Time	t <sub>r</sub>	—	1.0	μs
178	SCL and SDA Fall Time	t <sub>f</sub>	—	0.3	μs
179	Data Set-up Time	t <sub>SU;DAT</sub>	250	—	ns
180	Data Hold Time	t <sub>HD;DAT</sub>	0.0	—	ns
182	SCL Low to Data Out Valid	t <sub>VD;DAT</sub>	—	3.4	μs
183	Stop Condition Set-up Time	t <sub>SU;STO</sub>	4.0	—	μs
<b>Note:</b>	Refer to the <i>DSP56004 User's Manual</i> for a detailed description of how to use the different filtering modes.				

The Programmed Serial Clock Cycle,  $t_{I^2C_{CCP}}$ , is specified by the value of the HDM5–HDM0 and HRS bits of the HCKR (SHI Clock control Register).

The expression for  $t_{I^2C_{CCP}}$  is:

$$t_{I^2C_{CCP}} = [T_C \times 2 \times (HDM[5:0] + 1) \times (7 \times (1 - HRS) + 1)]$$

where

- HRS is the Prescaler Rate Select bit. When HRS is cleared, the fixed divide-by-eight prescaler is operational. When HRS is set, the prescaler is bypassed.
- HDM5–HDM0 are the Divider Modulus Select bits.
- A divide ratio from 1 to 64 (HDM5–HDM0 = 0 to \$3F) may be selected.

In I<sup>2</sup>C mode, you may select a value for the Programmed Serial Clock Cycle from  $6 \times T_C$  (HDM5–HDM0 = 2, HRS = 1) to  $1024 \times T_C$  (HDM5–HDM0 = \$3F, HRS = 0).

The DSP56004 provides an improved I<sup>2</sup>C bus protocol. In addition to supporting the 100 kHz I<sup>2</sup>C bus protocol, the SHI in I<sup>2</sup>C mode supports data transfers at up to 1000 kHz. The actual maximum frequency is limited by the bus capacitances ( $C_L$ ), the pull-up resistors ( $R_p$ ), (which affect the rise and fall time of SDA and SCL, (see table below)), and by the input filters.

Consideration for programming the SHI Clock Control Register (HCKR) – Clock Divide Ratio: the master must generate a bus free time greater than T172 slave when operating with a DSP56004 SHI I<sup>2</sup>C slave.

The table below describes a few examples:

**Table 2-14** Considerations for Programming the SHI Clock control Register (HCKR)

Conditions to be Considered						Resulting Limitations		
Bus Load	Master Operating Freq.	Slave Operating Freq.	Master Filter Mode	Slave Filter Mode	T172 Slave	Min. Permissible $t_{I^2C_{CCP}}$	T172 Master	Maximum I <sup>2</sup> C Serial Frequency
$C_L = 50 \text{ pF}$ , $R_p = 2 \text{ k}\Omega$	81 MHz	81 MHz	Bypassed	Bypassed	36 ns	$52 \times T_C$	41 ns	1010 kHz
			Narrow	Narrow	60 ns	$56 \times T_C$	66 ns	825 kHz
			Wide	Wide	95 ns	$62 \times T_C$	103 ns	634 kHz

**Example:** for  $C_L = 50$  pF,  $R_P = 2$  k $\Omega$ ,  $f = 88$  MHz, Bypassed Filter mode: The master, when operating with a DSP56004 SHI I<sup>2</sup>C slave with an 88 MHz operating frequency, must generate a bus free time greater than 36 ns (T172 slave). Thus, the minimum permissible  $t_{I^2C_{CCP}}$  is  $56 \times T_C$  which gives a bus free time of at least 41 ns (T172 master). This implies a maximum I<sup>2</sup>C serial frequency of 1010 kHz.

In general, bus performance may be calculated from the  $C_L$  and  $R_P$  of the bus, the Input Filter modes and operating frequencies of the master and the slave. **Table 2-15** contains the expressions required to calculate all relevant performance timing for a given  $C_L$  and  $R_P$ .

**Table 2-15** SHI Improved I<sup>2</sup>C Protocol Timing

Improved I <sup>2</sup> C ( $C_L = 50$ pF, $R_P = 2$ k $\Omega$ )												
No.	Char.	Sym.	Mode	Filter Mode	Expression	50 MHz <sup>2</sup>		66 MHz <sup>3</sup>		81 MHz <sup>4</sup>		Unit
						Min	Max	Min	Max	Min	Max	
—	Tolerable Spike Width on SCL or SDA			bypassed	0	—	0	—	0	—	0	ns
				narrow	20	—	20	—	20	—	20	ns
				wide	100	—	100	—	100	—	100	ns
171	SCL Serial Clock Cycle	$t_{SCL}$	master	bypassed	$t_{I^2C_{CCP}} + 3 \times T_C + 72 + t_r$	1050	—	1007	—	989	—	ns
				narrow	$t_{I^2C_{CCP}} + 3 \times T_C + 245 + t_r$	1263	—	1225	—	1212	—	ns
				wide	$t_{I^2C_{CCP}} + 3 \times T_C + 535 + t_r$	1593	—	1591	—	1576	—	ns
			slave	bypassed	$4 \times T_C + T_H + 172 + t_r$	500	—	478	—	466	—	ns
				narrow	$4 \times T_C + T_H + 366 + t_r$	694	—	672	—	660	—	ns
				wide	$4 \times T_C + T_H + 648 + t_r$	976	—	954	—	942	—	ns
172	Bus Free Time	$t_{BUF}$	master	bypassed	$0.5 \times t_{I^2C_{CCP}} - 42 - t_r$	60	—	46	—	41.1	—	ns
				narrow	$0.5 \times t_{I^2C_{CCP}} - 42 - t_r$	80	—	68	—	65.8	—	ns
				wide	$0.5 \times t_{I^2C_{CCP}} - 42 - t_r$	100	—	102	—	103	—	ns
			slave	bypassed	$2 \times T_C + 11$	51	—	41	—	35.7	—	ns
				narrow	$2 \times T_C + 35$	75	—	65	—	59.7	—	ns
				wide	$2 \times T_C + 70$	110	—	100	—	94.7	—	ns
173	Start Condition Set-up Time	$t_{SU;STA}$	slave	bypassed	12	12	—	12	—	12	—	ns
				narrow	50	50	—	50	—	50	—	ns
				wide	150	150	—	150	—	150	—	ns



Table 2-15 SHI Improved I<sup>2</sup>C Protocol Timing (Continued)

Improved I <sup>2</sup> C (C <sub>L</sub> = 50 pF, R <sub>p</sub> = 2 kΩ)												
No.	Char.	Sym.	Mode	Filter Mode	Expression	50 MHz <sup>2</sup>		66 MHz <sup>3</sup>		81 MHz <sup>4</sup>		Unit
						Min	Max	Min	Max	Min	Max	
174	Start Condition Hold Time	t <sub>HD;STA</sub>	master	bypassed	$0.5 \times t_{FCCP} + 12 - t_f$	332	—	318	—	313	—	ns
				narrow	$0.5 \times t_{FCCP} + 12 - t_f$	352	—	340	—	338	—	ns
				wide	$0.5 \times t_{FCCP} + 12 - t_f$	372	—	378	—	375	—	ns
			slave	bypassed	$2 \times T_C + T_H + 21$	71	—	59	—	51.9	—	ns
				narrow	$2 \times T_C + T_H + 100$	150	—	138	—	131	—	ns
				wide	$2 \times T_C + T_H + 200$	250	—	238	—	231	—	ns
175	SCL Low Period	t <sub>LOW</sub>	master	bypassed	$0.5 \times t_{FCCP} + 18 - t_f$	338	—	324	—	319	—	ns
				narrow	$0.5 \times t_{FCCP} + 18 - t_f$	358	—	346	—	344	—	ns
				wide	$0.5 \times t_{FCCP} + 18 - t_f$	378	—	384	—	381	—	ns
			slave	bypassed	$2 \times T_C + 74 + t_r$	352	—	342	—	337	—	ns
				narrow	$2 \times T_C + 286 + t_r$	564	—	554	—	536	—	ns
				wide	$2 \times T_C + 586 + t_r$	864	—	854	—	849	—	ns
176	SCL High Period	t <sub>HIGH</sub>	master	bypassed	$0.5 \times t_{FCCP} + 2 \times T_C + 19$	379	—	375	—	365	—	ns
				narrow	$0.5 \times t_{FCCP} + 2 \times T_C + 144$	544	—	523	—	514	—	ns
				wide	$0.5 \times t_{FCCP} + 2 \times T_C + 356$	776	—	773	—	763	—	ns
			slave	bypassed	$2 \times T_C + T_H - 1$	49	—	37	—	30	—	ns
				narrow	$2 \times T_C + T_H + 18$	68	—	56	—	49	—	ns
				wide	$2 \times T_C + T_H + 30$	80	—	68	—	61	—	ns
177	SCL Rise Time Output <sup>1</sup>	t <sub>r</sub>			$1.7 \times R_p \times (C_L + 20) / 2000$	—	238	—	238	—	238	ns
	Input					—	2000	—	2000	—	2000	ns
178	SCL Fall Time Output <sup>1</sup>	t <sub>f</sub>			$20 + 0.1 \times (C_L - 50) / 2000$	—	20	—	20	—	20	ns
	Input					—	2000	—	2000	—	2000	ns
179	Data Set-up Time	t <sub>SU;DAT</sub>		bypassed	T <sub>C</sub> + 8	28	—	23	—	20	—	ns
				narrow	T <sub>C</sub> + 60	80	—	75	—	72	—	ns
				wide	T <sub>C</sub> + 74	94	—	89	—	86	—	ns

**Table 2-15 SHI Improved I<sup>2</sup>C Protocol Timing (Continued)**

Improved I <sup>2</sup> C (C <sub>L</sub> = 50 pF, R <sub>p</sub> = 2 kΩ)												
No.	Char.	Sym.	Mode	Filter Mode	Expression	50 MHz <sup>2</sup>		66 MHz <sup>3</sup>		81 MHz <sup>4</sup>		Unit
						Min	Max	Min	Max	Min	Max	
180	Data Hold Time	t <sub>HD;DAT</sub>		bypassed	0	0	—	0	—	0	—	ns
				narrow	0	0	—	0	—	0	—	ns
				wide	0	0	—	0	—	0	—	ns
182	SCL Low to Data Out Valid	t <sub>VD;DAT</sub>		bypassed	2 × T <sub>C</sub> + 71 + t <sub>r</sub>	—	349	—	339	—	344	ns
				narrow	2 × T <sub>C</sub> + 244 + t <sub>r</sub>	—	522	—	512	—	507	ns
				wide	2 × T <sub>C</sub> + 535 + t <sub>r</sub>	—	813	—	803	—	798	ns
183	Stop Condition Set-up Time	t <sub>SU;STO</sub>	master	bypassed	0.5 × t <sub>rCCP</sub> + T <sub>C</sub> + T <sub>H</sub> + 11	381	—	359	—	351	—	ns
				narrow	0.5 × t <sub>rCCP</sub> + T <sub>C</sub> + T <sub>H</sub> + 69	459	—	440	—	433	—	ns
				wide	0.5 × t <sub>rCCP</sub> + T <sub>C</sub> + T <sub>H</sub> + 183	613	—	592	—	584	—	ns
			slave	bypassed	11	11	—	11	—	11	—	ns
				narrow	50	50	—	50	—	50	—	ns
				wide	150	150	—	150	—	150	—	ns
184	HREQ In Deassertion to Last SCL Edge (HREQ In Set-up Time)		master	bypassed	0	0	—	0	—	0	—	ns
				narrow	0	0	—	0	—	0	—	ns
				wide	0	0	—	0	—	0	—	ns
186	First SCL Sampling Edge to HREQ Output Deassertion		slave	bypassed	3 × T <sub>C</sub> + T <sub>H</sub> + 32	—	102	—	85	—	75	ns
				narrow	3 × T <sub>C</sub> + T <sub>H</sub> + 209	—	279	—	262	—	252	ns
				wide	3 × T <sub>C</sub> + T <sub>H</sub> + 507	—	577	—	560	—	550	ns
187	Last SCL Edge to HREQ Output Not Deasserted		slave	bypassed	2 × T <sub>C</sub> + T <sub>H</sub> + 6	56	—	44	—	37	—	ns
				narrow	2 × T <sub>C</sub> + T <sub>H</sub> + 63	113	—	101	—	93.9	—	ns
				wide	2 × T <sub>C</sub> + T <sub>H</sub> + 169	219	—	207	—	200	—	ns
188	HREQ In Assertion to First SCL Edge		master	bypassed	t <sub>rCCP</sub> + 2 × T <sub>C</sub> + 6	726	—	688	—	673	—	ns
				narrow	t <sub>rCCP</sub> + 2 × T <sub>C</sub> + 6	766	—	733	—	722	—	ns
				wide	t <sub>rCCP</sub> + 2 × T <sub>C</sub> + 6	846	—	809	—	796	—	ns

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Table 2-15 SHI Improved I<sup>2</sup>C Protocol Timing (Continued)

Improved I <sup>2</sup> C (C <sub>L</sub> = 50 pF, R <sub>p</sub> = 2 kΩ)												
No.	Char.	Sym.	Mode	Filter Mode	Expression	50 MHz <sup>2</sup>		66 MHz <sup>3</sup>		81 MHz <sup>4</sup>		Unit
						Min	Max	Min	Max	Min	Max	
189	First SCL Edge to $\overline{\text{HREQ}}$ In Not Asserted ( $\overline{\text{HREQ}}$ In Hold Time)		master		0	0	—	0	—	0	—	ns

- Note:
- C<sub>L</sub> is in pF, R<sub>p</sub> is in kΩ, and result is in ns.
  - A t<sub>FCCP</sub> of 34 × T<sub>C</sub> (the maximum permitted for the given bus load) was used for the calculations in the Bypassed Filter mode.  
A t<sub>FCCP</sub> of 36 × T<sub>C</sub> (the maximum permitted for the given bus load) was used for the calculations in the Narrow Filter mode.  
A t<sub>FCCP</sub> of 40 × T<sub>C</sub> (the maximum permitted for the given bus load) was used for the calculations in the Wide Filter mode.
  - A t<sub>FCCP</sub> of 43 × T<sub>C</sub> (the maximum permitted for the given bus load) was used for the calculations in the Bypassed Filter mode.  
A t<sub>FCCP</sub> of 46 × T<sub>C</sub> (the maximum permitted for the given bus load) was used for the calculations in the Narrow Filter mode.  
A t<sub>FCCP</sub> of 51 × T<sub>C</sub> (the maximum permitted for the given bus load) was used for the calculations in the Wide Filter mode.
  - A t<sub>FCCP</sub> of 52 × T<sub>C</sub> (the maximum permitted for the given bus load) was used for the calculations in the Bypassed Filter mode.  
A t<sub>FCCP</sub> of 56 × T<sub>C</sub> (the maximum permitted for the given bus load) was used for the calculations in the Narrow Filter mode.  
A t<sub>FCCP</sub> of 62 × T<sub>C</sub> (the maximum permitted for the given bus load) was used for the calculations in the Wide Filter mode.
  - Refer to the *DSP56004 User's Manual* for a detailed description of how to use the filtering modes.

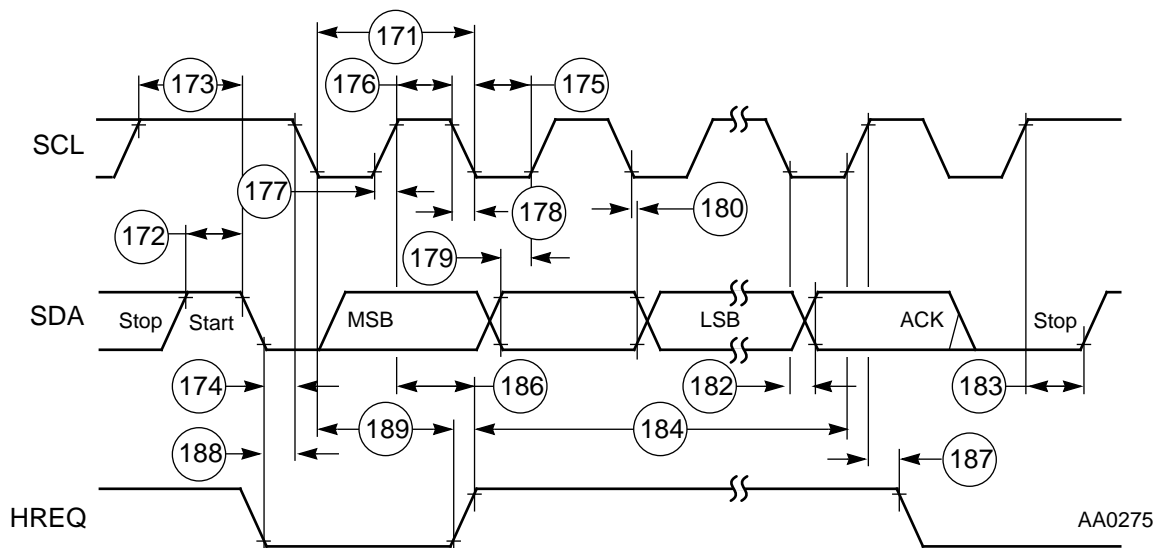


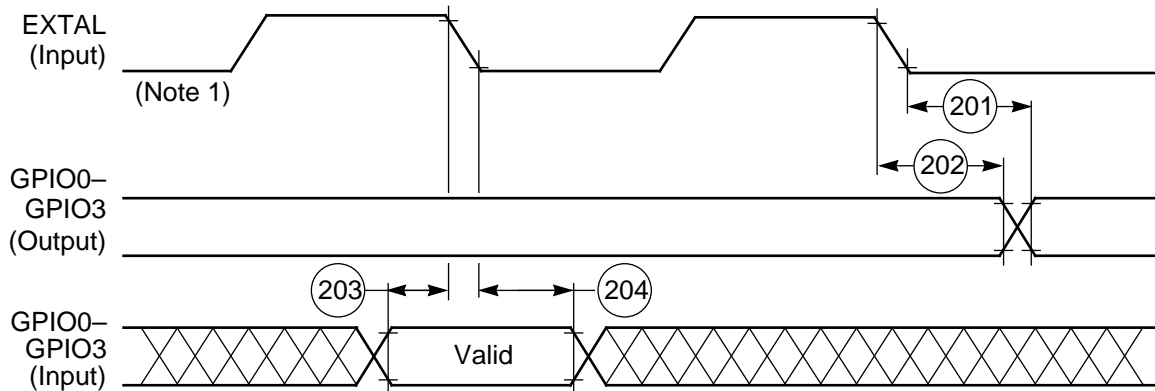
Figure 2-21 I<sup>2</sup>C Timing

**GENERAL PURPOSE I/O (GPIO) TIMING**

( $C_L = 50 \text{ pF} + 2 \text{ TTL Loads}$ )

**Table 2-16** GPIO Timing

No.	Characteristics	Expression	All frequencies		Unit
			Min	Max	
201	EXTAL Edge to GPIO Out Valid (GPIO Out Delay Time)	26	—	26	ns
202	EXTAL Edge to GPIO Out Not Valid (GPIO Out Hold Time)	2	2	—	ns
203	GPIO In Valid to EXTAL Edge (GPIO In Set-up Time)	10	10	—	ns
204	EXTAL Edge to GPIO In Not Valid (GPIO In Hold Time)	6	6	—	ns



Note: 1. Valid when the ratio between EXTAL frequency and internal clock frequency equals 1

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**Figure 2-22** GPIO Timing

## ON-CHIP EMULATION (OnCE™) TIMING

(C<sub>L</sub> = 50 pF + 2 TTL Loads)

Table 2-17 OnCE Timing

No.	Characteristics	All frequencies		Unit
		Min	Max	
230	DSCK Low	40	—	ns
231	DSCK High	40	—	ns
232	DSCK Cycle Time	200	—	ns
233	$\overline{DR}$ Asserted to DSO $(\overline{ACK})$ Asserted	5 T <sub>C</sub>	—	ns
234	DSCK High to DSO Valid	—	42	ns
235	DSCK High to DSO Invalid	3	—	ns
236	DSI Valid to DSCK Low (Set-up)	15	—	ns
237	DSCK Low to DSI Invalid (Hold)	3	—	ns
238	Last DSCK Low to OS0–OS1, $\overline{ACK}$ Active	3 T <sub>C</sub> + T <sub>L</sub>	—	ns
239	DSO $(\overline{ACK})$ Asserted to First DSCK High	2 T <sub>C</sub>	—	ns
240	DSO $(\overline{ACK})$ Assertion Width	4 T <sub>C</sub> + T <sub>H</sub> - 3	5 T <sub>C</sub> + 7	ns
241	DSO $(\overline{ACK})$ Asserted to OS0–OS1 High Impedance <sup>1</sup>	—	0	ns
242	OS0–OS1 Valid to EXTAL Transition #2	T <sub>C</sub> - 21	—	ns
243	EXTAL Transition #2 to OS0–OS1 Invalid	0	—	ns
244	Last DSCK Low of Read Register to First DSCK High of Next Command	7 T <sub>C</sub> + 10	—	ns
245	Last DSCK Low to DSO Invalid (Hold)	3	—	ns
246	$\overline{DR}$ Assertion to EXTAL Transition #2 for Wake Up from Wait State	10	T <sub>C</sub> - 10	ns
247	EXTAL Transition #2 to DSO After Wake Up from Wait State	17 T <sub>C</sub>	—	ns

Table 2-17 OnCE Timing (Continued)

No.	Characteristics	All frequencies		Unit
		Min	Max	
248	$\overline{DR}$ Assertion Width <ul style="list-style-type: none"> <li>to recover from WAIT</li> <li>to recover from WAIT and enter Debug mode</li> </ul>	15 13 $T_C + 15$	12 $T_C - 15$ —	ns ns
249	$\overline{DR}$ Assertion to DSO ( $\overline{ACK}$ ) Valid (Enter Debug mode) After Asynchronous Recovery from Wait State	17 $T_C$	—	ns
250A	$\overline{DR}$ Assertion Width to Recover from STOP <sup>2</sup> <ul style="list-style-type: none"> <li>Stable External Clock, OMR Bit 6 = 0</li> <li>Stable External Clock, OMR Bit 6 = 1</li> <li>Stable External Clock, PCTL Bit 17 = 1</li> </ul>	15 15 15	65548 $T_C + T_L$ 20 $T_C + T_L$ 13 $T_C + T_L$	ns ns ns
250B	$\overline{DR}$ Assertion Width to Recover from STOP and enter Debug mode <sup>2</sup> <ul style="list-style-type: none"> <li>Stable External Clock, OMR Bit 6 = 0</li> <li>Stable External Clock, OMR Bit 6 = 1</li> <li>Stable External Clock, PCTL Bit 17 = 1</li> </ul>	65549 $T_C + T_L$ 21 $T_C + T_L$ 14 $T_C + T_L$	— — —	ns ns ns
251	$\overline{DR}$ Assertion to DSO ( $\overline{ACK}$ ) Valid (Enter Debug mode) After Recovery from Stop State <sup>2</sup> <ul style="list-style-type: none"> <li>Stable External Clock, OMR Bit 6 = 0</li> <li>Stable External Clock, OMR Bit 6 = 1</li> <li>Stable External Clock, PCTL Bit 17 = 1</li> </ul>	65553 $T_C + T_L$ 25 $T_C + T_L$ 18 $T_C + T_L$	— — —	ns ns ns
Note: 1. Maximum $T_L$ 2. Periodically sampled, not 100% tested				

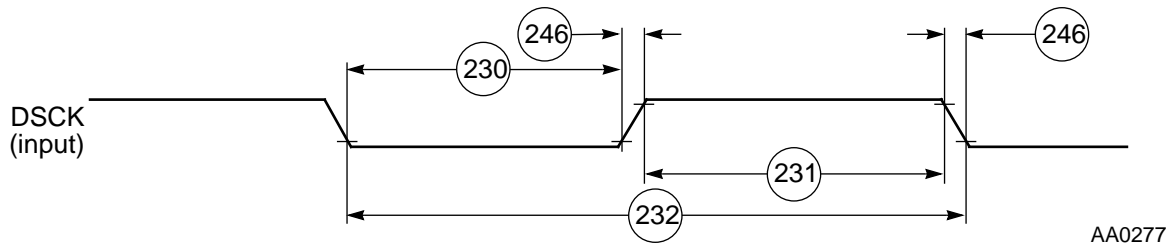


Figure 2-23 DSP56004 OnCE Serial Clock Timing

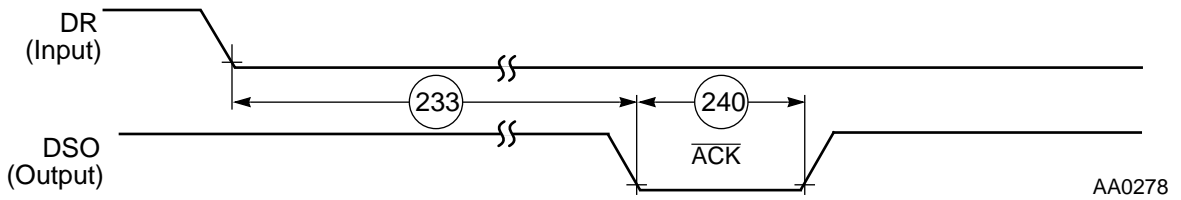


Figure 2-24 DSP56004 OnCE Acknowledge Timing

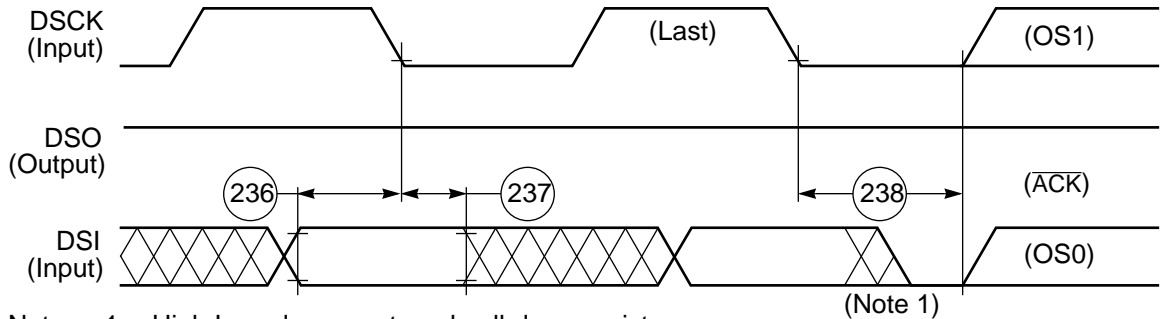


Figure 2-25 DSP56004 OnCE Data I/O to Status Timing

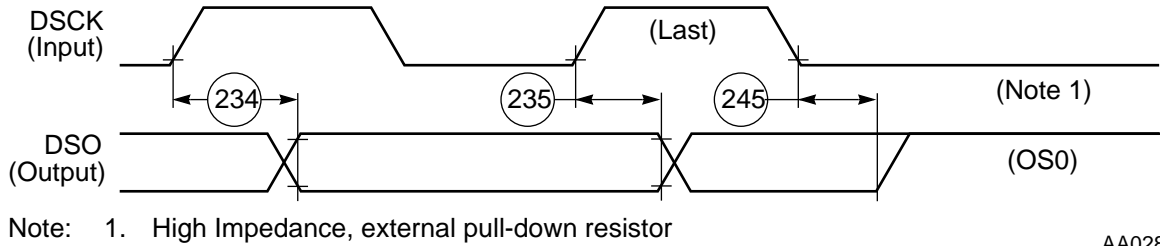


Figure 2-26 DSP56004 OnCE Read Timing

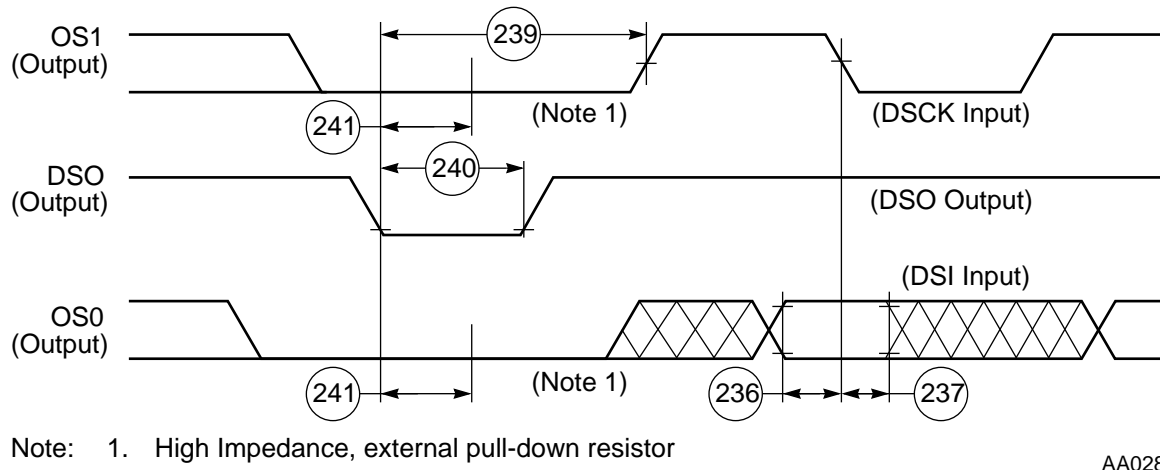
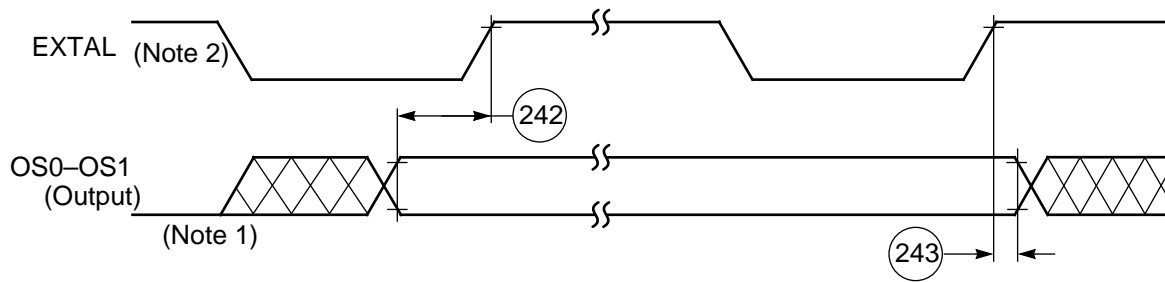


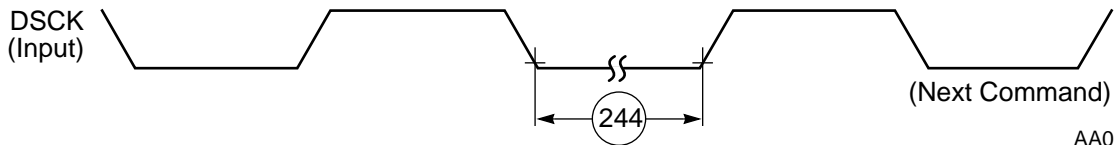
Figure 2-27 DSP56004 OnCE Data I/O Status Timing



- Note: 1. High Impedance, external pull-down resistor  
 2. Valid when the ratio between EXTAL frequency and clock frequency equals 1

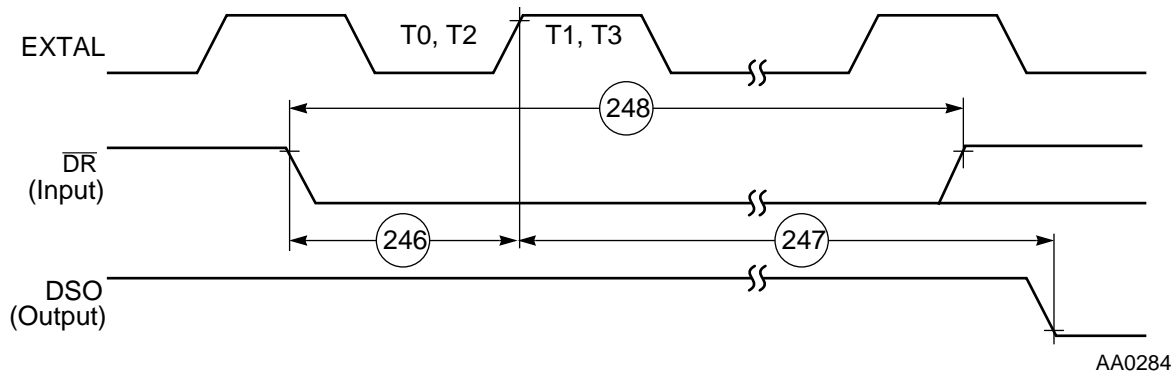
AA0282

**Figure 2-28** DSP56004 OnCE EXTAL to Status Timing



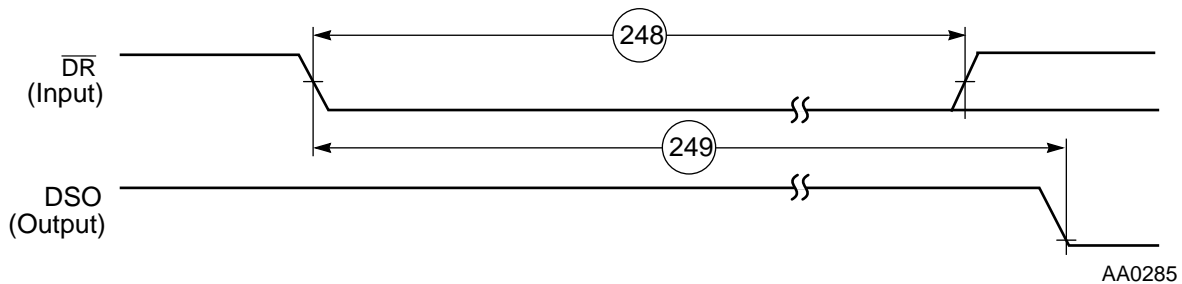
AA0283

**Figure 2-29** DSP56004 OnCE DSCK Next Command After Read Register Timing



AA0284

**Figure 2-30** Synchronous Recovery from Wait State



AA0285

**Figure 2-31** Asynchronous Recovery from Wait State



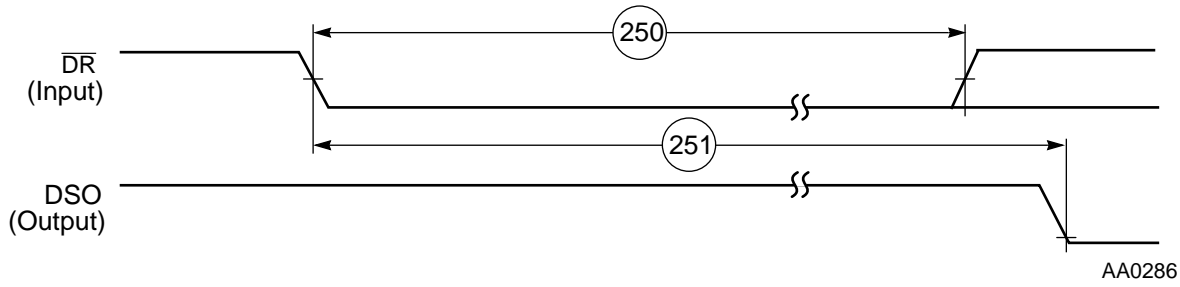


Figure 2-32 Asynchronous Recovery from Stop State



# SECTION 3

## PACKAGING

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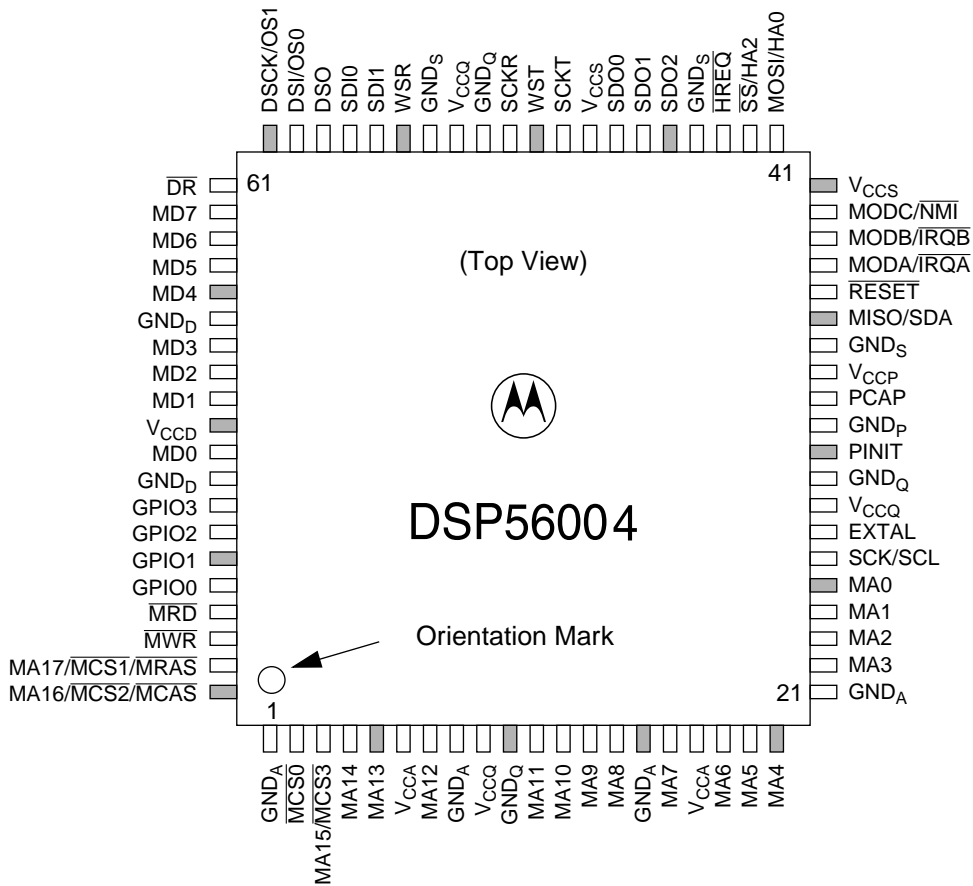
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### PIN-OUT AND PACKAGE INFORMATION

This section provides information about the available packages for this product, including diagrams of the package pinouts and tables describing how the signals described in **Section 1** are allocated. The DSP56004 is available in an 80-pin Plastic Quad Flat Pack (PQFP) package.

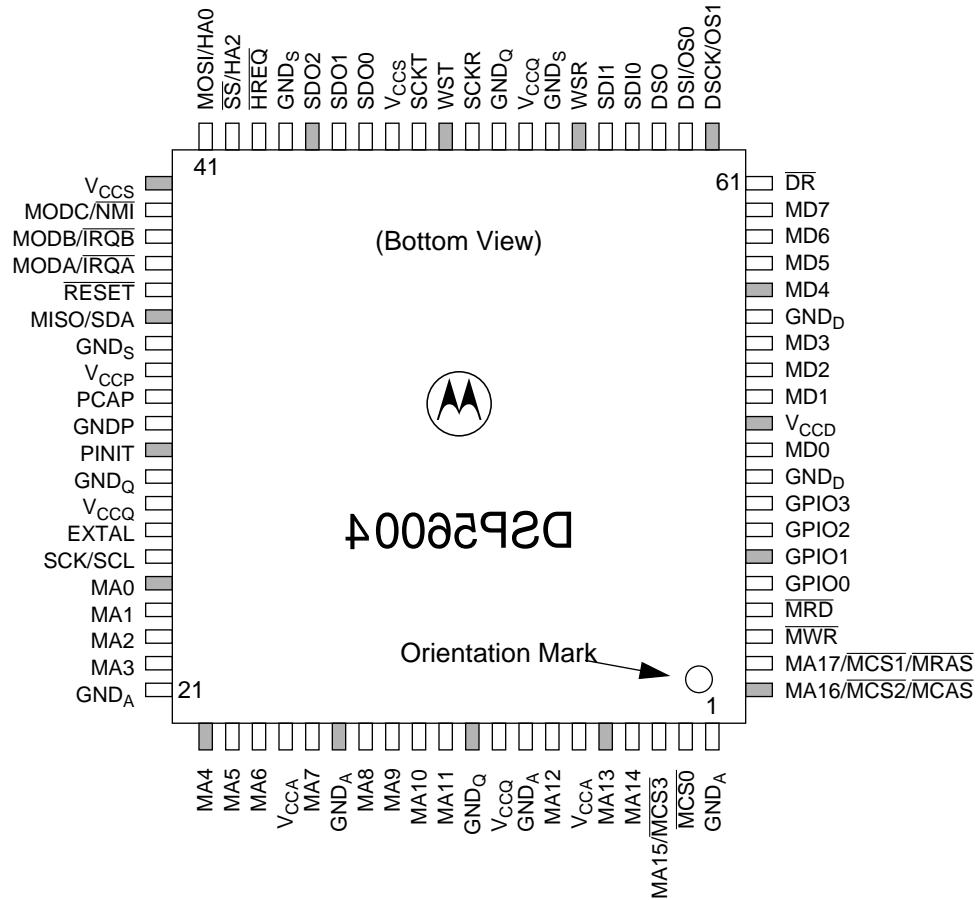
**PQFP Package Description**

Top and bottom views of the PQFP package are shown in **Figure 3-1** and **Figure 3-2** with their pin-outs.



**Note:** An OVERBAR indicates the signal is asserted when the voltage = ground (active low). To simplify locating the pins, each fifth pin is shaded in the illustration.

**Figure 3-1** Top View



**Note:** An OVERBAR indicates the signal is asserted when the voltage = ground (active low). To simplify locating the pins, each fifth pin is shaded in the illustration.

**Figure 3-2** Bottom View

**Table 3-1 DSP56004 Pin Identification by Pin Number**

Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
1	GND <sub>A</sub>	28	V <sub>CCQ</sub>	55	WSR
2	$\overline{\text{MCS0}}$	29	GND <sub>Q</sub>	56	SDI1
3	MA15/ $\overline{\text{MCS3}}$	30	PINIT	57	SDI0
4	MA14	31	GND <sub>P</sub>	58	DSO
5	MA13	32	PCAP	59	DSI/OS0
6	V <sub>CCA</sub>	33	V <sub>CCP</sub>	60	DSCK/OS1
7	MA12	34	GND <sub>S</sub>	61	$\overline{\text{DR}}$
8	GND <sub>A</sub>	35	MISO/SDA	62	MD7
9	V <sub>CCQ</sub>	36	$\overline{\text{RESET}}$	63	MD6
10	GND <sub>Q</sub>	37	MODA/ $\overline{\text{IRQA}}$	64	MD5
11	MA11	38	MODB/ $\overline{\text{IRQB}}$	65	MD4
12	MA10	39	MODC/ $\overline{\text{NMI}}$	66	GND <sub>D</sub>
13	MA9	40	V <sub>CCS</sub>	67	MD3
14	MA8	41	MOSI/HA0	68	MD2
15	GND <sub>A</sub>	42	$\overline{\text{SS}}/\text{HA2}$	69	MD1
16	MA7	43	$\overline{\text{HREQ}}$	70	V <sub>CCD</sub>
17	V <sub>CCA</sub>	44	GND <sub>S</sub>	71	MD0
18	MA6	45	SDO2	72	GND <sub>D</sub>
19	MA5	46	SDO1	73	GPIO3
20	MA4	47	SDO0	74	GPIO2
21	GND <sub>A</sub>	48	V <sub>CCS</sub>	75	GPIO1
22	MA3	49	SCKT	76	GPIO0
23	MA2	50	WST	77	$\overline{\text{MRD}}$
24	MA1	51	SCKR	78	$\overline{\text{MWR}}$
25	MA0	52	GND <sub>Q</sub>	79	MA17/ $\overline{\text{MCS1}}$ / MRAS
26	SCK/SCL	53	V <sub>CCQ</sub>	80	MA16/ $\overline{\text{MCS2}}$ / MCAS
27	EXTAL	54	GND <sub>S</sub>		

Table 3-2 DSP56004 Pin Identification by Signal Name

Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #
DR	61	MA5	19	MRD	77
DSCK	60	MA6	18	MWR	78
DSI	59	MA7	16	NMI	39
DSO	58	MA8	14	OS0	59
EXTAL	27	MA9	13	OS1	60
GND <sub>A</sub>	1	MA10	12	PCAP	32
GND <sub>A</sub>	8	MA11	11	PINIT	30
GND <sub>A</sub>	15	MA12	7	RESET	36
GND <sub>A</sub>	21	MA13	5	SCK	26
GND <sub>D</sub>	66	MA14	4	SCKR	51
GND <sub>D</sub>	72	MA15	3	SCKT	49
GND <sub>P</sub>	31	MA16	80	SCL	26
GND <sub>Q</sub>	10	MA17	79	SDA	35
GND <sub>Q</sub>	29	MCAS	80	SDI0	57
GND <sub>Q</sub>	52	MCS0	2	SDI1	56
GND <sub>S</sub>	34	MCS1	79	SDO0	47
GND <sub>S</sub>	44	MCS2	80	SDO1	46
GND <sub>S</sub>	54	MCS3	3	SDO2	45
GPIO0	76	MD0	71	SS	42
GPIO1	75	MD1	69	V <sub>CCA</sub>	6
GPIO2	74	MD2	68	V <sub>CCA</sub>	17
GPIO3	73	MD3	67	V <sub>CCD</sub>	70
HA0	41	MD4	65	V <sub>CCP</sub>	33
HA2	42	MD5	64	V <sub>CCQ</sub>	9
HREQ	43	MD6	63	V <sub>CCQ</sub>	28
IRQA	37	MD7	62	V <sub>CCQ</sub>	53
IRQB	38	MISO	35	V <sub>CCS</sub>	40
MA0	25	MODA	37	V <sub>CCS</sub>	48
MA1	24	MODB	38	WSR	55
MA2	23	MODC	39	WST	50
MA3	22	MOSI	41		
MA4	20	MRAS	79		

**Table 3-3** DSP56004 Power Supply Pins

Pin #	Signal Name	Circuit Supplied
6	$V_{CCA}$	Address Bus Buffers
17		
1	$GND_A$	
8		
15		
21		
70	$V_{CCD}$	Data Bus Buffers
66	$GND_D$	
72		
9	$V_{CCQ}$	Internal Logic
28		
53		
10	$GND_Q$	
29		
52		
33	$V_{CCP}$	PLL
31	$GND_P$	
40	$V_{CCS}$	Serial Ports
48		
34	$GND_S$	
44		
54		



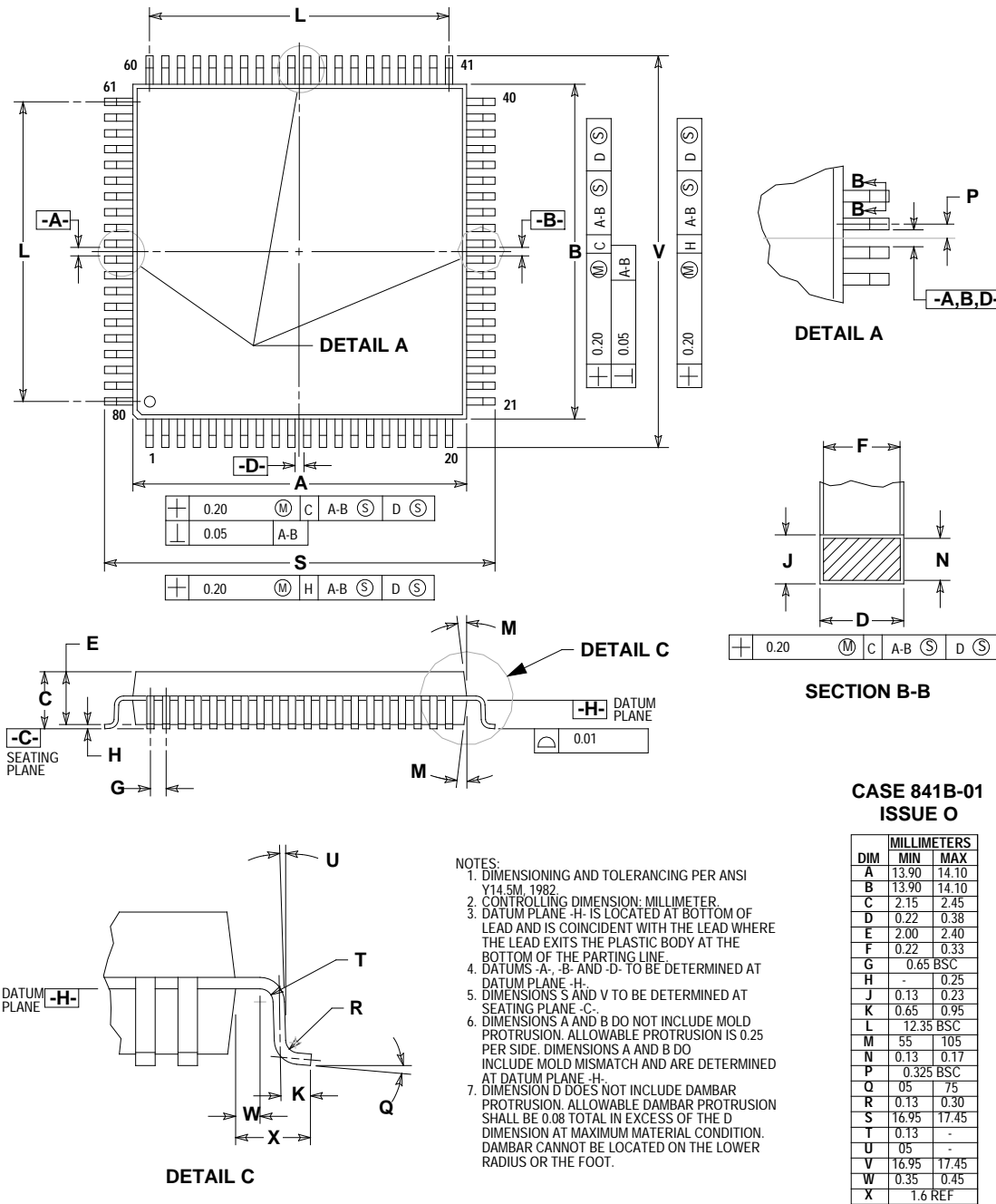


Figure 3-3 80-pin Plastic Quad Flat Pack (PQFP) Mechanical Information

## ORDERING DRAWINGS

Complete mechanical information regarding DSP56004 packaging is available by facsimile through Motorola's Mfax™ system. Call the following number to obtain information by facsimile:

(602) 244-6591

The Mfax automated system requests the following information:

- The receiving facsimile telephone number including area code or country code
- The caller's Personal Identification Number (PIN)

**Note:** For first time callers, the system provides instructions for setting up a PIN, which requires entry of a name and telephone number.

- The type of information requested:
  - Instructions for using the system
  - A literature order form
  - Specific part technical information or data sheets
  - Other information described by the system messages

A total of three documents may be ordered per call.

The DSP56004 80-pin PQFP package mechanical drawing is referenced as 841B-01.



# SECTION 4

## DESIGN CONSIDERATIONS

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### THERMAL DESIGN CONSIDERATIONS

An estimation of the chip junction temperature,  $T_J$ , in °C can be obtained from the equation:

**Equation 1:**  $T_J = T_A + (P_D \times R_{\theta JA})$

Where:

$T_A$  = ambient temperature °C

$R_{\theta JA}$  = package junction-to-ambient thermal resistance °C/W

$P_D$  = power dissipation in package

Historically, thermal resistance has been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

**Equation 2:**  $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

Where:

$R_{\theta JA}$  = package junction-to-ambient thermal resistance °C/W

$R_{\theta JC}$  = package junction-to-case thermal resistance °C/W

$R_{\theta CA}$  = package case-to-ambient thermal resistance °C/W

$R_{\theta JC}$  is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance,  $R_{\theta CA}$ . For example, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the Printed Circuit Board, or otherwise change the thermal dissipation capability of the area surrounding the device on a Printed Circuit Board. This model is most useful for ceramic packages with heat sinks; some 90% of the heat flow is dissipated through the case to the heat sink and out to the ambient environment. For ceramic packages, in situations where the heat flow is split between a path to the case and an alternate path through the Printed Circuit Board, analysis of the device thermal performance may need the additional modeling capability of a system level thermal simulation tool.

The thermal performance of plastic packages is more dependent on the temperature of the Printed Circuit Board to which the package is mounted. Again, if the estimations obtained from  $R_{\theta JA}$  do not satisfactorily answer whether the thermal performance is adequate, a system level model may be appropriate.

A complicating factor is the existence of three common ways for determining the junction-to-case thermal resistance in plastic packages:

- To minimize temperature variation across the surface, the thermal resistance is measured from the junction to the outside surface of the package (case) closest to the chip mounting area when that surface has a proper heat sink.
- To define a value approximately equal to a junction-to-board thermal resistance, the thermal resistance is measured from the junction to where the leads are attached to the case.
- If the temperature of the package case ( $T_T$ ) is determined by a thermocouple, the thermal resistance is computed using the value obtained by the equation  $(T_J - T_T)/P_D$ .

As noted above, the junction-to-case thermal resistances quoted in this data sheet are determined using the first definition. From a practical standpoint, that value is also suitable for determining the junction temperature from a case thermocouple reading in forced convection environments. In natural convection, using the junction-to-case thermal resistance to estimate junction temperature from a thermocouple reading on the case of the package will estimate a junction temperature slightly hotter than actual temperature. Hence, the new thermal metric, Thermal Characterization Parameter or  $\Psi_{JT}$ , has been defined to be  $(T_J - T_T)/P_D$ . This value gives a better estimate of the junction temperature in natural convection when using the surface temperature of the package. Remember that surface temperature readings of packages are subject to significant errors caused by inadequate attachment of the sensor to the surface and to errors caused by heat loss to the sensor. The recommended technique is to attach a 40-gauge thermocouple wire and bead to the top center of the package with thermally conductive epoxy.

## ELECTRICAL DESIGN CONSIDERATIONS

### CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ).

Use the following list of recommendations to assure correct DSP operation:

- Provide a low-impedance path from the board power supply to each  $V_{CC}$  pin on the DSP, and from the board ground to each GND pin.
- Use at least four 0.01–0.1  $\mu\text{F}$  bypass capacitors positioned as close as possible to the four sides of the package to connect the  $V_{CC}$  power source to GND.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip  $V_{CC}$  and GND pins are less than 0.5 in per capacitor lead.
- Use at least a four-layer Printed Circuit Board (PCB) with two inner layers for  $V_{CC}$  and GND.
- Because the DSP output signals have fast rise and fall times, PCB trace lengths should be minimal. This recommendation particularly applies to the address and data buses as well as the  $\overline{\text{IRQA}}$ ,  $\overline{\text{IRQB}}$ , and  $\overline{\text{NMI}}$  pins. Maximum Printed Circuit Board (PCB) trace lengths on the order of 6 inches are recommended.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the  $V_{CC}$  and GND circuits.
- All inputs must be terminated (i.e., not allowed to float) using CMOS levels, except as noted in **Section 1**.
- Take special care to minimize noise levels on the  $V_{CCP}$  and  $\text{GND}_P$  pins.
- If multiple DSP56004 devices are on the same board, check for cross-talk or excessive spikes on the supplies due to synchronous operation of the devices.

## POWER CONSUMPTION CONSIDERATIONS

Power dissipation is a key issue in portable DSP applications. Some of the factors which affect current consumption are described in this section. Most of the current consumed by CMOS devices is Alternating Current (AC), which is charging and discharging the capacitances of the pins and internal nodes.

Current consumption is described by the formula:

**Equation 3:**  $I = C \times V \times f$

where:  $C$  = node/pin capacitance  
 $V$  = voltage swing  
 $f$  = frequency of node/pin toggle

### Example 4-1 Current Consumption

---

For an I/O pin loaded with 50 pF capacitance, operating at 5.5 V, and with a 81 MHz clock, toggling at its maximum possible rate (20 MHz), the current consumption is:

**Equation 4:**  $I = 50 \times 10^{-12} \times 5.5 \times 20 \times 10^6 = 5.5\text{mA}$

---

The Maximum Internal Current ( $I_{CCI\text{max}}$ ) value reflects the typical possible switching of the internal buses on best-case operation conditions, which is not necessarily a real application case. The Typical Internal Current ( $I_{CCI\text{typ}}$ ) value reflects the average switching of the internal buses on typical operating conditions.

For applications that require very low current consumption:

- Minimize the number of pins that are switching.
- Minimize the capacitive load on the pins.
- Connect the unused inputs to pull-up or pull-down resistors.
- Disable unused peripherals.
- Disable unused pin activity.

Current consumption test code:

```

org      p:RESET
        jmp      MAIN
        org      p:MAIN
        movep    #$180000,x:$FFFD
        move     #0,r0
        move     #0,r4
        move     #$00FF,m0
        move     #$00FF,m4
        nop
        rep      #256
        move     r0,x:(r0)+
        rep      #256
        mov      r4,y:(r4)+
        clr      a
        move     l:(r0)+,a
        rep      #30
        mac      x0,y0,a      x:(r0)+,x0      y:(r4)+,y0
        move     a,p:(r5)
        jmp      TP1
TP1     nop
        jmp      MAIN

```

## POWER-UP CONSIDERATIONS

To power-up the device properly, ensure that the following conditions are met:

- Stable power is applied to the device according to the specifications in **Table 2-3** (DC Electrical Characteristics).
- The external clock oscillator is active and stable.
- $\overline{\text{RESET}}$  is asserted according to the specifications in **Table 2-7** (Reset, Stop, Mode Select, and Interrupt Timing).
- The following input pins are driven to valid voltage levels:  $\overline{\text{DR}}$ , PINIT, MODA, MODB, and MODC.

Care should be taken to ensure that the maximum ratings for all input voltages obey the restrictions on **Table 2-1** (Maximum Ratings), at all phases of the power-up procedure. This may be achieved by powering the external clock, hardware reset, and mode selection circuits from the same power supply that is connected to the power supply pins of the chip.

At the beginning of the hardware reset procedure, the device might consume significantly more current than the specified typical supply current. This is because of contentions among the internal nodes being affected by the hardware reset signal until they reach their final hardware reset state.





## SECTION 5

# ORDERING INFORMATION

Consult a Motorola Semiconductor sales office or authorized distributor to determine product availability and to place an order.

Table 5-1 Ordering Information

Part	Supply Voltage	Package Type	Pin Count	Frequency (MHz)	Order Number
DSP56004	5 V	Quad Flat Pack (QFP)	80	50	DSP56004FJ50
				66	DSP56004FJ66
				81	DSP56004FJ81
DSP56004ROM <sup>1</sup>	5 V	Quad Flat Pack (QFP)	80	50	Customer Specific
				66	Customer Specific
				81	Customer Specific
Note: 1. For additional information on future part development, or to request specific ROM-based support, call your local Motorola Semiconductor sales office or authorized distributor.					




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