

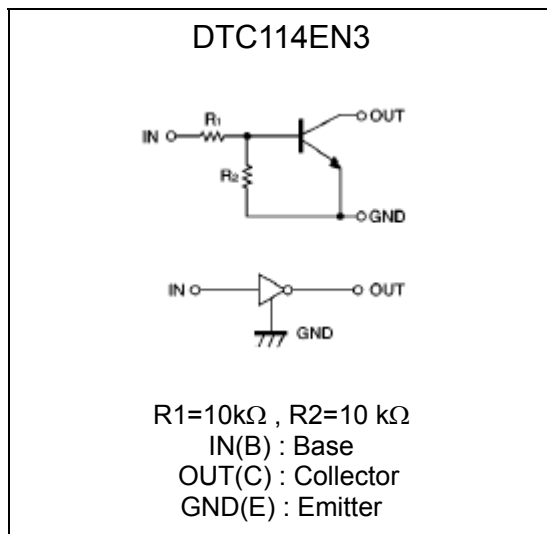
NPN Digital Transistors (Built-in Resistors)

DTC114EN3

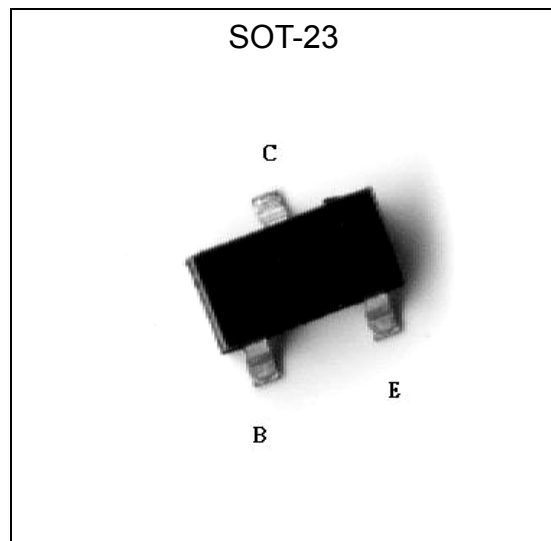
Features

- Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors (see equivalent circuit).
- The bias resistors consist of thin-film resistors with complete isolation to allow negative biasing of the input. They also have the advantage of almost completely eliminating parasitic effects.
- Only the on/off conditions need to be set for operation, making device design easy.
- Complements the DTA114EN3.
- Pb-free lead plating and halogen-free package

Equivalent Circuit

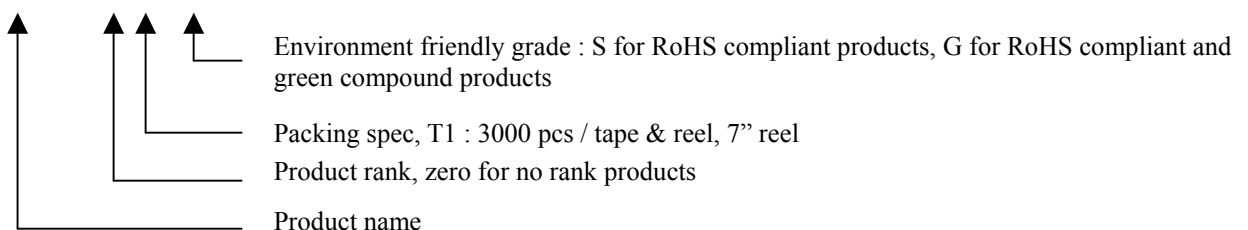


Outline



Ordering Information

Device	Package	Shipping
DTC114EN3-0-T1-G	SOT-23 (Pb-free lead plating and halogen-free package)	3000 pcs / Tape & Reel



**Absolute Maximum Ratings** (Ta=25°C)

Parameter	Symbol	Limits	Unit
Supply Voltage	V _{CC}	50	V
Input Voltage	V _{IN}	-10~+40	V
Output Current	I _o	50	mA
	I _{O(max.)}	100	mA
Power Dissipation	P _d	200	mW
Operating Junction Temperature Range	T _j	-55~+150	°C
Storage Temperature Range	T _{stg}	-55~+150	°C

Characteristics (Ta=25°C)

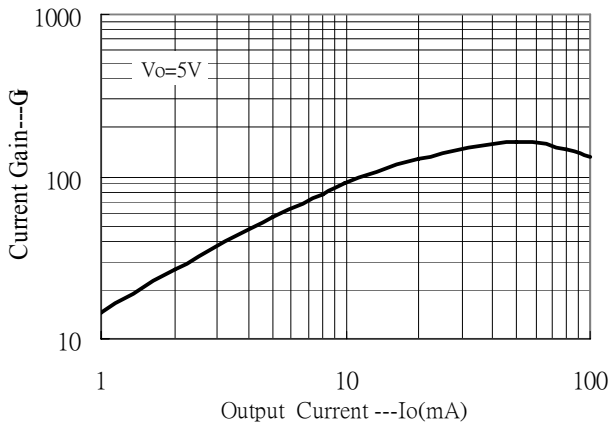
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input Voltage	V _{I(off)}	-	-	0.5	V	V _{CC} =5V, I _o =100μA
	V _{I(on)}	3	-	-	V	V _o =0.3V, I _o =10mA
Output Voltage	V _{O(on)}	-	0.1	0.3	V	I _o /I _i =10mA/0.5mA
Input Current	I _i	-	-	0.88	mA	V _I =5V
Output Current	I _{O(off)}	-	-	0.5	μA	V _{CC} =50V, V _I =0V
DC Current Gain	G _i	30	-	-	-	V _o =5V, I _o =5mA
Input Resistance	R ₁	7	10	13	kΩ	-
Resistance Ratio	R ₂ /R ₁	0.8	1	1.2	-	-
Transition Frequency	f _T	-	250	-	MHz	V _{CE} =10V, I _C =5mA, f=100MHz*

* Transition frequency of the device

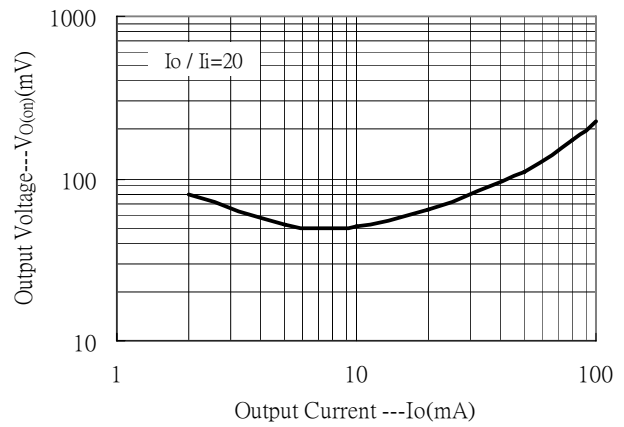


Typical Characteristics

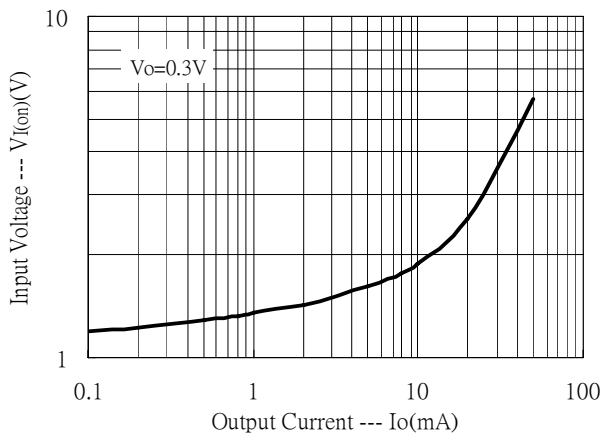
Current Gain vs Output Current



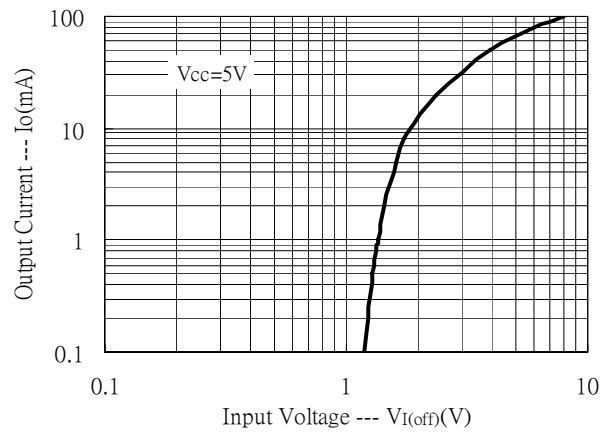
Output Voltage vs Output Current



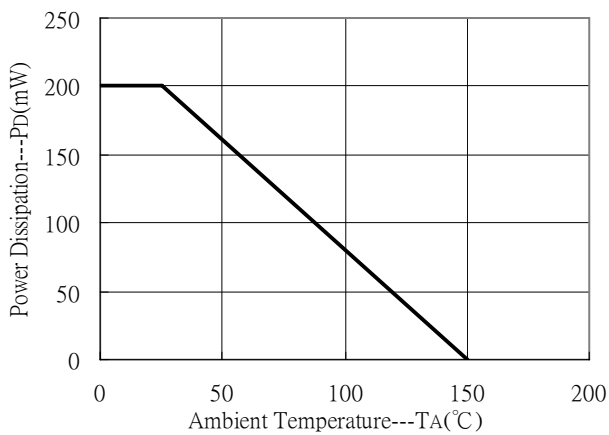
Input Voltage vs Output Current (ON characteristics)



Output Current vs Input Voltage (OFF characteristics)



Power Derating Curve





Product Designation

DT X X X X X XX
(1) (2) (3) (4) (5) (6) (7)

(1) Indicates that transistor is digital

(2) Indicates polarity
A, B PNP
C, D NPN

(3) Indicates device specification

(4) Indicates the basis of the R1 resistance value
1 1.0
2 2.2
3 3.3
4 4.7
6 6.8

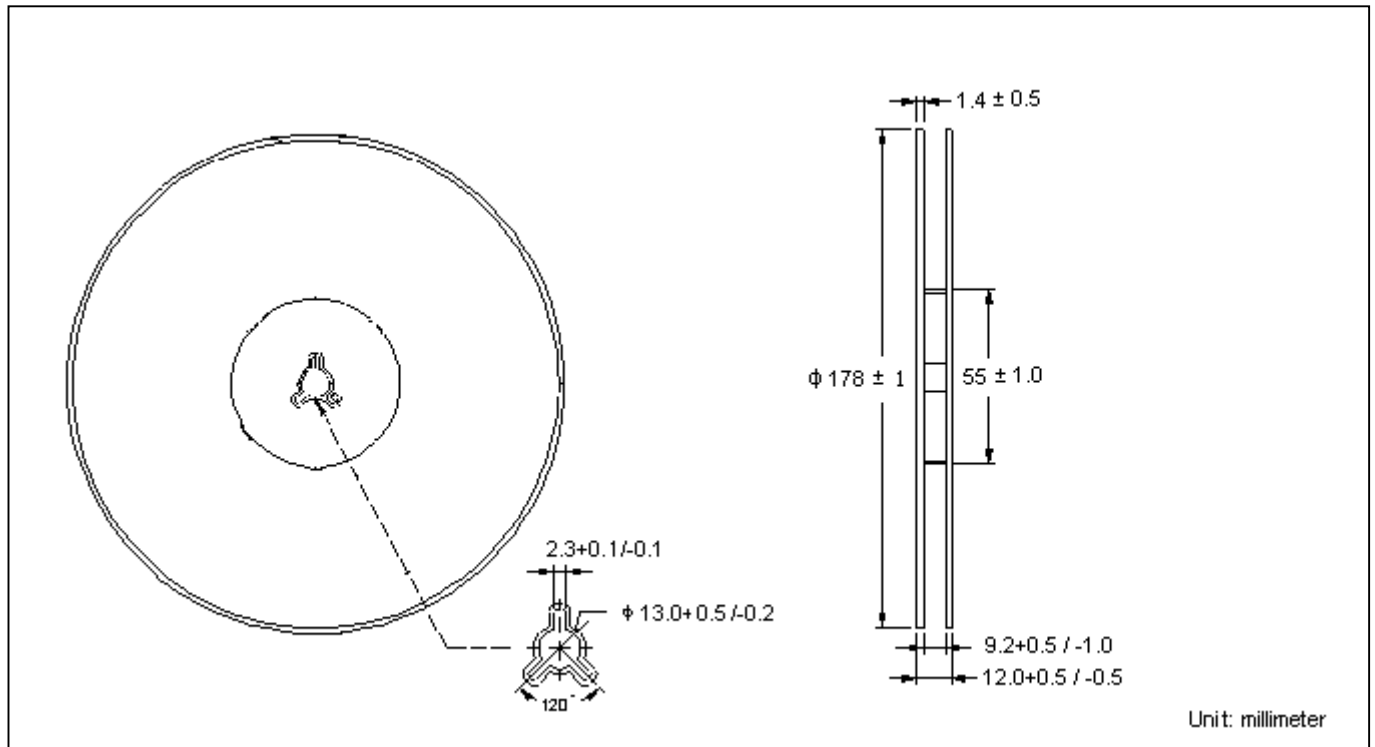
(5) Indicates power-of-ten of R1 value
3 10³
4 10⁴

The value of R1 is indicated by combining (4) and (5)
24 2.2×10⁴ =22kΩ
43 4.3×10³ =4.7kΩ

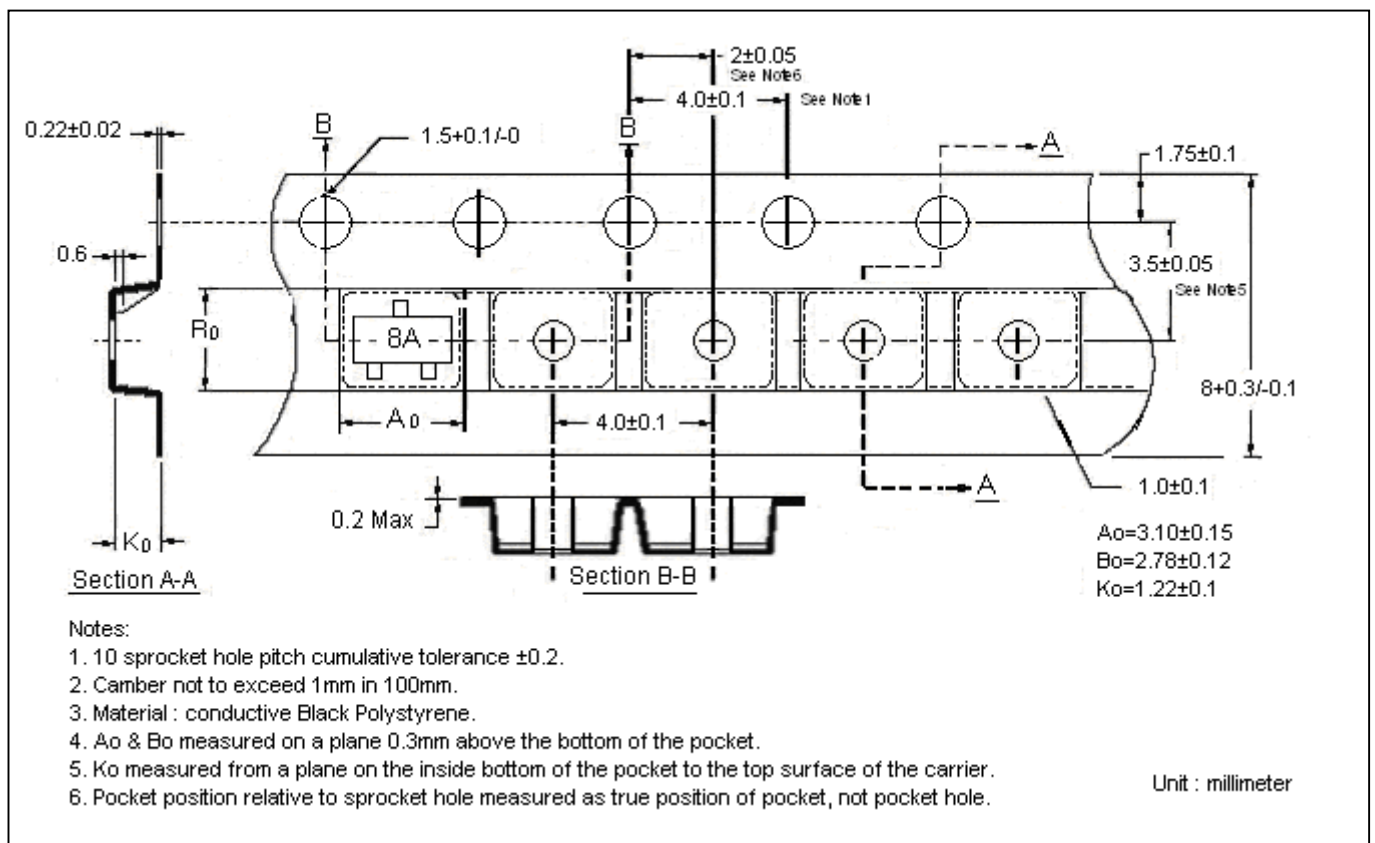
(6) Indicates resistance ratio R1 / R2
E R1/R2 = 1/1
X R1/R2 = 1/2
Y R1/R2 = 1/5
Z R1/R2 = 1/10
J R1/R2 = 1/20
W R1/R2 = 2/1
U R1/R2 = 10/1
V R1/R2 = 5/1
T R1 only
G R2 only

(7) Indicates package shape
N3 SOT-23
A3 TO-92

Reel Dimension



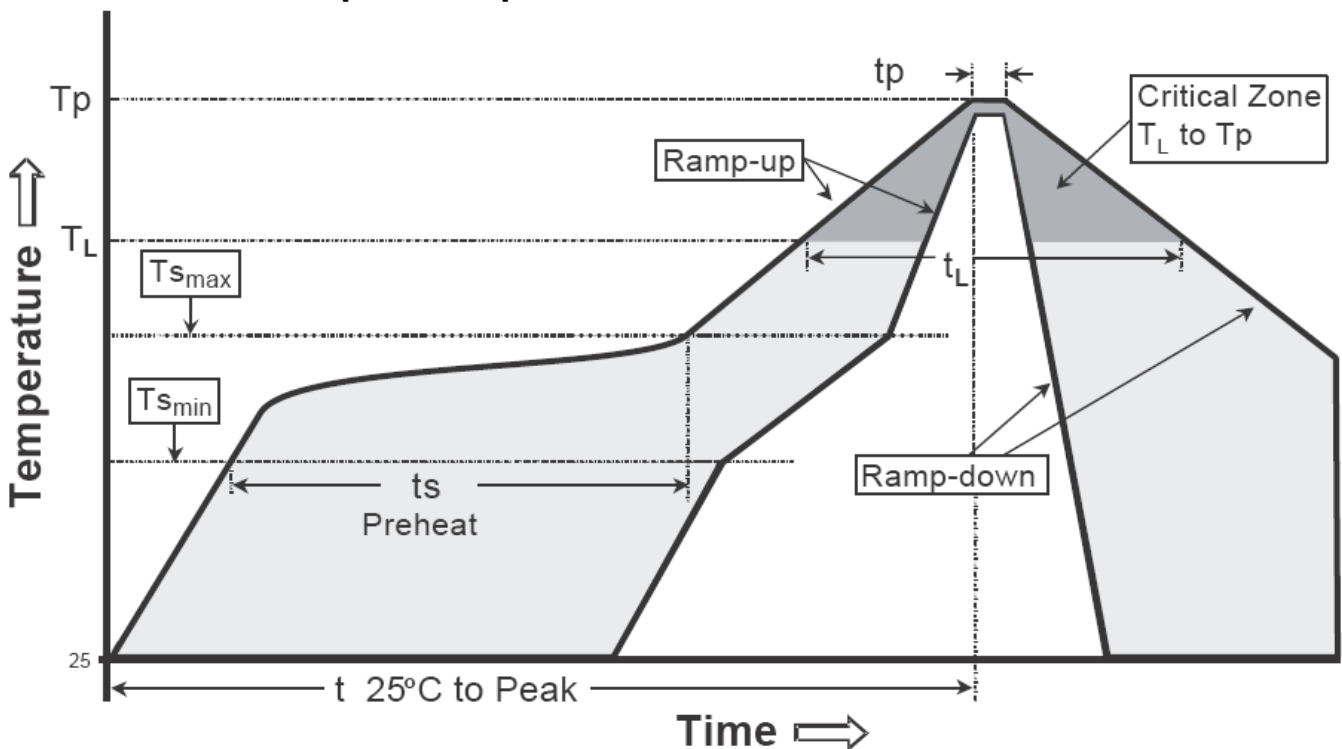
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

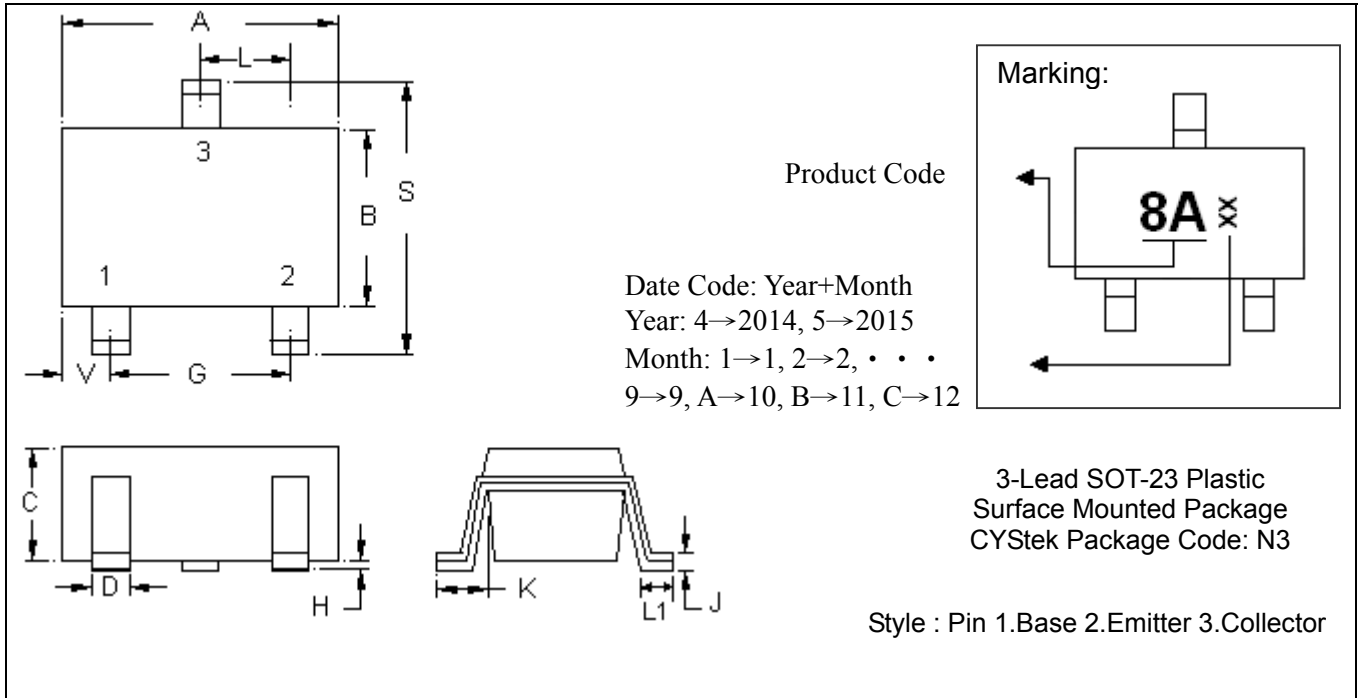
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (Tl)	183°C	217°C
- Time (tL)	60-150 seconds	60-150 seconds
Peak Temperature(Tp)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

SOT-23 Dimension



*:Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1102	0.1204	2.80	3.04	J	0.0032	0.0079	0.08	0.20
B	0.0472	0.0669	1.20	1.70	K	0.0118	0.0266	0.30	0.67
C	0.0335	0.0512	0.89	1.30	L	0.0335	0.0453	0.85	1.15
D	0.0118	0.0197	0.30	0.50	S	0.0830	0.1161	2.10	2.95
G	0.0669	0.0910	1.70	2.30	V	0.0098	0.0256	0.25	0.65
H	0.0000	0.0040	0.00	0.10	L1	0.0118	0.0197	0.30	0.50

Notes : 1.Controlling dimension : millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material :

- Lead : Pure tin plated.
- Mold Compound : Epoxy resin family, flammability solid burning class:UL94V-0.

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.