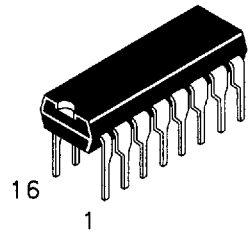
Dual JK Negative Edge-Triggered Flip-Flop

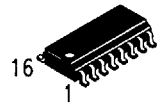
DV74AC112

This device consists of two high-speed completely independent transition clocked JK flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The JK design allows operation as a D flip-flop by connecting the J and K inputs together.

- **Advanced very high speed CMOS**
- **Outputs source/sink 24 mA**
- **Transmission line driving 50 ohms**
- **ACT has TTL compatible inputs**
- **Operation from 2 to 6 volts guaranteed**
- **DC & AC Parameters guaranteed over –40 to +85°C**

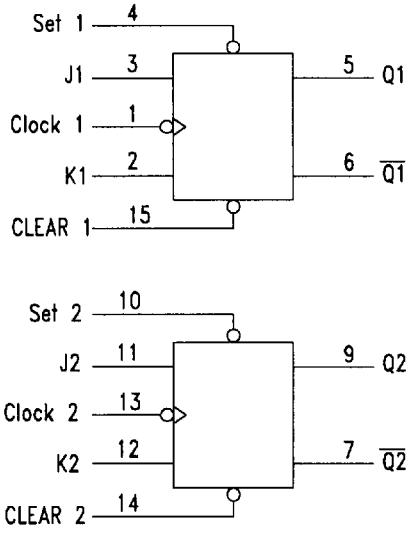


N Suffix
Plastic DIP
AVG-003 Case



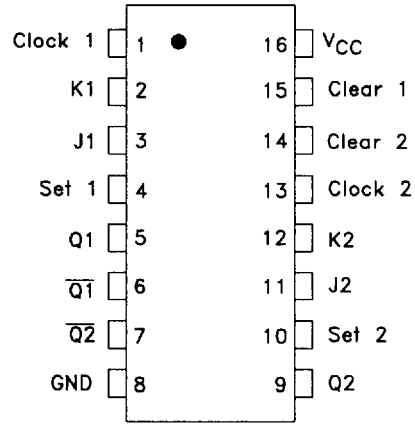
D Suffix
Plastic SOP
AVG-004 Case

LOGIC DIAGRAM



PIN 16 = V_{CC}
PIN 8 = GND

PIN ASSIGNMENT



TRUTH TABLE

Mode	Inputs				Output	
	Set	Clear	J	K	Q	$\overline{Q}$
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
Undertermined *	L	L	X	X	H	H
Toggle	H	H	h	h	$\overline{q}$	q
Load "O" (Reset)	H	H	l	h	L	H
Load "1" (Set)	H	H	h	l	H	L
Hold	H	H	i	l	q	$\overline{q}$

H,h = High Level Logic
L,l = Low Level Logic
X = Don't Care
l,h,q = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.
* Both outputs will be HIGH while both Set and Clear are LOW , but the output states are unpredictable if Set and Clear go HIGH simultaneously.

ABSOLUTE MAXIMUM RATINGS

Maximum ratings are those values beyond which damage to the device may occur.

Symbol	Parameter	AC112	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	− 0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	− 0.5 to V_{CC} +0.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	− 0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	± 20	mA
I_{OUT}	DC Output Sink/Source Current, per Pin	± 50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	± 50	mA
T_{STG}	Storage Temperature	− 65 to +150	°C

GUARANTEED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	'AC	2.0	5.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage, (Ref. to GND)		0		V_{CC}	V
t_r, t_f	Input Rise and Fall Time (V_{IN} from 30% to 70% V_{CC})	V_{CC} @ 3.0 V			150	ns/V
		V_{CC} @ 4.5 V			40	ns/V
		V_{CC} @ 5.5 V			25	ns/V
T_A	Operating Ambient Temperature Range		−40		85	°C
C_{IN}	Input Capacitance			4.5		pF
C_{PD}	Power Dissipation Capacitance			35		pF

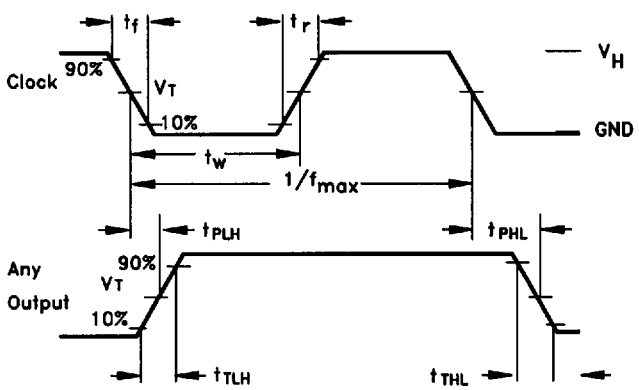
DC ELECTRICAL CHARACTERISTICS

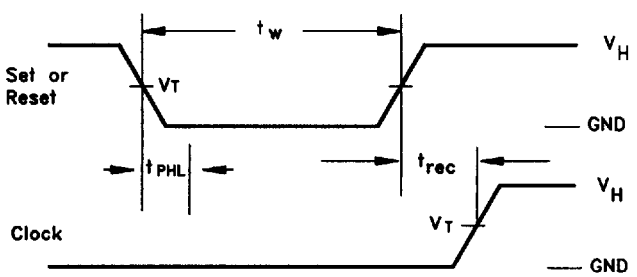
Symbol	Parameter	Conditions	V_{CC} (V)	AC112			Unit
				TA = +25°C		TA = −40 to +85°C	
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage	V_{OUT} = 0.1V or V_{CC} − 0.1 V	3.0 4.5 5.5	1.5 2.25 2.75	2.1 3.15 3.85	2.1 3.15 3.85	V
V_{IL}	Maximum Low Level Input Voltage	V_{OUT} = 0.1V or V_{CC} − 0.1 V	3.0 4.5 5.5	1.5 2.25 2.75	0.9 1.35 1.65	0.9 1.35 1.65	V
V_{OH}	Minimum High Level Output Voltage	IOUT = −50 µA	3.0 4.5 5.5	2.99 4.49 5.49	2.9 4.4 5.4	2.9 4.4 5.4	V
		V_{IN} = V_{IL} or V_{IH} −12mA I_{OH} −24mA −24 mA	3.0 4.5 5.5		2.56 3.86 4.86	2.46 3.76 4.76	V
V_{OL}	Maximum Low Level Output Voltage	IOUT = 50 µA	3.0 4.5 5.5	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{IN} = V_{IL} or V_{IH} 12mA I_{OL} 24mA 24 mA	3.0 4.5 5.5		0.36 0.36 0.36	0.44 0.44 0.44	V
I_{IN}	Maximum Input Leakage Current	VI=V_{CC}, GND	5.5		±0.1	±1.0	µA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND	5.5		4.0	40	µA

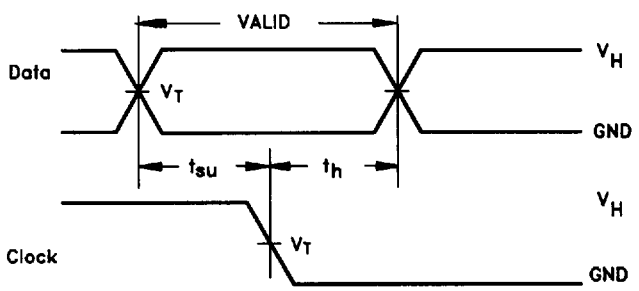
AC CHARACTERISTICS over full operating conditions

Symbol	Parameter	Vcc ±10% (V)	AC112				Unit
			T_A = +25°C, C_L = 50 pF		T_A = – 40°C to +85°C, C_L = 50 pF		
			Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	3.3 5.0	145 145		125 125		MHz
t_{PLH}	Propagation Delay C_{Pn} to Q_n or $\overline{Q}_n$	3.3 5.0	1.0 1.0	16.0 13.0	1.0 1.0	17.0 13.5	ns
t_{PHL}	Propagation Delay C_{Pn} to Q_n or $\overline{Q}_n$	3.3 5.0	1.0 1.0	16.0 13.0	1.0 1.0	16.5 13.5	ns
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.3 5.0	1.0 1.0	11.0 9.5	1.0 1.0	11.5 10.0	ns
t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.3 5.0	1.0 1.0	11.0 9.5	1.0 1.0	11.5 10.0	ns
t_s	Set-up Time, High or Low J_n or $\overline{K}_n$ to CP_n	3.3 5.0	6.5 4.5		7.5 5.0		ns
t_h	Hold Time, High or Low J_n or $\overline{K}_n$ to CP_n	3.3 5.0	0 0		0 0		ns
t_w	Pulse Width CP_n	3.3 5.0	6.0 5.0		6.5 5.5		ns
t_w	Pulse Width $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$	3.3 5.0	6.0 5.0		7.5 5.5		ns
t_{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	3.3 5.0	0 0		0 0		ns

SWITCHING WAVEFORMS







Input and output threshold voltage:
V_T = 50% Vcc for AC
V_H = Vcc for AC