FEATURES

- Wide supply voltage range 4.5V ~ 20V
- Input range 500mV beyond the rails
- Unity-gain stable
- Rail-to-rail output swing
- High slew rate 30V/μs
- GBWP 20MHz
- 30MHz -3dB Bandwidth
- Ultra-small Package MSOP-8 SOP-8. and TSSOP-8

APPLICATIONS

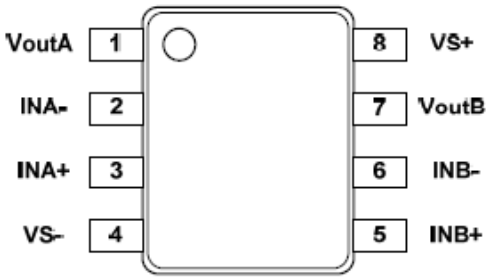
- TFT-LCD Reference Driver
- Touch-Screen Display
- Wireless LANs
- Personal Communication Devices
- Direct Access Arrangement
- Personal Digital Assistant (PDA)
- Active Filter
- Sampling ADC Amplifier
- ADC/DAC Buffer
- Electronic Notebook
- Office Automation

GENERAL DESCRIPTION

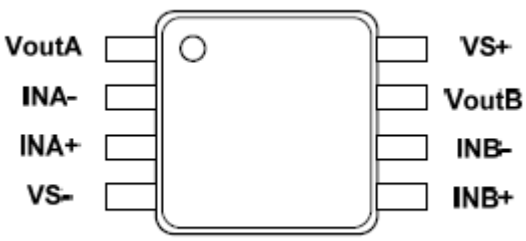
The EC5612 is a 100mA output current rail-to-rail dual channels operational amplifier with wide supply range from 4.5V to 20V while consumes only 3.0 mA per channel. It provides 0.5V beyond the supply rails of common mode input range and capability of rail-to-rail output swing as well. This enables the amplifier to offer maximum dynamic range at any supply voltage among many applications. A 20MHz gain bandwidth product allows EC5612 to perform more stable than other devices in Internet applications.

With features of 30V/μs high slew rate and 500ns of fast settling time, as well as 100mA (sink and source) of high output driving capability, the EC5612 is ideal for the requirements of flat panel Thin Film Transistor Liquid Crystal Displays (TFT-LCD) panel reference buffers application. Due to insensitive to power supply variation, EC5612 offers flexibility of use in multitude of applications such as battery power, portable devices and anywhere low power consumption is concerned. With standard operational amplifier pin assignment, the EC5612 is specified over the -40°C to +85°C temperature range.

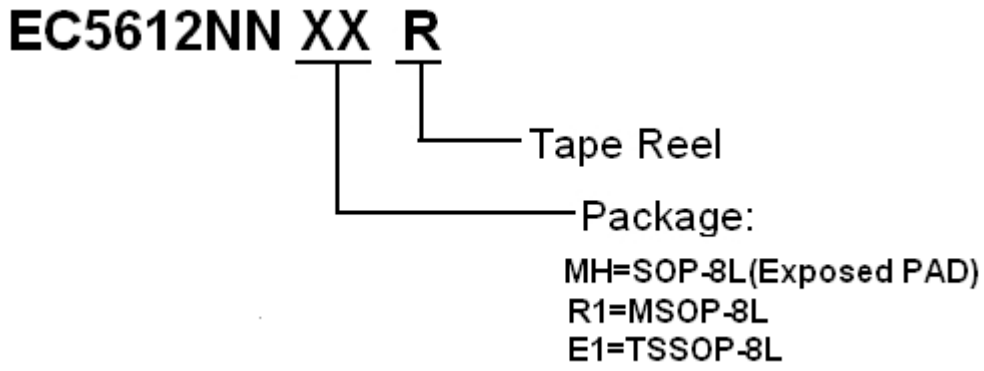
SOP 8



MSOP 8 / TSSOP-8



Ordering Information



Marking Information

Part No.	Package Type	Marking Information	Remark
EC5612NNMHR	SOP-8L (Exposed PAD)	EC5612 LLLLL YYWWT	1. LLLLL：Lot No 2. YYWW：Date Code 3. T：Internal Tracking Code
EC5612NNR1R	MSOP-8L	EC5612 LLLLL YYWWT	
EC5612NNE1R	TSSOP-8L	EC5612 LLLLL YYWWT	

ABSOLUTE MAXIMUM RATINGS (TA = 25 °C)

Values beyond absolute maximum ratings may cause permanent damage to the device. These are stress ratings only; functional device operation is not implied. Exposure to AMR conditions for extended periods may affect device reliability.

Supply Voltage between V_{S+} and V_{S-}	+20V	Storage Temperature	-65°C to +150°C
Input Voltage	$V_{S-}-0.5V$, $V_{S+}+0.5V$	Operating Temperature	-40°C to +85°C
Maximum Continuous Output Current	100mA	Lead Temperature	260°C
Maximum Die Temperature	+125°C	ESD Voltage	2kV

Important Note:
All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: TJ = TC = TA

ELECTRICAL CHARACTERISTICS

V_{S+}= +5V, V_{S-} = -5V, R_L = 10kΩ and C_L = 10pF to 0V, T_A = 25°C unless otherwise specified.

Parameter	Description	Condition	Min	Typ	Max	Units
Input Characteristics						
V_{OS}	Input Offset Voltage	V_{CM}= 0V		2	12	mV
TCV_{OS}	Average Offset Voltage Drift	[1]		5		µV/°C
I_B	Input Bias Current	V_{CM}= 0V		2	50	nA
R_{IN}	Input Impedance			1		GΩ
C_{IN}	Input Capacitance			1.35		pF
CMIR	Common-Mode Input Range		-5.0		+5.5	V
CMRR	Common-Mode Rejection Ratio	for V_{IN} from -0.5V to 5.5V	50	70		dB
A_{VOL}	Open-Loop Gain	0.5V ≤V_{OUT} ≤4.5V	75	90		dB
Output Characteristics						
V_{OL}	Output Swing Low	Vs+=8V,Vs-=-8V,I_L=-5mA		-7.92	-7.85	V
V_{OH}	Output Swing High	Vs+=8V,Vs-=-8V,I_L=5mA	7.85	7.92		V
I_{SC}	Short Circuit Current			±400		mA
I_{OUT}	Output Current			±100		mA
I_{pack}	I_{pack} Current	Source Current: I load V_{OUT} to GND		500		mA
		Sink Current: I load V_{OUT} to VDD				
Power Supply Performance						
PSRR	Power Supply Rejection Ratio	V_S is moved from ±2.25V to ±7.75V	60	80		dB
I_S	Supply Current (Per Amplifier)	No Load		3		mA
Dynamic Performance						
SR	Slew Rate [2]	Vs+=8V,Vs-=-8V, -4.0V ≤V_{OUT}≤4.0V, 20% to 80%	30	40		V/µs
t_S	Settling to +0.1% (AV = +1)	(AV = +1), V_O=2V Step		500		Ns
BW	-3dB Bandwidth	R_L = 10k , C_L=10pF		30		MHz
GBWP	Gain-Bandwidth Product	R_L = 10k , CL=10pF		20		MHz
PM	Phase Margin	RL = 10k , CL = 10 pF		50		Degrees
CS	Channel Separation	f = 1 MHz		75		dB
TSD	Thermal Shutdown			150		°C

1. Measured over operating temperature range
2. Slew rate is measured on rising and falling edges

TYPICAL PERFORMANCE CURVES

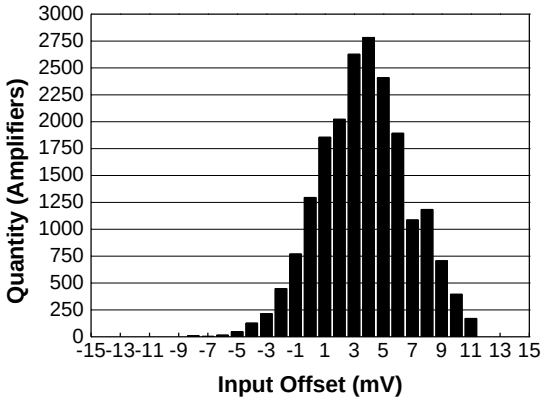


Figure (a) Input Offset Voltage Distribution

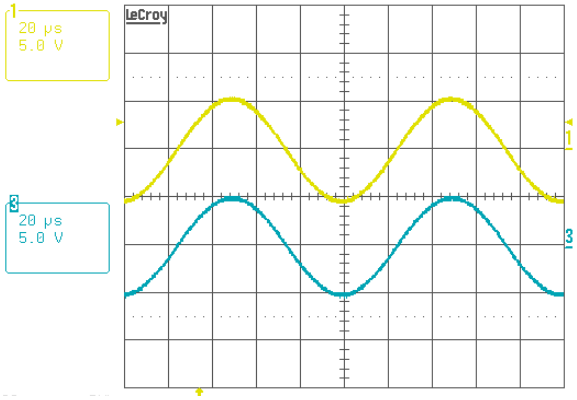


Figure (b) Rail to Rail Capability

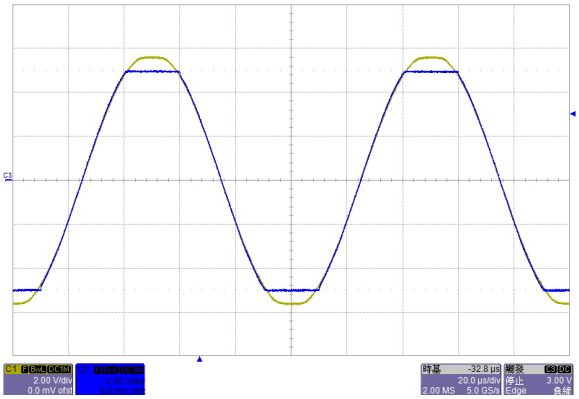


Figure (c) Input beyond the rails

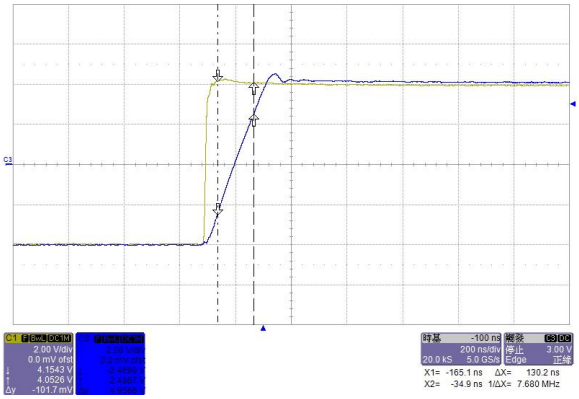


Figure (d) Large Signal Transient Response

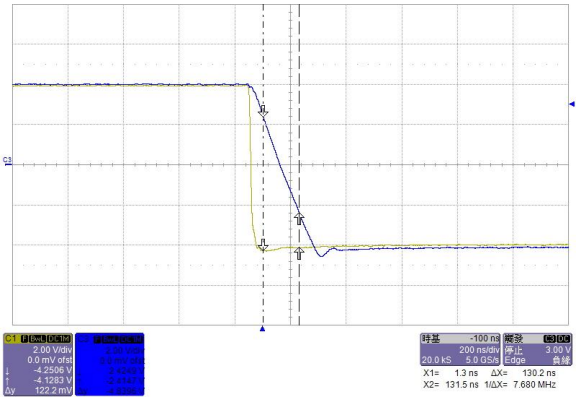


Figure (e) Large Signal Transient Response

TYPICAL PERFORMANCE CURVES

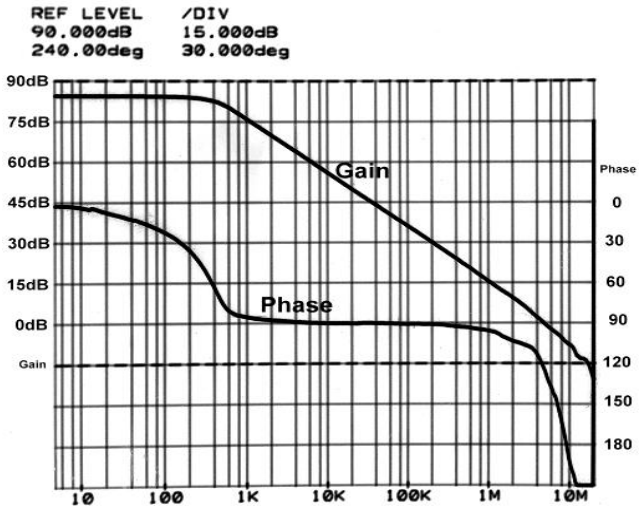


Figure (g) Open Loop Gain & Phase vs. Frequency

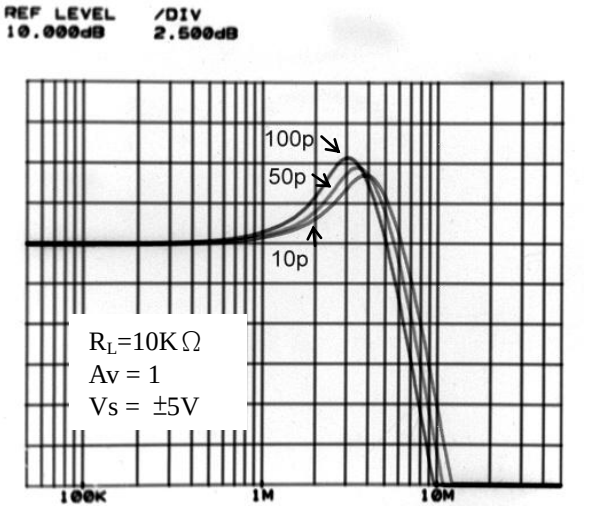


Figure (h) Frequency Response for Various C_L

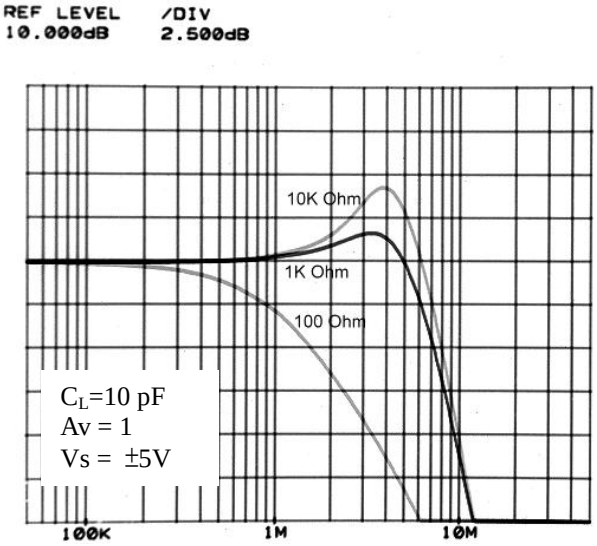


Figure (h) Frequency Response for Various R_L

APPLICATIONS INFORMATION

Product Description

The EC5612 rail-to-rail dual channels amplifier is built on an advanced high voltage CMOS process. It's beyond rails input capability and full swing of output range made itself an ideal amplifier for use in a wide range of general-purpose applications. The features of 30V/μS high slew rate, fast settling time, 20MHz of GBWP as well as high output driving capability have proven the EC5612 a good voltage reference buffer for TFT-LCD for applications. High phase margin make the EC5612 ideal for Connected in voltage follower mode for high drive applications

Supply Voltage, Input Range and Output Swing

The EC5612 can be operated with a single nominal wide supply voltage ranging from 4.5V to 20V with stable performance over operating temperatures of -40°C to +85 °C. With 500mV greater than rail-to-rail input common mode voltage range and 80dB of Common Mode Rejection Ratio, the EC5612 allows a wide range sensing among many applications without having any concerns over exceeding the range and no compromise in accuracy. The output swings of the EC5612 typically extend to within 80mV of positive and negative supply rails with load currents of 5mA. The output voltage swing can be even closer to the supply rails by merely decreasing the load current. Figure 1 shows the input and output waveforms for the device in the unity-gain configuration. The amplifier is operated under ±5V supply with a 10k Ω load connected to GND. The input is a 10Vp-p sinusoid. An approximately 9.985 Vp-p of output voltage swing can be easily achieved.

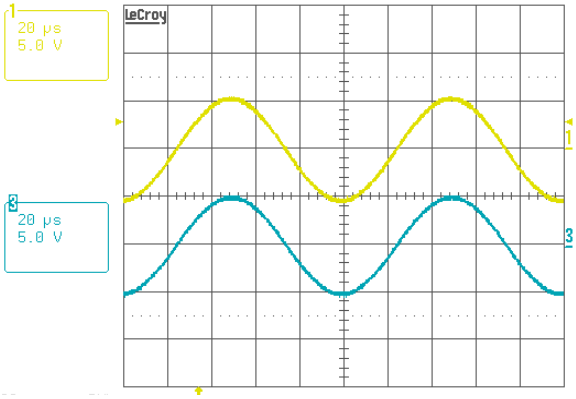


Figure 1. Operation with Rail-to-Rail Input and Output

Output Short Circuit Current Limit

A +/-400mA short circuit current will be limited by the EC5612 if the output is directly shorted to the positive or the negative supply. For an indefinitely output short circuit, the power dissipation could easily increase such that the device may be damaged. The internal metal interconnections are well designed to prevent the output continuous current from exceeding +/-100 mA such that the maximum reliability can be well maintained.

Output Phase Reversal

The EC5612 is designed to prevent its output from being phase reversal as long as the input voltage is limited from V_{S-} − 0.5V to V_{S+} + 0.5V. Figure 2 shows a photo of the device output with its input voltage driven beyond the supply rails. Although the phase of the device's output will not be reversed, the input's over-voltage should be avoided. An improper input voltage exceeds supply range by more than 0.6V may result in an over stress damage.

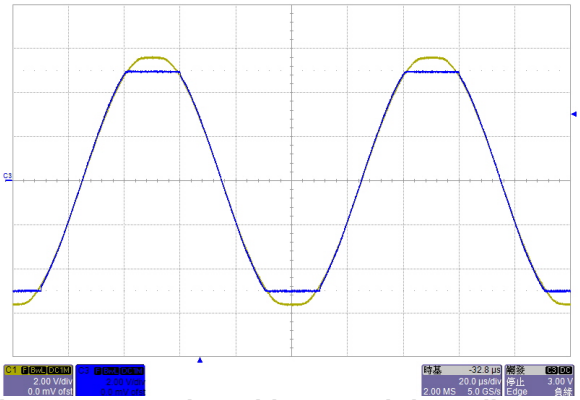


Figure 2. Operation with Beyond-the Rails Input

Power Dissipation

The EC5612 is designed for maximum output current capability. Even though momentary output shorted to ground causes little damage to the device.

For the high drive amplifier EC5612, it is possible to exceed the 'absolute-maximum junction temperature' under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if load conditions need to be modified for the amplifier to remain in the safe operating area. The maximum power dissipation allowed in a package is determined according to:

$$P_{Dmax} = \frac{T_{Jmax} - T_{Amax}}{\Theta_{JA}}$$

Where:

T_{Jmax} = Maximum Junction Temperature

T_{Amax}= Maximum Ambient Temperature

$_{JA}$ = Thermal Resistance of the Package

P_{Dmax} = Maximum Power Dissipation in the Package.

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the loads, or:

$P_{Dmax} = {}_{i}[V_S * I_{Smax} + (V_{S+} - V_O) * I_L]$

When sourcing, and

$P_{Dmax} = {}_{i}[V_S * I_{Smax} + (V_O - V_{S-}) * I_L]$

When sinking.

Where:

i = 1 to 4

V_S = Total Supply Voltage

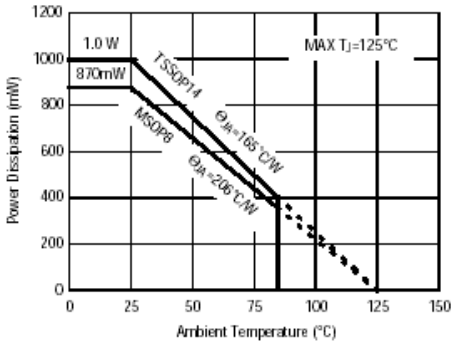
I_{Smax} = Maximum Supply Current Per Amplifier

V_O = Maximum Output Voltage of the Application

I_L= Load current

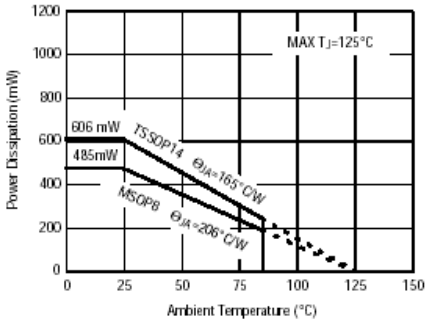
R_L= Load Resistance = $(V_{S+} - V_O)/I_L = (V_O - V_{S-})/ I_L$

A calculation for R_L to prevent device from overheat can be easily solved by setting the two P_{Dmax} equations equal to each other. Figure 3 and Figure 4 show the relationship between package power dissipation and ambient temperature under the JEDEC JESD 51-7 high effective thermal conductivity test board and SEMI G42-88 single layer test board respectively. From these charts, conditions of the device overheat then can be easily found. The maximum safe power dissipation can be found graphically, based on the package type and the ambient temperature. By using the previous equation, it is a simple matter to see if P_{DMAX} exceeds the device's power de-rating curves. To ensure proper operation, it is important to observe the recommended de-rating curves shown in Figure 3 and Figure 4.



JEDEC JESD 51-7 High Effective Thermal Conductivity Test Board

Figure 3. Package Power Dissipation vs. Ambient Temperature



SEMI G42-88 Single Layer Test Board

Figure 4. Package Power Dissipation vs. Ambient Temperature

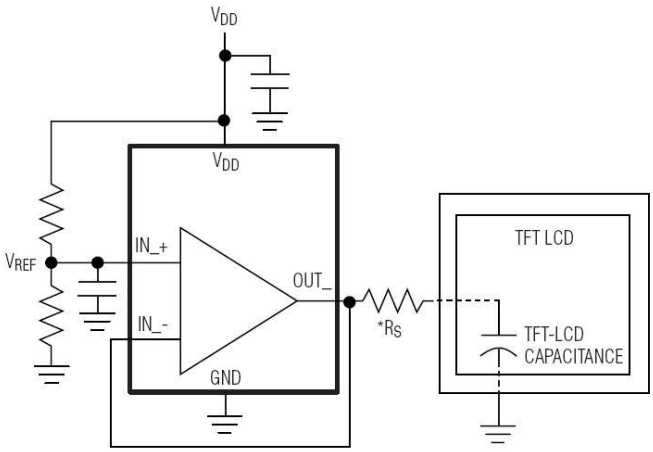
Driving Capacitive Loads

The EC5612 is designed to drive a wide range of capacitive loads. In addition, the output current handling capability of the device allows for good slewing characteristics even with large capacitive loads. The combination of these features make the EC5612 ideally for applications such as TFT LCD panel buffers, ADC input amplifiers, etc. As load capacitance increases, the -3dB bandwidth will decrease and peaking can occur. Depending on the application, it must be necessary to reduce peaking and to improve device stability. To improve device stability a snubber circuit or a series resistor must be added to the output of the EC5612.

A snubber is a shunt load consisting of a resistor in series with a capacitor. An optimized snubber can improve the phase margin and the stability of the EC5612. Another method to reduce peaking is to add a series out put resistor (typically between 5Ω to 50Ω). Depending on the capacitive loading, a small value resistor may be the most appropriate choice to minimize any reduction in gain.

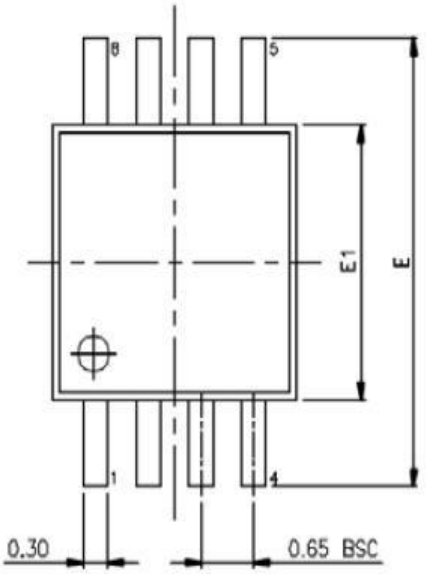
Power Supply Bypassing and Printed Circuit Board Layout

With high phase margin, the EC5612 performs stable gain at high frequency. Like any high-frequency device, good layout of the printed circuit board usually comes with optimum performance. Ground plane construction is highly recommended, lead lengths should be as short as possible and the power supply pins must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the VS- pin is connected to ground, a 0.1 µF ceramic capacitor should be placed from VS+ pin to VS- pin as a bypassing capacitor. A 4.7µF tantalum capacitor should then be connected in parallel, placed in the region of the amplifier. One 4.7µF capacitor may be used for multiple devices. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used.



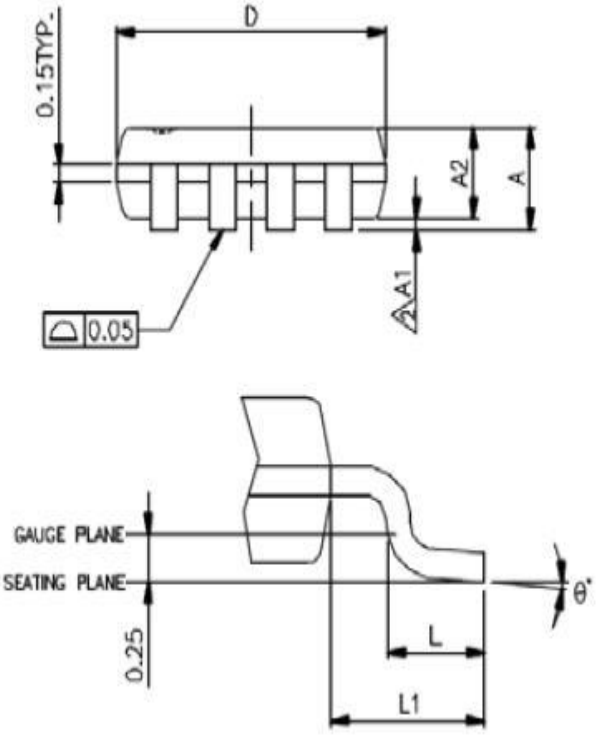
*RS BE NEEDED FOR SOME APPLICATIONS.

OUTLINE DIMENSIONS
MSOP 8



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.10
A1	0.00	–	0.15
A2	0.75	0.85	0.95
D		3.00 BSC	
E		4.90 BSC	
E1		3.00 BSC	
L	0.40	0.60	0.80
L1		0.95 REF	
θ°	0	–	8

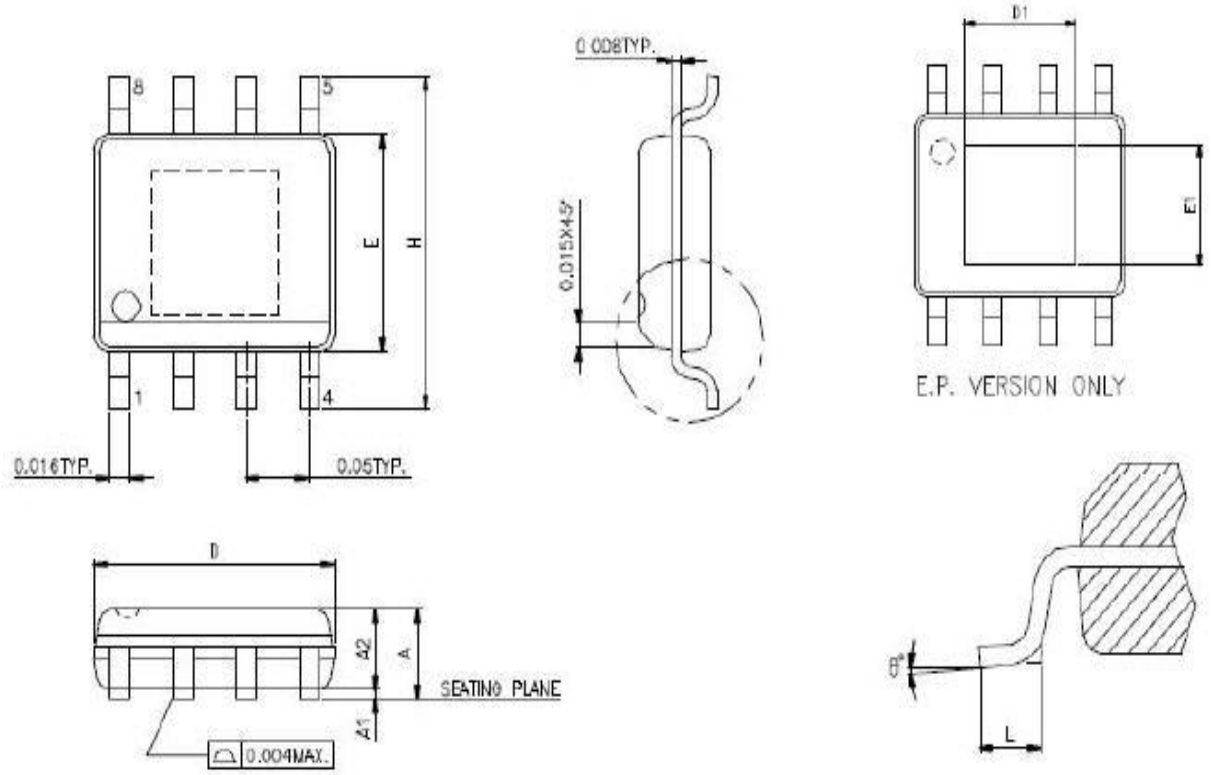
UNIT : MM



NOTES:
1. JEDEC OUTLINE : MO-187 AA
2. DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
3. DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
4. DIMENSION '0.22' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE '0.22' DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPAC BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 MM.
5. DIMENSIONS 'D' AND 'E1' TO BE DETERMINED AT DATUM PLANE H .

OUTLINE DIMENSIONS

SOP 8 (EXPOSED PAD)



DIMN	INCH	
	MIN	MAX
A	0.053	0.069
A1	0.002	0.006
A2	—	0.059
D	0.189	0.196
E	0.150	0.157
H	0.228	0.244
L	0.016	0.050
θ°	0	8

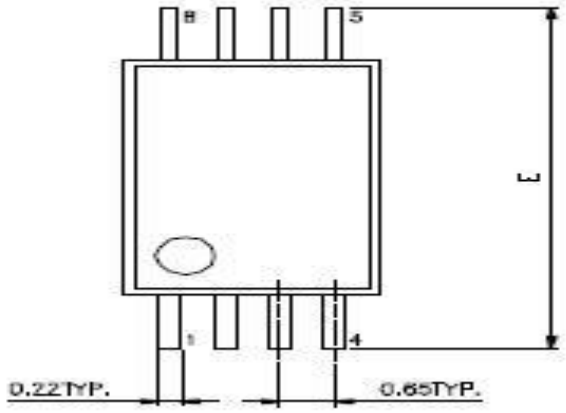
NOTE:

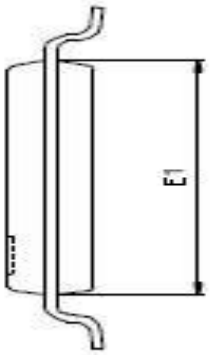
1. JEDEC OUTLINE: N/A.
2. DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONDS AND GATE BURRS SHALL NOT EXCEED 0.15mm (.006in) PER SIDE.
3. DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS.INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25mm (.010in) PER SIDE

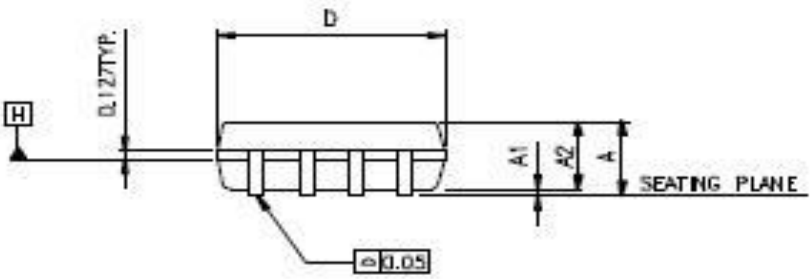
THERMALLY ENHANCED DIMENSIONS

PAD SIZE	INCH	
	E1	D1
90X90E	0.081REF	0.081REF

OUTLINE DIMENSIONS
TSSOP 8

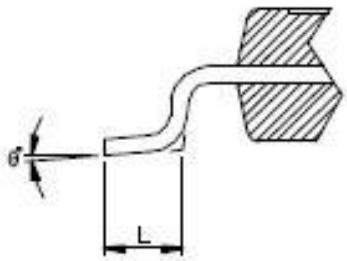






SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.96	1.01	1.06
D	2.90	3.00	3.10
E		6.40 BSC	
E1	4.30	4.40	4.50
L	0.45	0.60	0.75
θ°	0	–	8

UNIT : MM



NOTES:
1. JEDEC OUTLINE : MO-153 AA
2. DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
3. DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
4. DIMENSION '0.22' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE '0.22' DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPAC BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 MM.
5. DIMENSIONS 'D' AND 'E1' TO BE DETERMINED AT DATUM PLANE H.