128Kx8 Monolithic SRAM, SMD 5962-89598

FEATURES

- Access Times of 15*, 17, 20, 25, 35, 45, 55ns
- CS# and OE# Functions for Bus Control
- 2V Data Retention (EDI88128LPS)
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks
- Organized as 128Kx8
- Commercial, Industrial and Military Temperature Ranges
- Thru-hole and Surface Mount Packages JEDEC Pinout
  - 32 pin Ceramic DIP, 400 mil (Package 102)
  - 32 pin Ceramic DIP, 600 mil (Package 9)
  - 32 lead Ceramic ZIP (Package 100)
  - 32 lead Ceramic SOJ (Package 140)
  - 32 pad Ceramic LCC (Package 141)
  - 32 lead Ceramic Flatpack (Package 142)
- Single +5V (±10%) Supply OperationThe EDI88128CS is a high speed, high performance, 128Kx8 megabit density Monolithic CMOS Static RAM.

The device has eight bi-directional input-output lines to provide simultaneous access to all bits in a word. An automatic power down feature permits the on-chip circuitry to enter a very low standby mode and be brought back into operation at a speed equal to the address access time.

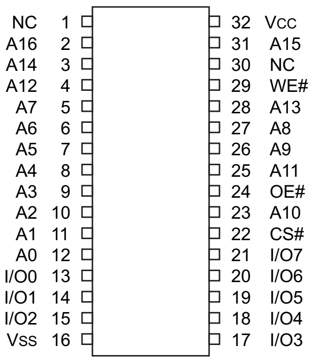
A Low Power version with 2V Data Retention (EDI88128LPS) is also available for battery back-up opperation. Military product is available compliant to MIL-PRF-38535.

* 15ns access time is advanced information, contact factory for availability.

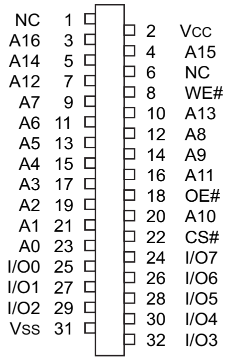
This product is subject to change without notice.

FIGURE 1 – PIN CONFIGURATION

32 DIP
32 SOJ
32 LCC
32 FLATPACK
TOP VIEW



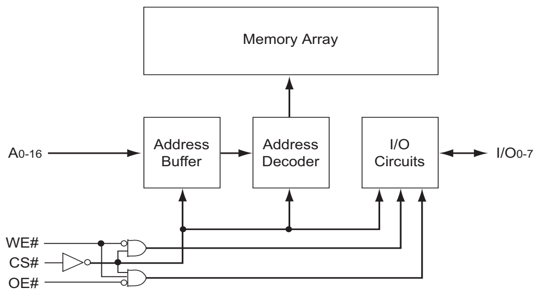
32 ZIP
TOP VIEW



PIN DESCRIPTION

I/O0-7	Data Inputs/Outputs
A0-16	Address Inputs
WE#	Write Enable
CS#	Chip Select
OE#	Output Enable
VCC	Power (+5V ±10%)
VSS	Ground
NC	Not Connected

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Voltage on any pin relative to V_{SS}	-0.5 to 7.0	V
Operating Temperature T_A (Ambient)		
Commercial	0 to +70	°C
Industrial	-40 to +85	°C
Military	-55 to +125	°C
Storage Temperature, Plastic	-65 to +150	°C
Power Dissipation	1.5	W
Output Current	20	mA
Junction Temperature, T_J	175	°C

NOTE:
Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TRUTH TABLE

OE#	CS#	WE#	Mode	Output	Power
X	H	X	Standby	High Z	Icc2, Icc3
H	L	H	Output Deselect	High Z	Icc1
L	L	H	Read	Data Out	Icc1
X	L	L	Write	Data In	Icc1

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} +0.5	V
Input Low Voltage	V_{IL}	-0.3	—	+0.8	V

CAPACITANCE

T_A = +25°C

Parameter	Symbol	Condition	Max		Unit
			LLC	CSOJ, ZIP, DIP, Flatpack	
Address Lines	C_I	V_{IN} = V_{CC} or V_{SS}, f = 1.0MHz	12		pF
Data Lines	C_O	V_{OUT} = V_{CC} or V_{SS}, f = 1.0MHz	14		pF

These parameters are sampled, not 100% tested.

DC CHARACTERISTICS

V_{CC} = 5.0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Input Leakage Current	I_{LI}	V_{IN} = 0V to V_{CC}		—	—	±5	µA
Output Leakage Current	I_{LO}	$V_{I/O}$ = 0V to V_{CC}		—	—	±10	µA
Operating Power Supply Current	I_{CC1}	WE#, CS# = V_{IL}, $I_{I/O}$ = 0mA, CS2 = V_{IH}	(15-17ns) (20ns) (25-55ns)	— — —		300 225 200	mA mA mA
Standby (TTL) Power Supply Current	I_{CC2}	CS# ≥ V_{IH}, V_{IN} ≤ V_{IH} or ≥ V_{IL}	(17-55ns) (15ns)	— —		25 60	mA mA
Full Standby Power Supply Current	I_{CC3}	CS# ≥ V_{CC} -0.2V V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2V	CS (17-55ns) CS (15ns) LPS	— — —	3 — —	10 15 5	mA mA mA
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA		—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA		2.4	—	—	V

NOTE: DC test conditions : V_{IL} = 0.3V, V_{IH} = V_{CC} -0.3V

AC CHARACTERISTICS – READ CYCLE (15 to 20ns)

V_{CC} = 5.0V, Vss = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol		15ns*		17ns		20ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	15		17		20		ns
Address Access Time	t_{AVQV}	t_{AA}		15		17		20	ns
Chip Enable Access Time	t_{ELQV}	t_{ACS}		15		17		20	ns
Chip Enable to Output in Low Z (1)	t_{ELQX}	t_{CLZ}	3		3		3		ns
Chip Disable to Output in High Z (1)	t_{EHQZ}	t_{CHZ}		8		8		10	ns
Output Hold from Address Change	t_{AVQX}	t_{OH}	0		0		0		ns
Output Enable to Output Valid	t_{GLQV}	t_{OE}		6		6		8	ns
Output Enable to Output in Low Z (1)	t_{GLQX}	t_{OLZ}	0		0		0		ns
Output Disable to Output in High Z(1)	t_{GHQZ}	t_{OHZ}		6		6		8	ns
Chip Enable to Power Up (1)	t_{ELICCH}	t_{PU}	0		0		0		ns
Chip Enable to Power Down (1)	t_{EHICCL}	t_{PD}		15		17		20	ns

1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS – READ CYCLE (25 to 55ns)

V_{CC} = 5.0V, Vss = 0V, -55°C ≤ T_A ≤ +125°C

	Symbol		25ns		35ns		45ns		55ns		
Parameter	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	Units
Read Cycle Time	t_{AVAV}	t_{RC}	25		35		45		55		ns
Address Access Time	t_{AVQV}	t_{AA}		25		35		45		55	ns
Chip Enable Access Time	t_{ELQV}	t_{ACS}		25		35		45		55	ns
Chip Enable to Output in Low Z (1)	t_{ELQX}	t_{CLZ}	3		3		3		3		ns
Chip Disable to Output in High Z (1)	t_{EHQZ}	t_{CHZ}		12		20		20		20	ns
Output Hold from Address Change	t_{AVQX}	t_{OH}	0		0		0		0		ns
Output Enable to Output Valid	t_{GLQV}	t_{OE}		10		15		20		25	ns
Output Enable to Output in Low Z (1)	t_{GLQX}	t_{OLZ}	0		0		0		0		ns
Output Disable to Output in High Z(1)	t_{GHQZ}	t_{OHZ}		10		15		20		20	ns
Chip Enable to Power Up (1)	t_{ELICCH}	t_{PU}	0		0		0		0		ns
Chip Enable to Power Down (1)	t_{EHICCL}	t_{PD}		25		35		45		55	ns

1. This parameter is guaranteed by design but not tested.

AC TEST CONDITIONS

Figure 1

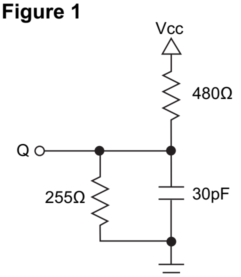
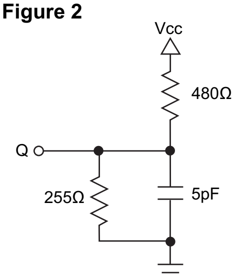


Figure 2



Input Pulse Levels	Vss to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

NOTE: For t_{EHQZ}, t_{GHQZ} and t_{WLQZ}, CL = 5pF Figure 2

AC CHARACTERISTICS – WRITE CYCLE (15 to 20ns)

V_{CC} = 5.0V, Vss = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol JEDEC	Symbol Alt.	15ns* Min	15ns* Max	17ns Min	17ns Max	20ns Min	20ns Max	Units
Write Cycle Time	t_{AVAV}	t_{WC}	15		17		20		ns
Chip Enable to End of Write	t_{ELWH} t_{ELEH}	t_{CW} t_{CW}	12 12		13 13		15 15		ns ns
Address Setup Time	t_{AVWL} t_{AVEL}	t_{AS} t_{AS}	0 0		0 0		0 0		ns ns
Address Valid to End of Write	t_{AVWH} t_{AVEH}	t_{AW} t_{AW}	12 12		13 13		15 15		ns ns
Write Pulse Width	t_{WLWH} t_{WLEH}	t_{WP} t_{WP}	12 12		13 13		15 15		ns ns
Write Recovery Time	t_{WHAX} t_{EHAX}	t_{WR} t_{WR}	0 0		0 0		0 0		ns ns
Data Hold Time	t_{WHDX} t_{EHDX}	t_{DH} t_{DH}	0 0		0 0		0 0		ns ns
Write to Output in High Z (1)	t_{WLQZ}	t_{WHZ}	0	7	0	8	0	8	ns
Data to Write Time	t_{DVWH} t_{DVEH}	t_{DW} t_{DW}	7 7		8 8		10 10		ns ns
Output Active from End of Write (1)	t_{WHQX}	t_{WLZ}	3		3		3		ns

1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS – WRITE CYCLE (25 to 55ns)

V_{CC} = 5.0V, Vss = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol JEDEC	Symbol Alt.	25ns Min	25ns Max	35ns Min	35ns Max	45ns Min	45ns Max	55ns Min	55ns Max	Units
Write Cycle Time	t_{AVAV}	t_{WC}	25		35		45		55		ns
Chip Enable to End of Write	t_{E1LWH} t_{ELEH}	t_{CW} t_{CW}	20 20		25 25		35 35		45 45		ns ns
Address Setup Time	t_{AVWL} t_{AVEL}	t_{AS} t_{AS}	0 0		0 0		0 0		0 0		ns ns
Address Valid to End of Write	t_{AVWH} t_{AVEH}	t_{AW} t_{AW}	20 20		25 25		35 35		45 45		ns ns
Write Pulse Width	t_{WLWH} t_{WLEH}	t_{WP} t_{WP}	20 20		30 30		30 30		35 35		ns ns
Write Recovery Time	t_{WHAX} t_{EHAX}	t_{WR} t_{WR}	0 0		0 0		5 5		5 5		ns ns
Data Hold Time	t_{WHDX} t_{EHDX}	t_{DH} t_{DH}	0 0		0 0		0 0		0 0		ns ns
Write to Output in High Z (1)	t_{WLQZ}	t_{WHZ}	0	10	0	13	0	15	0	20	ns
Data to Write Time	t_{DVWH} t_{DVEH}	t_{DW} t_{DW}	15 15		20 20		20 20		25 25		ns ns
Output Active from End of Write (1)	t_{WHQX}	t_{WLZ}	3		3		3		3		ns

1. This parameter is guaranteed by design but not tested.

FIGURE 2 – TIMING WAVEFORM - READ CYCLE

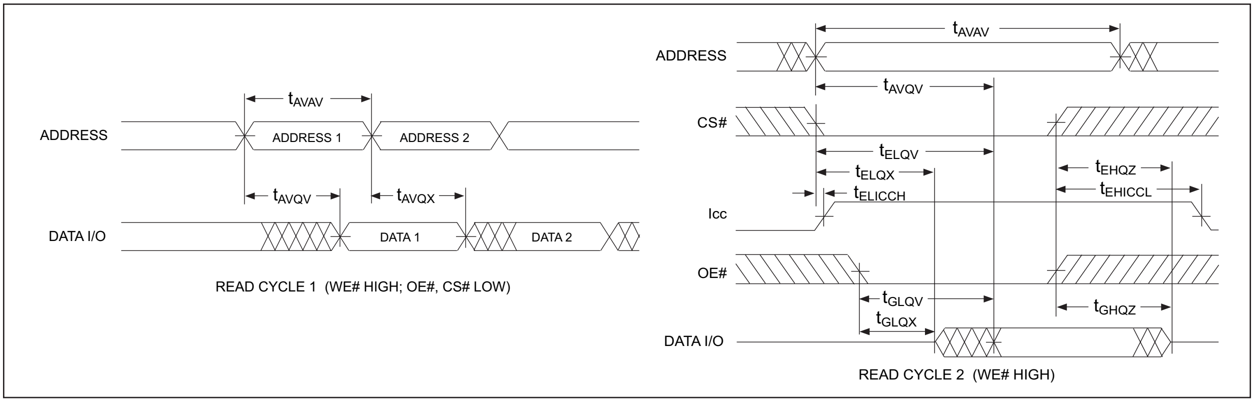


FIGURE 3 – WRITE CYCLE - WE# CONTROLLED

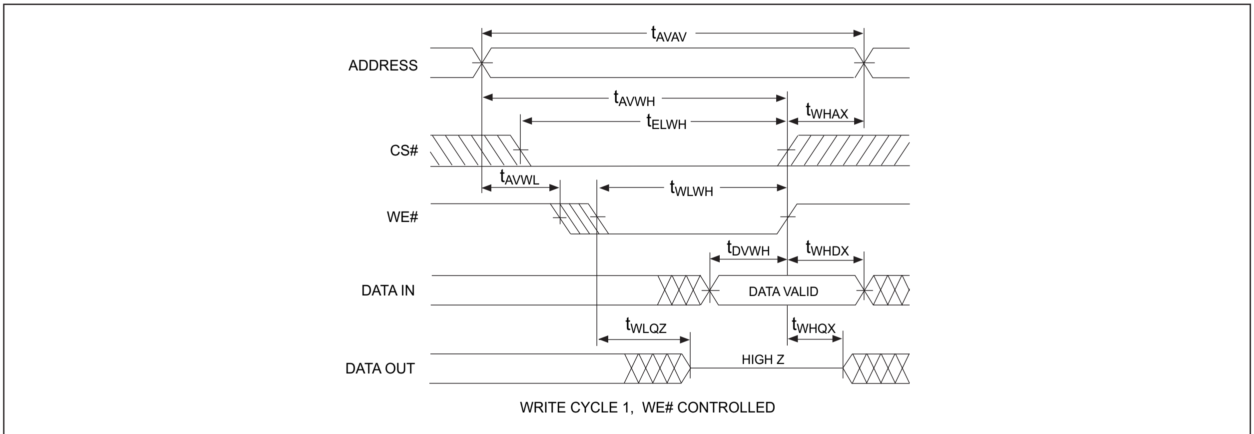
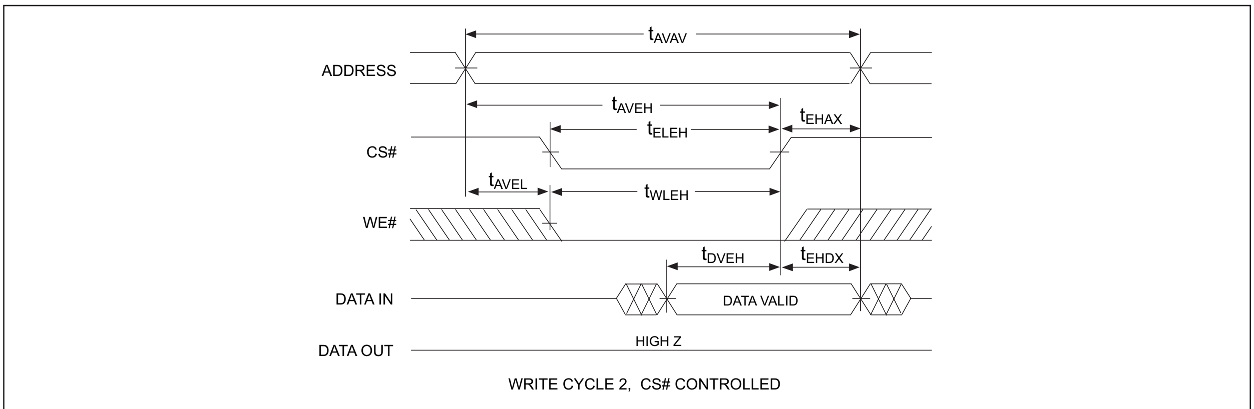


FIGURE 4 – WRITE CYCLE - CS# CONTROLLED



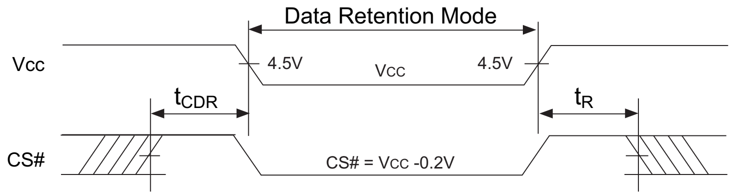
DATA RETENTION CHARACTERISTICS (EDI88128LPA only)

$-55°C \leq T_A \leq +125°C$

Characteristic Low Power Version only	Sym	Conditions	Min	Typ	Max	Units
Data Retention Voltage Data Retention Quiescent Current	V_{CC} I_{CCDR}	V_{CC} = 2.0V CS# ≥ V_{CC} -0.2V	2 –	– 0.5	– 2	V mA
Chip Disable to Data Retention Time (1) Operation Recovery Time (1)	T_{CDR} T_R	V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2V	0 T_{AVAV}*	– –	– –	ns ns

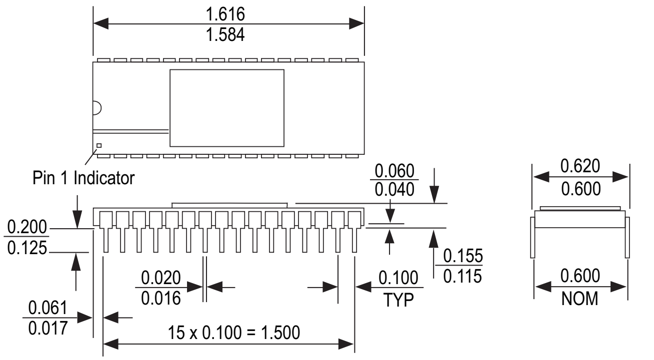
NOTE:
1. Parameter guaranteed by design, but not tested.
* Read Cycle Time

FIGURE 5 – DATA RETENTION - CS# CONTROLLED



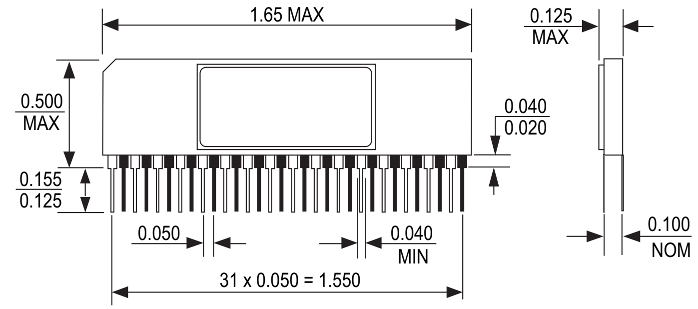
DATA RETENTION, CS# CONTROLLED

PACKAGE 9: 32 PIN SIDEBRAZED CERAMIC DIP (600mils wide)



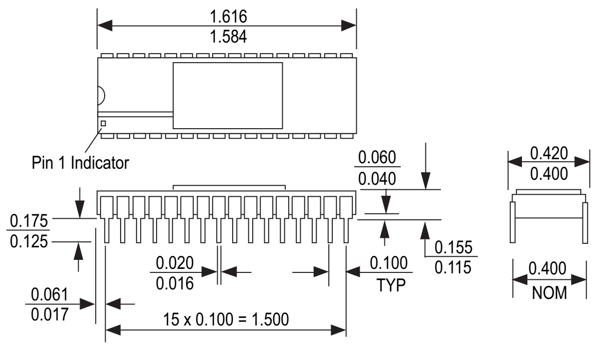
ALL DIMENSIONS ARE IN INCHES

PACKAGE 100: 32 LEAD CERAMIC ZIP



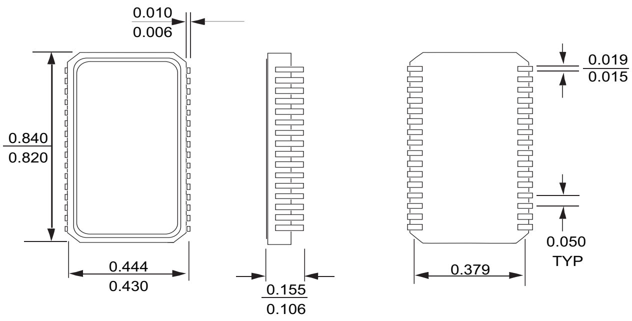
ALL DIMENSIONS ARE IN INCHES

PACKAGE 102: 32 PIN SIDEBRAZED CERAMIC DIP (400mils wide)



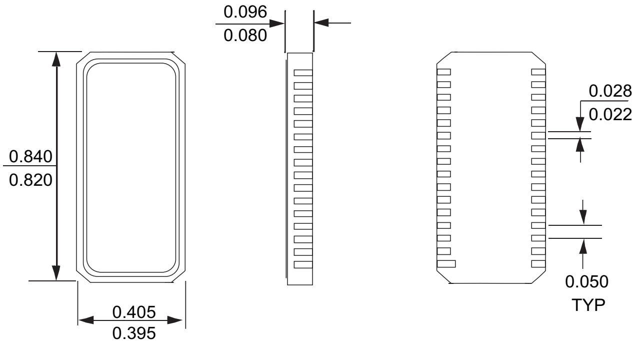
ALL DIMENSIONS ARE IN INCHES

PACKAGE 140: 32 LEAD CERAMIC SOJ



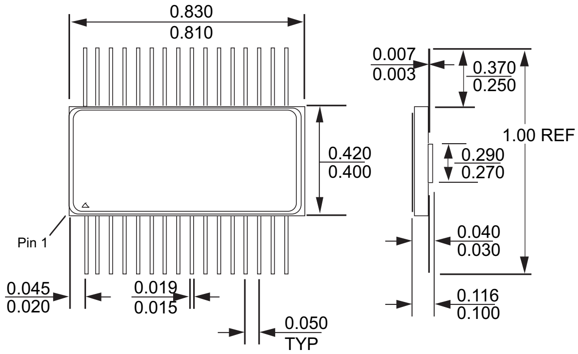
ALL DIMENSIONS ARE IN INCHES

PACKAGE 141: 32 PAD CERAMIC LCC



ALL DIMENSIONS ARE IN INCHES

PACKAGE 142: 32 PIN CERAMIC FLATPACK



ALL DIMENSIONS ARE IN INCHES

ORDERING INFORMATION

EDI 8 8 128 CS X X X

WHITE ELECTRONIC DESIGNS

SRAM

ORGANIZATION, 128Kx8

TECHNOLOGY:
- CS = CMOS Standard Power
- LPS = Low Power

ACCESS TIME (ns)

PACKAGE TYPE:
- C = 32 lead Sidebrazed DIP, 600 mil (Package 9)
- F = 32 lead Ceramic Flatpack (Package 142)
- L = 32 pad Ceramic LCC (Package 141)
- N = 32 lead Ceramic SOJ (Package 140)
- T = 32 lead Sidebrazed DIP, 400 mil (Package 102)
- Z = 32 lead Ceramic ZIP (Package 100)

DEVICE GRADE:

B = MIL-STD-883 Compliant	
M = Military Screened	-55°C to +125°C
I = Industrial	-40°C to +85°C
C = Commercial	0°C to +70°C