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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL4584C
Horizontal Genlock, 4 F_{SC}

Features

- 36 MHz, general purpose PLL
- 4 F_{SC} based timing (use the EL4585 for 8 F_{SC})
- Compatible w/EL4583 Sync Separator
- VCXO, Xtal, or LC tank oscillator
- $<$2 ns jitter (VCXO)
- User controlled PLL capture and lock
- Compatible with NTSC and PAL TV formats
- 8 pre-programmed TV scan rate clock divisors
- Selectable external divide for custom ratios
- Single 5V, low current operation

Applications

- Pixel Clock regeneration
- Video compression engine (MPEG) clock generator
- Video capture or digitization
- PIP (Picture in Picture) timing generator
- Text or graphics overlay timing

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL4584CN	-40°C to +85°C	16-Pin DIP	MDP0031
EL4584CS	-40°C to +85°C	16-Lead SO	MDP0027

For 6Fsc and 8Fsc clock frequencies, see EL4585 datasheet.

Demo Board

A demo PCB is available for this product. Request "EL4584/5 Demo Board".

General Description

The EL4584C is a PLL (Phase Lock Loop) sub system, designed for video applications but also suitable for general purpose use up to 36 MHz. In a video application this device generates a TTL/CMOS compatible Pixel Clock (Clk Out) which is a multiple of the TV Horizontal scan rate, and phase locked to it.

The reference signal is a horizontal sync signal, TTL/CMOS format, which can be easily derived from an analog composite video signal with the EL4583 Sync Separator. An input signal to "coast" is provided for applications were periodic disturbances are present in the reference video timing such as VTR head switching. The Lock detector output indicates correct lock.

The divider ratio is four ratios for NTSC and four similar ratios for the PAL video timing standards, by external selection of three control pins. These four ratios have been selected for common video applications including 4 F_{SC}, 3 F_{SC}, 13.5 MHz (CCIR 601 format) and square picture elements used in some workstation graphics. To generate 8 F_{SC}, 6 F_{SC}, 27 MHz (CCIR 601 format) etc. use the EL4585, which includes an additional divide by 2 stage.

For applications where these frequencies are inappropriate or for general purpose PLL applications the internal divider can be bypassed and an external divider chain used.

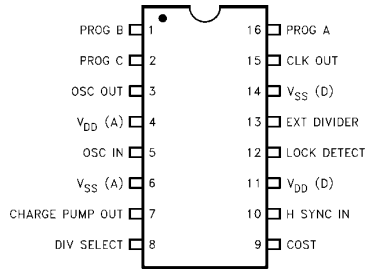
FREQUENCIES and DIVISORS

Function	3Fsc	CCIR 601	Square	4Fsc
Divisor	851	864	944	1135
PAL Fosc (MHz)	13.301	13.5	14.75	17.734
Divisor	682	858	780	910
NTSC Fosc (MHz)	10.738	13.5	12.273	14.318

CCIR 601 Divisors yield 720 pixels in the portion of each line for NTSC and PAL.
Square pixels format gives 640 pixels for NTSC and 768 pixels for PAL in the active portion.
3Fsc numbers do not yield integer divisors.

Connection Diagram

EL4584 SO, P-DIP Packages



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Absolute Maximum Ratings (T_A = 25°C)

V_{CC} Supply	7V	Operating Junction Temp	125°C
Storage Temperature	−65°C to +150°C	Power Dissipation	400 mW
Lead Temperature	260°C	Oscillator Frequency	36 MHz
Pin Voltages	−0.5V to V_{CC} + 0.5V		
Operating Ambient Temperature Range	−40°C to +85°C		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics (V_{DD} = 5V, T_A = 25°C unless otherwise noted)

Parameter	Conditions	Temp	Min	Typ	Max	Test Level	Units
I_{DD}	V_{DD} = 5V (Note 1)	25°C		2	4	I	mA
V_{IL} Input Low Voltage		25°C			1.5	I	V
V_{IH} Input High Voltage		25°C	3.5			I	V
I_{IL} Input Low Current	All inputs except COAST, V_{IN} = 1.5V	25°C	−100			I	nA
I_{IH} Input High Current	All inputs except COAST, V_{IN} = 3.5V	25°C			100	I	nA
I_{IL} Input Low Current	COAST pin, V_{IN} = 1.5V	25°C	−100	−60		I	µA
I_{IH} Input High Current	COAST pin, V_{IN} = 3.5V	25°C		60	100	I	µA
V_{OL} Output Low Voltage	Lock Det, I_{OL} = 1.6mA	25°C			0.4	I	V
V_{OH} Output High Voltage	Lock Det, I_{OH} = −1.6mA	25°C	2.4			I	V
V_{OL} Output Low Voltage	CLK, I_{OL} = 3.2mA	25°C			0.4	I	V
V_{OH} Output High Voltage	CLK, I_{OH} = −3.2mA	25°C	2.4			I	V
V_{OL} Output Low Voltage	OSC Out, I_{OL} = 200µA	25°C			0.4	I	V
V_{OH} Output High Voltage	OSC Out, I_{OH} = −200µA	25°C	2.4			I	V
I_{OL} Output Low Current	Filter Out, V_{OUT} = 2.5V	25°C	200	300		I	µA
I_{OH} Output High Current	Filter Out, V_{OUT} = 2.5V	25°C		−300	−200	I	µA
I_{OL}/I_{OH} Current Ratio	Filter Out, V_{OUT} = 2.5V	25°C	1.05	1.0	0.95	I	
I_{LEAK} Filter Out	Coast Mode, $V_{DD} > V_{OUT} > 0V$	25°C	−100	±1	100	I	nA

Note 1: All inputs to 0V, COAST floating.

TD is 3.5in

AC Electrical Characteristics (V_{DD} = 5V, T_A = 25°C unless otherwise noted)

Parameter	Conditions	Temp	Min	Typ	Max	Test Level	Units
VCO Gain @ 20 MHz	Test Circuit 1	25°C		15.5		V	dB
H-sync S/N Ratio	V_{DD} = 5V (Note 2)	25°C	35			V	dB
Jitter	VCXO Oscillator	25°C		1		V	ns
Jitter	LC Oscillator (Typ)	25°C		10		V	ns

Note 2: Noisy video signal input to EL4583C, H-sync input to EL4584C. Test for positive signal lock.

Pin Description

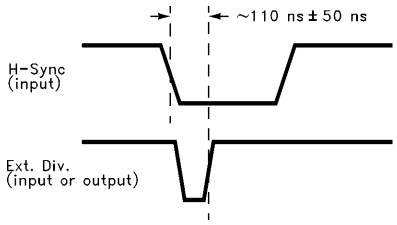
Pin No.	Pin Name	Function
16,1,2	Prog A,B,C	Digital inputs to select ÷ N value for internal counter. See table below for values.
3	Osc/VCO Out	Output of internal inverter/oscillator. Connect to external crystal or LC tank VCO circuit.
4	V_{DD} (A)	Analog positive supply for oscillator, PLL circuits.
5	Osc/VCO In	Input from external VCO.
6	V_{SS} (A)	Analog ground for oscillator, PLL circuits.
7	Charge Pump Out	Connect to loop filter. If the H-sync phase is leading or H-sync frequency > CLK ÷ N, current is pumped into the filter capacitor to increase VCO frequency. If H-sync phase is lagging or frequency < CLK ÷ N, current is pumped out of the filter capacitor to decrease VCO frequency. During coast mode or when locked, charge pump goes to a high impedance state.
8	Div Select	Divide select input. When high, the internal divider is enabled and EXT DIV becomes a test pin, outputting CLK ÷ N. When low, the internal divider is disabled and EXT DIV is an input from an external ÷ N.
9	Coast	Tri-state logic input. Low(< ⅓ * V_{CC}) = normal mode, Hi Z(or ⅓ to ⅔ * V_{CC}) = fast lock mode, High(> ⅔ * V_{CC}) = coast mode.
10	H-sync In	Horizontal sync pulse (CMOS level) input.
11	V_{DD} (D)	Positive supply for digital, I/O circuits.
12	Lock Det	Lock Detect output. Low level when PLL is locked. Pulses high when out of lock.
13	Ext Div	External Divide input when DIV SEL is low, internal ÷ N output when DIV SEL is high.
14	V_{SS} (D)	Ground for digital, I/O circuits.
15	CLK Out	Buffered output of the VCO.

VCO Divisors Table 1

Prog A Pin 16	Prog B Pin 1	Prog C Pin 2	Div Value N
0	0	0	851
0	0	1	864
0	1	0	944
0	1	1	1135
1	0	0	682
1	0	1	858
1	1	0	780
1	1	1	910

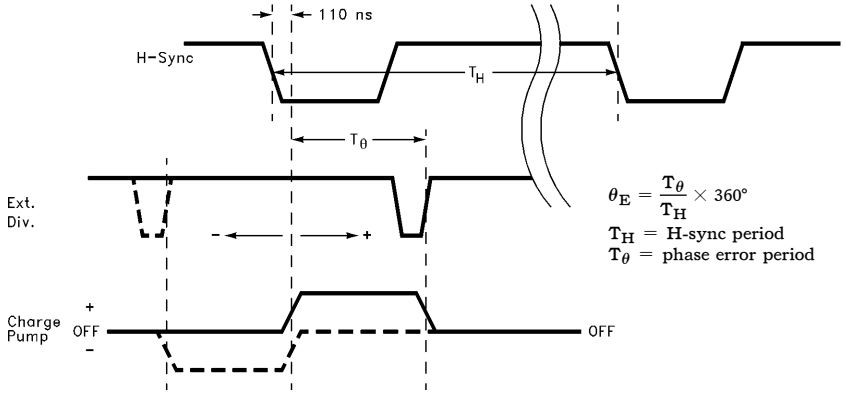
Timing Diagrams

PLL Locked Condition (Phase Error = 0)

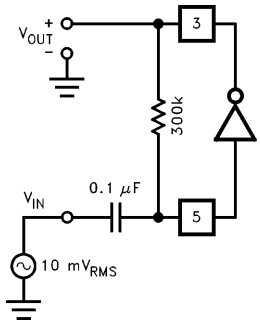


Falling edge of H-sync + 110 ns locks to rising edge of Ext Div signal.

Out of Lock Condition

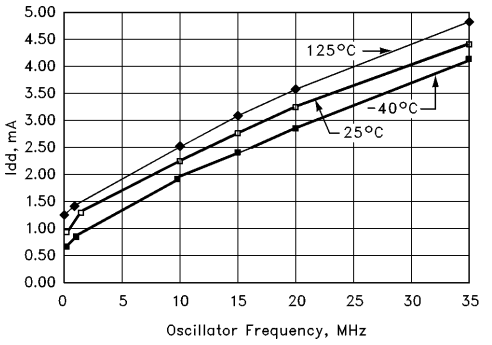


Test Circuit 1



Typical Performance Curves

Idd vs Fosc



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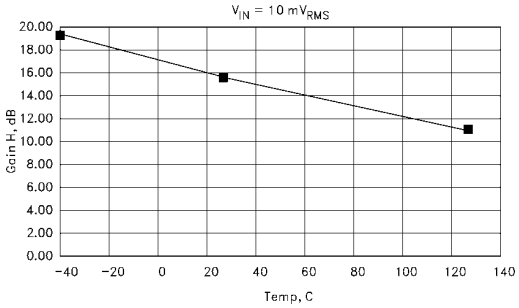
4584 OSC Gain @ 20 MHz vs Temp



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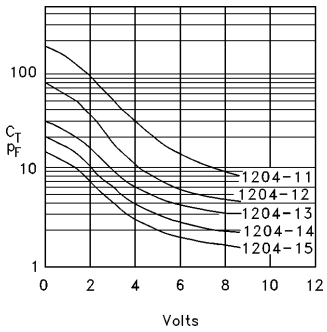
Typical Varactor



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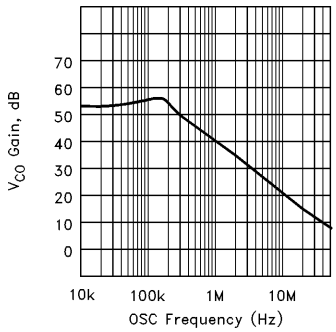
OSC Gain vs Fosc



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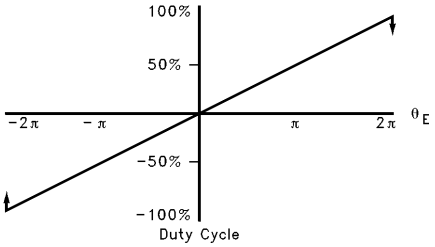
Charge Pump Duty Cycle vs θ_E



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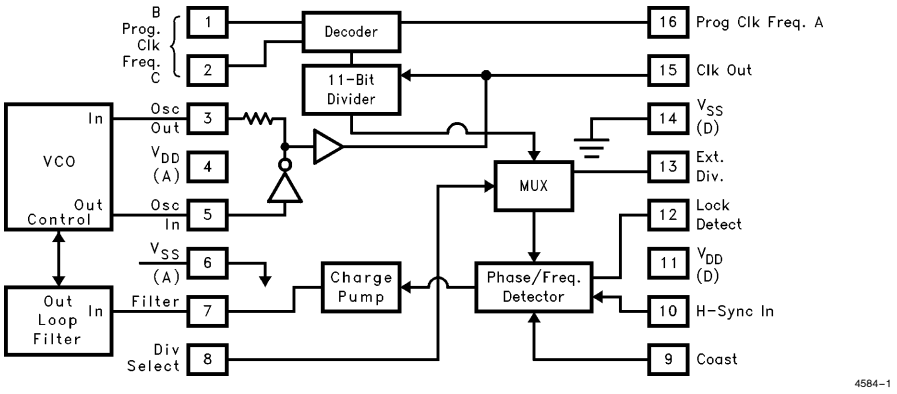
Block Diagram



Description Of Operation

The horizontal sync signal (CMOS level, falling leading edge) is input to H-sync input (pin 10). This signal is delayed about 110 ns, the falling edge of which becomes the reference to which the clock output will be locked. (See timing diagrams.) The clock is generated by the signal on pin 5, OSC in. There are 2 general types of VCO that can be used with the EL4584C, LC and crystal controlled. Additionally, each type can be either built up using discrete components, including a varactor as the frequency controlling element, or complete, self contained modules can be purchased with everything inside a metal can. The modules are very forgiving of PCB layout, but cost more than discrete solutions. The VCO or VCXO is used to generate the clock. An LC tank resonator has greater "pull" than a crystal controlled circuit, but will also be more likely to drift over time, and thus will generate more jitter. The "pullability" of the circuit refers to the ability to "pull" the frequency of oscillation away from its center frequency by modulating the voltage on the control pin of a VCO module or varactor, and is a function of the slope and range of the capacitance-voltage curve of the varactor or VCO module used. The VCO signal is sent to a divide by N counter, and to the CLK out pin. The divisor N is determined by the state of pins 1,2, and 16 and is described in table 1 above. The divided signal is sent, along with the delayed H-sync input, to the phase/frequency detector, which compares the two signals for phase and frequency differences. Any phase difference is converted to a current at the charge pump output FILTER (pin 7). A VCO with positive frequency deviation with control voltage must be used. Varactors have negative capacitance slope with voltage, resulting in positive frequency deviation with control voltage for the oscillators in figures 10 and 11 below.

VCO

The VCO should be tuned so its frequency of oscillation is very close to the required clock output frequency when the voltage on the varactor is 2.5 volts. VCXO and VCO modules are already tuned to the desired frequency, so this step is not necessary if using one of these units. The range of the charge pump output (pin 7) is 0 to 5 volts and it can source or sink a maximum of about 300 μA, so all frequency control must be accomplished with variable capacitance from the varactor within this range. Crystal oscillators are more stable than LC oscillators, which translates into lower jitter, but LC oscillators can be pulled from their mid-point values further, resulting in a greater capture and locking range. If the incoming horizontal sync signal is known to be very stable, then a crystal oscillator circuit can be used. If the h-sync signal experiences frequency variations of greater than about 300 ppm, an LC oscillator should be considered, as crystal oscillators are very difficult to pull this far. When H-SYNC input frequency is greater than CLK frequency $\div$ N, charge pump output (pin 7) sources current into the filter capacitor, increasing the voltage across the varactor, which lowers its capacitance, thus tending to increase VCO frequency. Conversely, filter output pulls current from the filter capacitor when H-SYNC frequency is less than CLK $\div$ N, forcing the VCO frequency lower.

Loop Filter

The loop filter controls how fast the VCO will respond to a change in filter output stimulus. Its components should be chosen so that fast lock can be achieved, yet with a minimum of VCO "hunting", preferably in one to two oscillations of charge pump output, assuming the VCO frequency starts within capture range. If the filter is under-damped, the VCO will over and undershoot the desired operating point many times before a stable lock takes place. It is possible to under-damp the filter so much that the loop itself oscillates, and VCO lock is never achieved. If the filter is over-damped, the VCO response time will be excessive and many cycles will be required for a lock condition. Over-damping is also characterized by an easily unlocked system because the filter can't respond fast enough to perturbations in VCO frequency. A severely over damped system will seem to endlessly oscillate, like a very large mass at the end of a long pendulum. Due to parasitic effects of PCB traces and component variables, it will take some trial and error experimentation to determine the best values to use for any given situation. Use the component tables as a starting point, but be aware that deviation from these values is not out of the ordinary.

Description of Operation — Contd.

External Divide

DIV SEL (pin 8) controls the use of the internal divider. When high, the internal divider is enabled and EXT DIV (pin 13) outputs the CLK out divided by N. This is the signal to which the horizontal sync input will lock. When divide select is low, the internal divider output is disabled, and external divide becomes an input from an external divider, so that a divisor other than one of the 8 pre-programmed internal divisors can be used.

Normal Mode

Normal mode is enabled by pulling COAST (pin 9) low (below $\frac{1}{3}*V_{CC}$). If H-sync and CLK ÷ N have any phase or frequency difference, an error signal is generated and sent to the charge pump. The charge pump will either force current into or out of the filter capacitor in an attempt to modulate the VCO frequency. Modulation will continue until the phase and frequency of CLK ÷ N exactly match the H-sync input. When the phase and frequency match (with some offset in phase that is a function of the VCO characteristics), the error signal goes to zero, lock detect no longer pulses high, and the charge pump enters a high impedance state. The clock is now locked to the H-sync input. As long as phase and frequency differences remain small, the PLL can adjust the VCO to remain locked and lock detect remains low.

Fast Lock Mode

Fast Lock mode is enabled by either allowing coast to float, or pulling it to mid supply (between $\frac{1}{3}$ and $\frac{2}{3}*V_{CC}$). In this mode, lock is achieved much faster than in normal mode, but the clock divisor is modified on the fly to achieve this. If the phase detector detects an error of enough magnitude, the clock is either inhibited or reset to attempt a "fast" lock of the signals. Forcing the clock to be synchronized to the H-sync input this way allows a lock in approximately 2 H-cycles, but the clock spacing will not be regular during this time. Once the near lock condition is attained, charge pump output should be very close to its lock-on value and placing the device into normal mode should result in a normal lock very quickly. Fast Lock mode is intended to be used where H-sync becomes irregular, until a stable signal is again obtained.

Coast Mode

Coast mode is enabled by pulling COAST (pin 9) high (above $\frac{2}{3}*V_{CC}$). In coast mode the internal phase detector is disabled and filter out remains in high impedance mode to keep filter out voltage and VCO frequency as constant a possible. VCO frequency will drift as charge leaks from the filter capacitor, and the voltage changes the VCO operating point. Coast mode is intended to be used when noise or signal degradation result in loss of horizontal sync for many cycles. The phase detector will not attempt to adjust to the resultant loss of signal so that when horizontal sync returns, sync lock can be re-established quickly. However, if much VCO drift has occurred, it may take as long to re-lock as when restarting.

Lock Detect

Lock detect (pin 12) will go low when lock is established. Any DC current path from charge pump out will skew EXT DIV relative to H-SYNC in, tending to offset or add to the 110 ns internal delay, depending on which way the extra current is flowing. This offset is called static phase error, and is always present in any PLL system. If, when the part stabilizes in a locked mode, lock detect is not low, adding or subtracting from the loop filter series resistor R_2 will change this static phase error to allow LDET to go low while in lock. The goal is to put the rising edge of EXT DIV in sync with the falling edge of H-SYNC + 110 ns. (See timing diagrams.) Increasing R_2 decreases phase error, while decreasing R_2 increases phase error. (Phase error is positive when EXT DIV lags H-SYNC.) The resistance needed will depend on VCO design or VCXO module selection.

Applications Information

Choosing External Components

1. To choose LC VCO components, first pick the desired operating frequency. For our example we will use 14.31818 MHz, with an H-sync frequency of 15.734 kHz.
2. Choose a reasonable inductor value (10–20μH works well). We choose 15 μH.
3. Calculate C_T needed to produce F_{OSC}.

$$F_{OSC} = \frac{1}{2\pi\sqrt{LC_T}}$$

$$C_T = \frac{1}{4\pi^2F^2L} = \frac{1}{4\pi^2(14.318e6)^2(15e-6)} = 8.2\ pF$$

4. From the varactor data sheet find C_V @ 2.5V, the desired lock voltage. $C_V = 23$ pF for our SMV1204-12, for example.
5. C_2 should be about $10C_V$, so we choose $C_2 = 220$ pF for our example.
6. Calculate C_1. Since

$$C_T = \frac{C_1C_2C_V}{(C_1C_2) + (C_1C_V) + (C_2C_V)},$$

then

$$C_1 = \frac{C_2C_TC_V}{(C_2C_V) - (C_2C_T) - (C_TC_V)}.$$

For our example, $C_1 = 14$ pF. (A trim cap may be used for fine tuning.) Examples for each frequency using the internal divider follow.

Typical Application

Horizontal genlock provides clock for an analog to digital converter, digitizing analog video.

Typical LC VCO

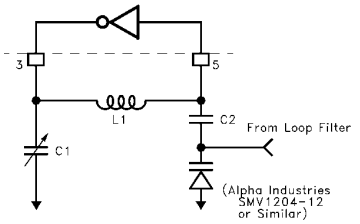


Figure 10

LC VCO Component Values (Approximate)

Frequency (MHz)	L1 (μH)	C1 (pF)	C2 (pF)
13.301	15	18	220
13.5	15	17	220
14.75	12	18	220
17.734	12	10	220
10.738	22	20	220
12.273	18	17	220
14.318	15	14	220

Note: Use shielded inductors for optimum performance.

Typical Xtal VCO

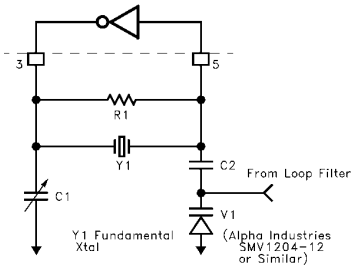
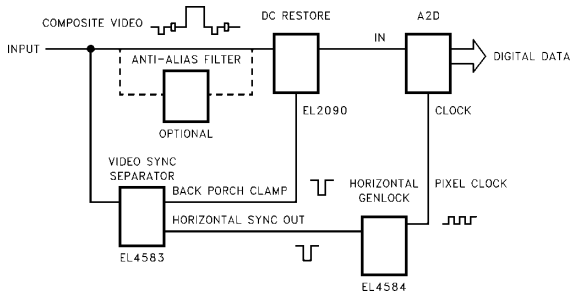


Figure 11

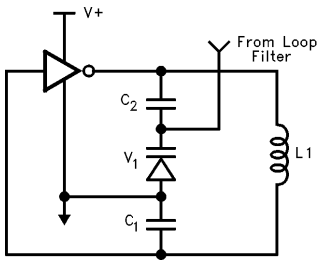


Xtal VCO Component Values (Approximate)

Frequency (MHz)	R1 (kΩ)	C1 (pF)	C2 (uF)
13.301	300	15	.001
13.5	300	15	.001
14.75	300	15	.001
17.734	300	15	.001
10.738	300	15	.001
12.273	300	15	.001
14.318	300	15	.001

The above oscillators are arranged as Colpitts oscillators, and the structure is redrawn here to emphasize the split capacitance used in a Colpitts oscillator. It should be noted that this oscillator configuration is just one of literally hundreds possible, and the configuration shown here does not necessarily represent the best solution for all applications. Crystal manufacturers are very informative sources on the design and use of oscillators in a wide variety of applications, and the reader is encouraged to become familiar with them.

Colpitts Oscillator



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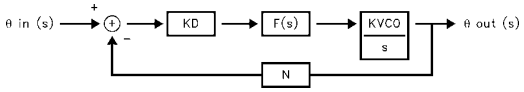
C_1 is to adjust the center frequency, C_2 DC isolates the control from the oscillator, and V1 is the primary control device. C_2 should be much larger than C_V so that V_1 has maximum modulation capability. The frequency of oscillation is given by:

$$F = \frac{1}{2\pi\sqrt{LC_T}}$$

$$C_T = \frac{C_1C_2C_V}{(C_1C_2) + (C_1C_V) + (C_2C_V)}$$

Choosing Loop Filter Components

The PLL, VCO, and loop filter can be described as:



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Where:

K_d = phase detector gain in A/rad

F(s) = loop filter impedance in V/A

K_{VCO} = VCO gain in rad/s/V

N = internal or external divisor

It can be shown that for the loop filter shown below:

$$C_3 = \frac{K_dK_{VCO}}{N\omega_n^2},\ C_4 = \frac{C_3}{10},\ R_3 = \frac{2N\zeta\omega_n}{K_dK_{VCO}}$$

Where ω_n = loop filter bandwidth, and ζ = loop filter damping factor.

1. K_d = 300 μA/2πrad = 4.77e-5A/rad for the EL4584C.

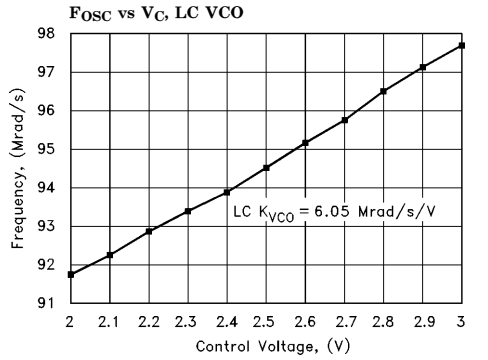
2. The loop bandwidth should be about H-sync frequency/20, and the damping ratio should be 1 for optimum performance. For our example, ω_n = 15.734 kHz/20 = 787 Hz $\approx$ 5000 rad/S.

3. N = 910 from table 1.

$$N = \frac{\text{VCOfrequency}}{\text{H-SYNCfrequency}} = \frac{14.31818M}{15.73426k} = 910$$

4. K_{VCO} represents how much the VCO frequency changes for each volt applied at the control pin. It is assumed (but probably isn't) linear about the lock point (2.5V). Its value depends on the VCO configuration and the varactor

transfer function $C_v = F(V_C)$, where V_C is the reverse bias control voltage, and C_V is varactor capacitance. Since $F(V_C)$ is nonlinear, it is probably best to build the VCO and measure K_{VCO} about 2.5V. The results of one such measurement are shown below. The slope of the curve is determined by linear regression techniques and equals K_{VCO}. For our example, K_{VCO} = 6.05 Mrad/S/V.



5. Now we can solve for C_3, C_4, and R_3.

$$C_3 = \frac{K_d K_{VCO}}{N\omega^2_n} = \frac{(4.77e-5)(6.05e6)}{(910)(5000)^2} = 0.01\ \mu F$$

$$C_4 = \frac{C_3}{10} = 0.001\ \mu F$$

$$R_3 = \frac{2N\zeta\omega_n}{K_d K_{VCO}} = \frac{(2)(910)(1)(5000)}{(4.77e-5)(6.05e6)} = 31.5\ k\Omega$$

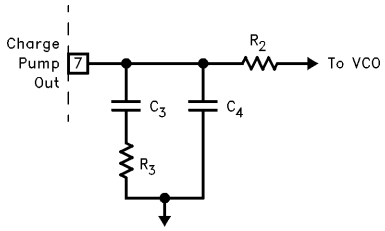
We choose R_3 = 30 kΩ for convenience.

6. Notice R_2 has little effect on the loop filter design. R_2 should be large, around 100k, and can be adjusted to compensate for any static phase error T_θ at lock, but if made too large, will slow loop response. If R_2 is made smaller, T_θ (see timing diagrams) increases, and if R_2 increases, T_θ decreases. For LDET to be low at lock, $|T_\theta| < 50$ ns. C_4 is used mainly to attenuate high frequency noise from the charge pump.

Lock Time

Let $T = R_3C_3$. As T increases, damping increases, but so does lock time. Decreasing T decreases damping and speeds up loop response, but increases overshoot and thus increases the number of hunting oscillations before lock. Critical damping ($\zeta = 1$) occurs at minimum lock time. Because decreased damping also decreases loop stability, it is sometimes desirable to design slightly overdamped ($\zeta > 1$), trading lock time for increased stability.

Typical Loop Filter



LC Loop Filter Components (Approximate)

Frequency (MHz)	R2 (kΩ)	R3 (kΩ)	C3 (μF)	C4 (μF)
13.301	100	30	0.01	0.001
13.5	100	30	0.01	0.001
14.75	100	33	0.01	0.001
17.734	100	39	0.01	0.001
10.738	100	22	0.01	0.001
12.273	100	27	0.01	0.001
14.318	100	30	0.01	0.001

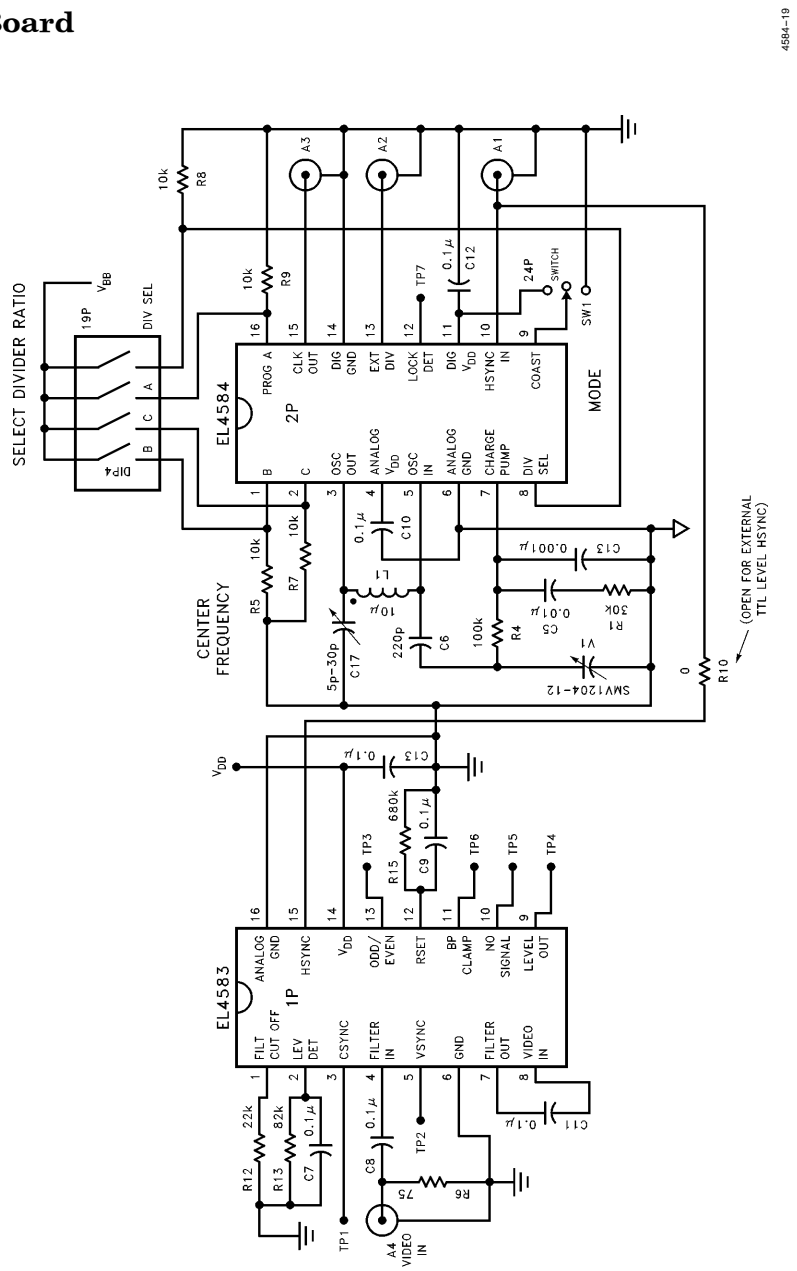
Xtal Loop Filter Components (Approximate)

Frequency (MHz)	R2 (kΩ)	R3 (MΩ)	C3 (pF)	C4 (pF)
13.301	100	4.3	68	6.8
13.5	100	4.3	68	6.8
14.75	100	4.3	68	6.8
17.734	100	4.3	68	6.8
10.738	100	4.3	68	6.8
12.273	100	4.3	68	6.8
14.318	100	4.3	68	6.8

PCB Layout Considerations

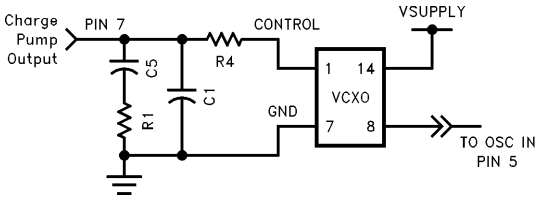
It is highly recommended that power and ground planes be used in layout. The oscillator and filter sections constitute a feedback loop and thus care must be taken to avoid any feedback signal influencing the oscillator except at the control input. The entire oscillator/filter section should be surrounded by copper ground to prevent unwanted influences from nearby signals. Use separate paths for analog and digital supplies, keeping the analog (oscillator section) as short and free from spurious signals as possible. Careful attention must be paid to correct bypassing. Keep lead lengths short and place bypass caps as close to the supply pins as possible. If laying out a PCB to use discrete components for the VCO section, care must be taken to avoid parasitic capacitance at the OSC pins 3 and 5, and FILTER out (pin 7). Remove ground and power plane copper above and below these traces to avoid making a capacitive connection to them. It is also recommended to enclose the oscillator section within a shielded cage to reduce external influences on the VCO, as they tend to be very sensitive to "hand-waving" influences, the LC variety being more sensitive than crystal controlled oscillators. In general, the higher the operating frequency, the more important these considerations are. Self contained VCXO or VCO modules are already mounted in a shielding cage and therefore do not require as much consideration in layout. Many crystal manufacturers publish informative literature regarding use and layout of oscillators which should be helpful.

Demo Board

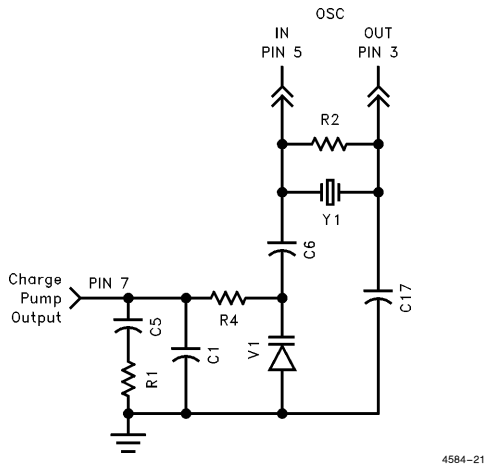

4584-19
SELECT DIVIDER RATIO
DIP4
19P
DIV SEL
A
C
B
V_{BB}
EL4584
2P
PROG A
CLK OUT
DIG GND
EXT DIV
LOCK DET
DIG V_{DD}
HSYNC IN
COAST
MODE
OSC OUT
ANALOG V_{DD}
OSC IN
ANALOG GND
CHARGE PUMP
DIV SEL
CENTER FREQUENCY
5p-30p
C17
10µ
L1
220p
C6
100k
R4
0.1µ
C5
30k
R1
0.001µ
C13
SW1204-12
V1
0
R10
(OPEN FOR EXTERNAL TTL LEVEL HSYNC)
10k
R8
10k
R9
0.1µ
C12
TP7
24P
SWITCH
SW1
A3
A2
A1
10k
R7
10k
R5
0.1µ
C10
V_{DD}
0.1µ
C13
680k
R15
0.1µ
C9
TP3
TP6
TP5
TP4
EL4583
1P
ANALOG GND
HSYNC
V_{DD}
ODD/ EVEN
RSET
BP CLAMP
NO SIGNAL
LEVEL OUT
FILT CUT OFF
LEV DET
CSYNC
FILTER IN
VSYNC
GND
FILTER OUT
VIDEO IN
22k
R12
82k
R13
0.1µ
C7
0.1µ
C8
TP2
75
R6
0.1µ
C11
TP1
A4
VIDEO IN

The VCO and loop filter section of the EL4583/4/5 demo board can be implemented in the following configurations:

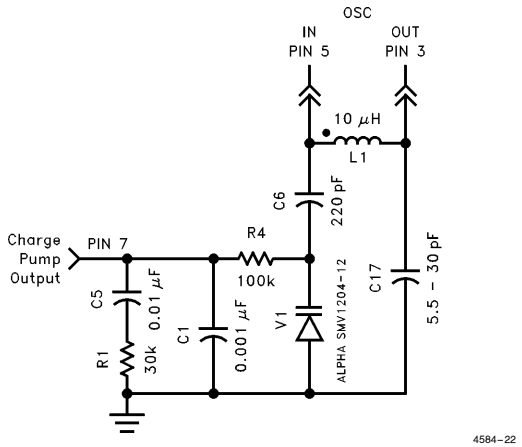
(1) VCXO



(2) XTAL



(3) LC Tank



BLANK

EL4584C
Horizontal Genlock, 4 F_{SC}

Component Sources

Inductors

- Dale Electronics
  E. Highway 50
  PO Box 180
  Yankton, SD 57078-0180
  (605) 665-9301

Crystals, VCXO, VCO Modules

- Connor-Winfield
  2111 Comprehensive Drive
  Aurora, IL 60606
  (708) 851-4722

- Piezo Systems
  100 K Street
  PO Box 619
  Carlisle, PA 17013
  (717) 249-2151

- Reeves-Hoffman
  400 West North Street
  Carlisle, PA 17013
  (717) 243-5929

- SaRonix
  151 Laura Lane
  Palo Alto, CA 94043
  (415) 856-6900

- Standard Crystal
  9940 Baldwin Place
  El Monte, CA 91731
  (818) 443-2121

Varactors

- Alpha Industries
  20 Sylvan Road
  Woburn, MA 01801
  (617) 935-5150

- Motorola Semiconductor Products
  2100 E. Elliot
  Tempe, AZ 85284
  (602) 244-6900

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