

## Dual Channel, High Speed, High Current Line Driver with 3-State

The EL7232 3-state drivers are particularly well suited for ATE and microprocessor based applications. The low quiescent power dissipation makes this part attractive in battery applications. The 2A peak drive capability, makes the EL7232 an excellent choice when driving high speed capacitive lines, as well. The input circuitry provides level shifting from TTL levels to the supply rails. The EL7232 is available in 8-pin PDIP and 8-lead SO packages.

### Ordering Information

PART NUMBER	PART MARKING	PACKAGE	TAPE & REEL	PKG. DWG. #
EL7232CN	EL7232CN	8 Ld PDIP	-	MDP0031
EL7232CNZ	EL7232CN Z	8 Ld PDIP*	-	MDP0031
EL7232CS	7232CS	8 Ld SOIC	-	MDP0027
EL7232CS-T7	7232CS	8 Ld SOIC	7"	MDP0027
EL7232CSZ (See Note)	7232CSZ	8 Ld SOIC (Pb-free)	-	MDP0027
EL7232CSZ-T7 (See Note)	7232CSZ	8 Ld SOIC (Pb-free)	7"	MDP0027
EL7232CSZ-T13 (See Note)	7232CSZ	8 Ld SOIC (Pb-free)	13"	MDP0027

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

\*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

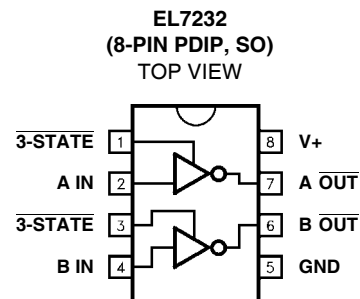
### Features

- 3-State output
- 3V and 5V input compatible
- Clocking speeds up to 10MHz
- 20ns Switching/delay time
- 2A Peak drive
- Low, matched output impedance 5Ω
- Low quiescent current 2.5mA
- Wide operating voltage 4.5V-16V
- Pb-Free available (RoHS compliant)

### Applications

- Parallel bus line drivers
- EPROM and PROM programming
- Motor controls
- Charge pumps
- Sampling circuits
- Pin drivers
- Bridge circuits

### Pinout



Manufactured under U.S. Patent Nos. 5,334,883, #5,341,047

### Truth Table

3-STATE	INPUT	OUTPUT
1	0	1
1	1	0
0	0	Open
0	1	Open

**Absolute Maximum Ratings** ( $T_A = 25^\circ\text{C}$ )

Supply (V+ to Gnd) ..... 16.5V  
 Input Pins ..... -0.3V to +0.3V above V+  
 Combined Peak Output Current ..... .4A  
 Storage Temperature Range ..... -65°C to +150°C  
 Ambient Operating Temperature ..... -40°C to +85°C

Operating Junction Temperature ..... 125°C  
 Power Dissipation  
 SOIC ..... .570mW  
 PDIP ..... .1050mW

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

*IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore:  $T_J = T_C = T_A$*

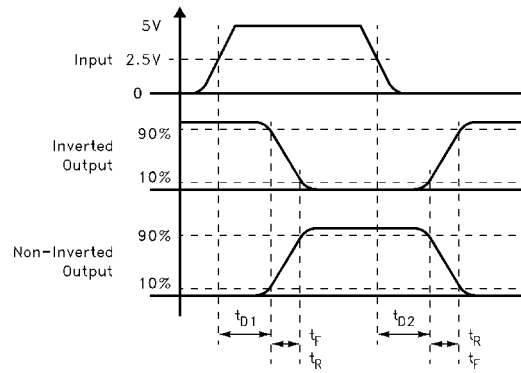
**DC Electrical Specifications**  $T_A = 25^\circ\text{C}$ , V = 15V unless otherwise specified

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>INPUT</b>						
V <sub>IH</sub>	Logic "1" Input Voltage		2.4			V
I <sub>IH</sub>	Logic "1" Input Current	@V+		0.1	10	μA
V <sub>IL</sub>	Logic "0" Input Voltage				0.8	V
I <sub>IL</sub>	Logic "0" Input Current	@0V		0.1	10	μA
V <sub>HVS</sub>	Input Hysteresis			0.3		V
<b>OUTPUT</b>						
R <sub>OH</sub>	Pull-Up Resistance	I <sub>OUT</sub> = -100 mA		3	6	Ω
R <sub>OL</sub>	Pull-Down Resistance	I <sub>OUT</sub> = +100 mA		4	6	Ω
I <sub>OFF</sub>	3-State Output Leakage	V <sub>OUT</sub> = V+ V <sub>OUT</sub> = 0V	0.2		10	μA
I <sub>PK</sub>	Peak Output Current	Source Sink		2.0 2.0		A
I <sub>DC</sub>	Continuous Output Current	Source/Sink	100			mA
<b>POWER SUPPLY</b>						
I <sub>S</sub>	Power Supply Current	Inputs High		1	2.5	mA
V <sub>S</sub>	Operating Voltage		4.5		16	V

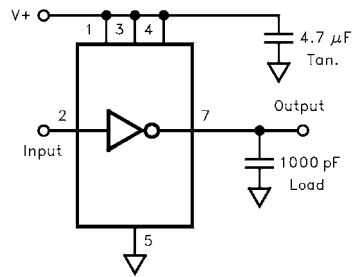
**AC Electrical Specifications**  $T_A = 25^\circ\text{C}$ , V = 15V unless otherwise specified

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>SWITCHING CHARACTERISTICS</b>						
t <sub>R</sub>	Rise Time	C <sub>L</sub> = 500pF C <sub>L</sub> = 1000pF		7.5 10		ns
t <sub>F</sub>	Fall Time	C <sub>L</sub> = 500pF C <sub>L</sub> = 1000pF		10 13	20	ns
t <sub>D-ON</sub>	Turn-On Delay Time			18	25	ns
t <sub>D-OFF</sub>	Turn-Off Delay Time			20	25	ns

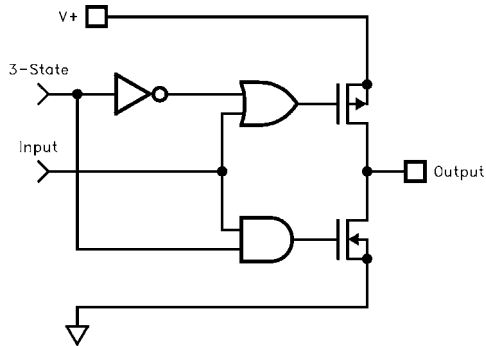
**Timing Table**



**Standard Test Configuration**

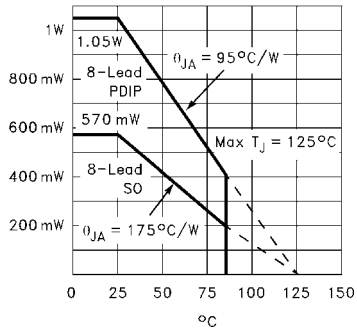


**Simplified Schematic**

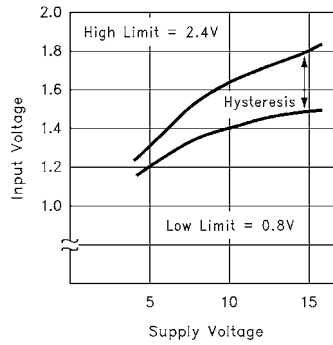


Typical Performance Curves

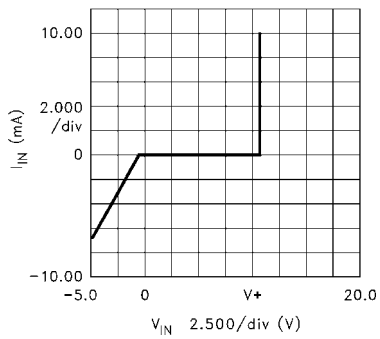
MAX POWER/DERATING CURVES



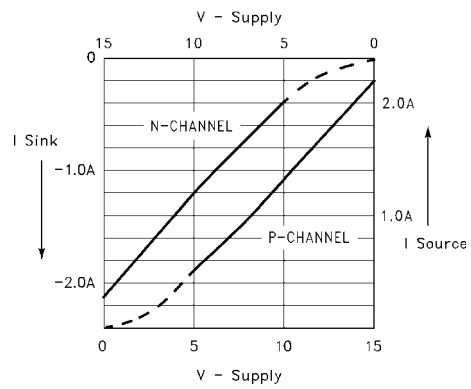
SWITCH THRESHOLD vs SUPPLY VOLTAGE



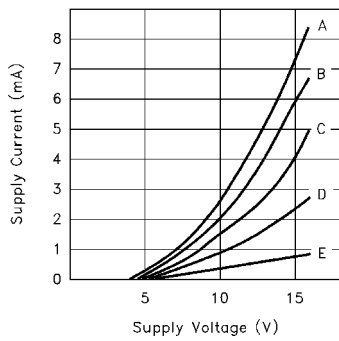
INPUT CURRENT vs VOLTAGE



PEAK DRIVE vs SUPPLY VOLTAGE



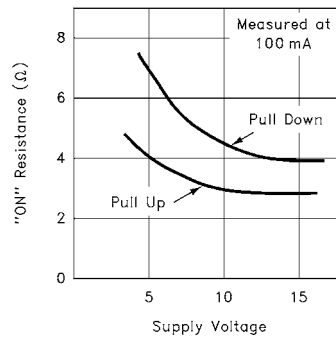
QUIESCENT SUPPLY CURRENT



CASE:

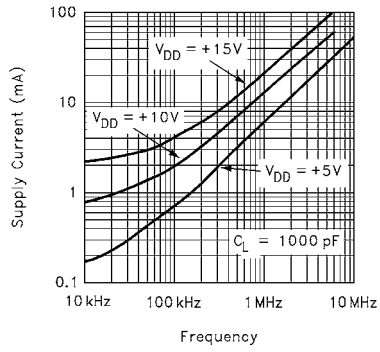
A	ALL INPUTS GND
B	3 INPUTS GND
C	2 INPUTS GND
D	1 INPUTS GND
E	ALL INPUTS V+

"ON" RESISTANCE vs SUPPLY VOLTAGE

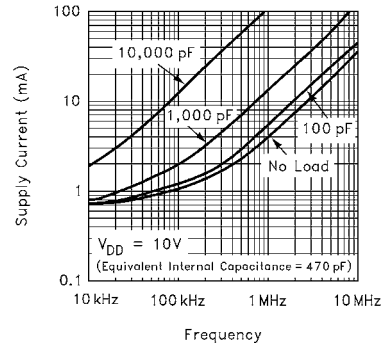


Typical Performance Curves (Continued)

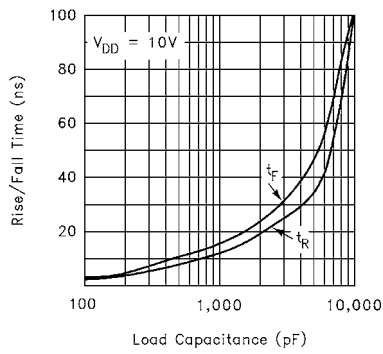
AVERAGE SUPPLY CURRENT vs VOLTAGE AND FREQUENCY



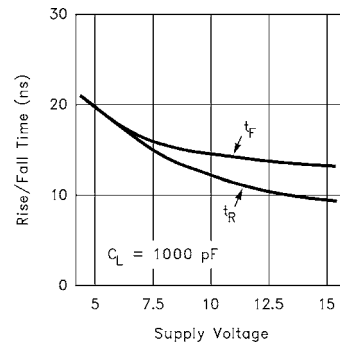
AVERAGE SUPPLY CURRENT vs CAPACITIVE LOAD



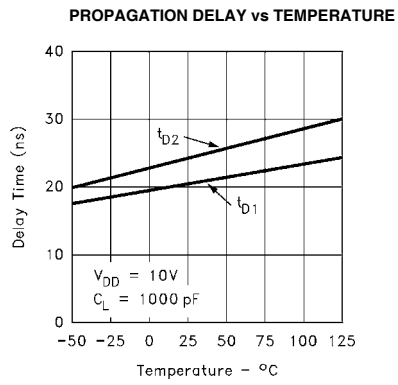
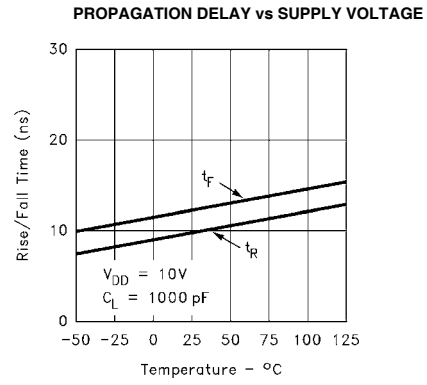
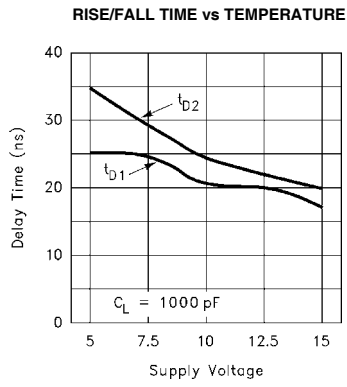
RISE/FALL TIME vs LOAD



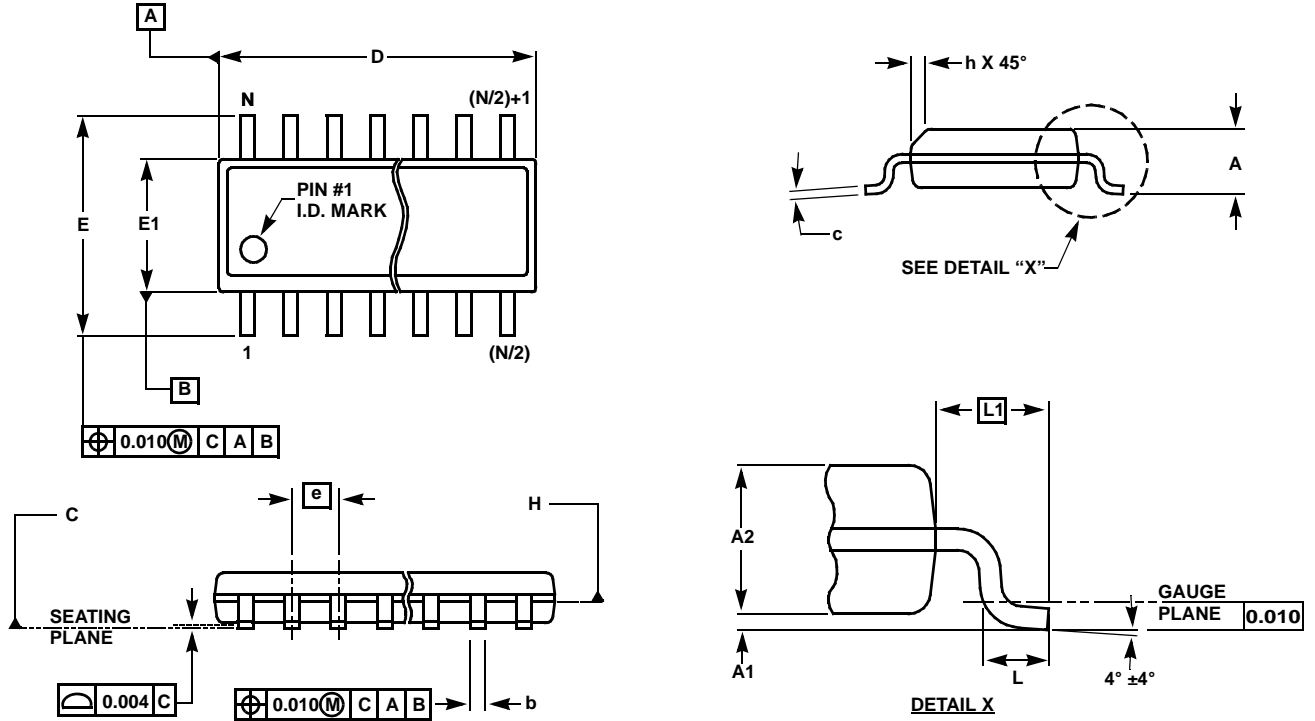
RISE/FALL TIME vs SUPPLY VOLTAGE



Typical Performance Curves (Continued)



**Small Outline Package Family (SO)**



**MDP0027**

**SMALL OUTLINE PACKAGE FAMILY (SO)**

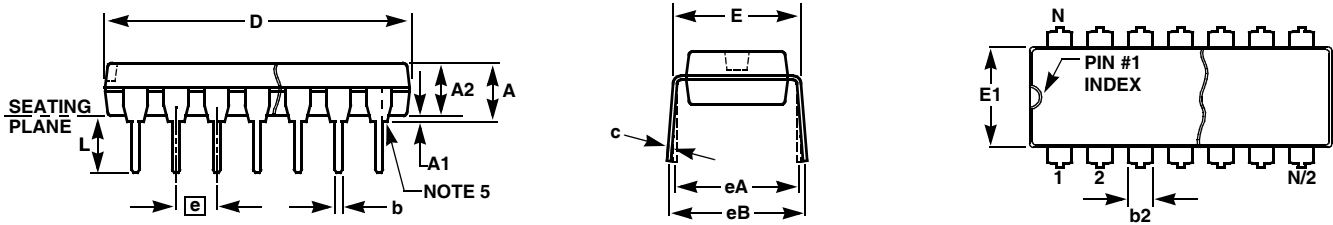
SYMBOL	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)	TOLERANCE	NOTES
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	$\pm 0.003$	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	$\pm 0.002$	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	$\pm 0.003$	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	$\pm 0.001$	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	$\pm 0.004$	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	$\pm 0.008$	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	$\pm 0.004$	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	$\pm 0.009$	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

Rev. L 2/01

**NOTES:**

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

**Plastic Dual-In-Line Packages (PDIP)**



**MDP0031**

**PLASTIC DUAL-IN-LINE PACKAGE**

SYMBOL	PDIP8	PDIP14	PDIP16	PDIP18	PDIP20	TOLERANCE	NOTES
A	0.210	0.210	0.210	0.210	0.210	MAX	
A1	0.015	0.015	0.015	0.015	0.015	MIN	
A2	0.130	0.130	0.130	0.130	0.130	±0.005	
b	0.018	0.018	0.018	0.018	0.018	±0.002	
b2	0.060	0.060	0.060	0.060	0.060	+0.010/-0.015	
c	0.010	0.010	0.010	0.010	0.010	+0.004/-0.002	
D	0.375	0.750	0.750	0.890	1.020	±0.010	1
E	0.310	0.310	0.310	0.310	0.310	+0.015/-0.010	
E1	0.250	0.250	0.250	0.250	0.250	±0.005	2
e	0.100	0.100	0.100	0.100	0.100	Basic	
eA	0.300	0.300	0.300	0.300	0.300	Basic	
eB	0.345	0.345	0.345	0.345	0.345	±0.025	
L	0.125	0.125	0.125	0.125	0.125	±0.010	
N	8	14	16	18	20	Reference	

Rev. B 2/99

**NOTES:**

1. Plastic or metal protrusions of 0.010" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions E and eA are measured with the leads constrained perpendicular to the seating plane.
4. Dimension eB is measured with the lead tips unconstrained.
5. 8 and 16 lead packages have half end-leads as shown.

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