

## GENERAL DESCRIPTION

EM19100 is an 8-bit CMOS A/D converter for video use. The adoption of a 2-step parallel system achieves low consumption at a maximum conversion speed of 20 MSPS typical.

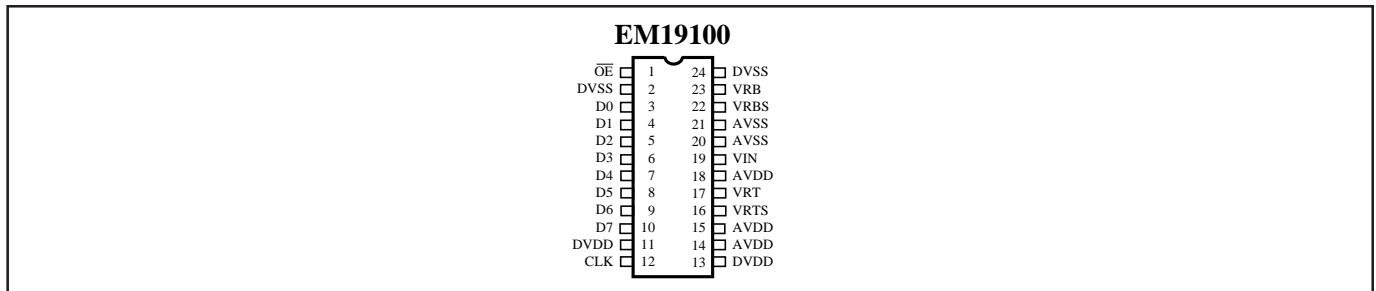
## FEATURES

- 20MSPS maximum conversion speed
- Build-in sampling and hold circuit
- Internal self-bias reference voltage
- 90mW power dissipation at 20MSPS
- +5V single power supply
- Available in 24 pin SOP
- Series
  - EM19100M for 300 mil SOP
  - EM19100S for 209 mil SOP

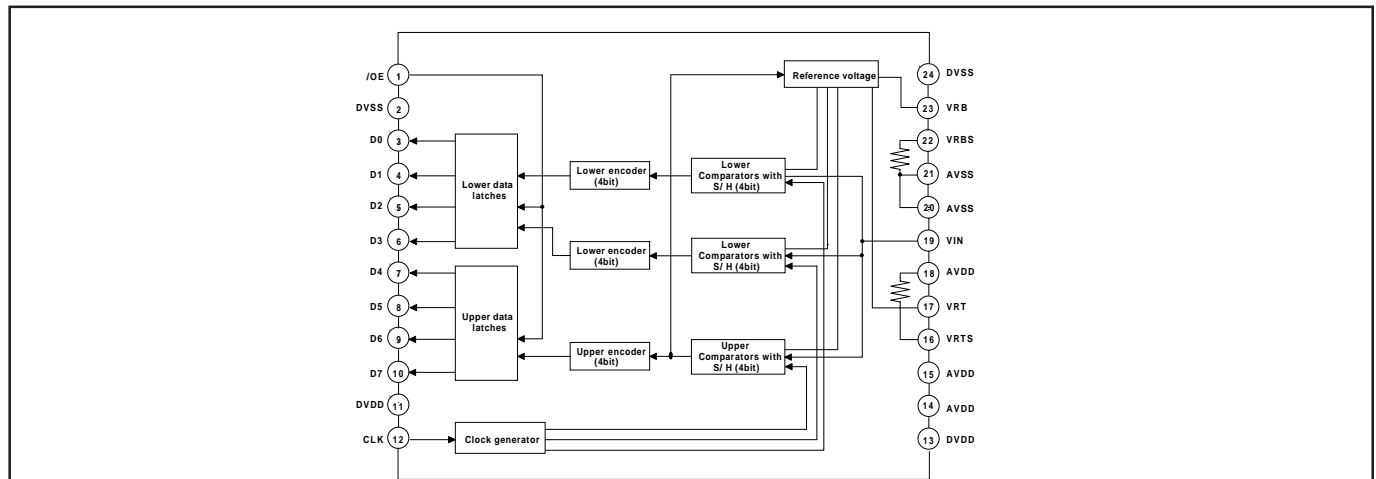
## APPLICATION

TV,VCR digital systems and a wide range of fields where high speed A/D conversion is required.

## PIN ASSIGNMENT

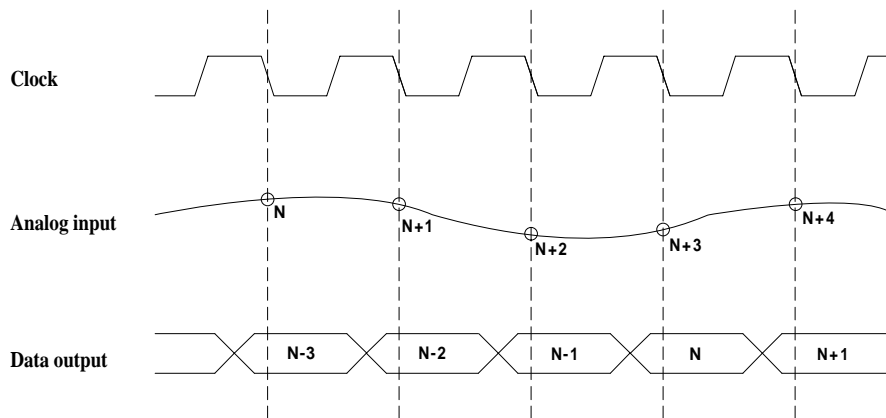


## FUNCTIONAL BLOCK DIAGRAM



### OUTPUT CODING

Step	Analog Input (V)	Digital Output Code	Conditions
0	0.607815	00000000	VRB=0.6V
1	0.607815~0.6156250	00000001	VRT=2.6V
2	0.6156250~0.6234375	00000010	1LSB=7.8125mV
...	...	...	
124	1.6000000~1.6078125	10000000	
125	1.6078125~1.6156250	10000001	
...	...	...	
254	2.5843750~2.5921875	11111110	
255	2.5921875~	11111111	



### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub>=25°C)

Items	Sym.	Rating	Unit
Supply voltage	V <sub>DD</sub>	7	V
Operating temperature	T <sub>OPR</sub>	-20 to +65	°C
Input voltage	V <sub>IN</sub>	V <sub>SS</sub> to V <sub>DD</sub>	V
Ref, Input voltage	V <sub>RT</sub> , V <sub>RB</sub>	V <sub>SS</sub> to V <sub>DD</sub>	V

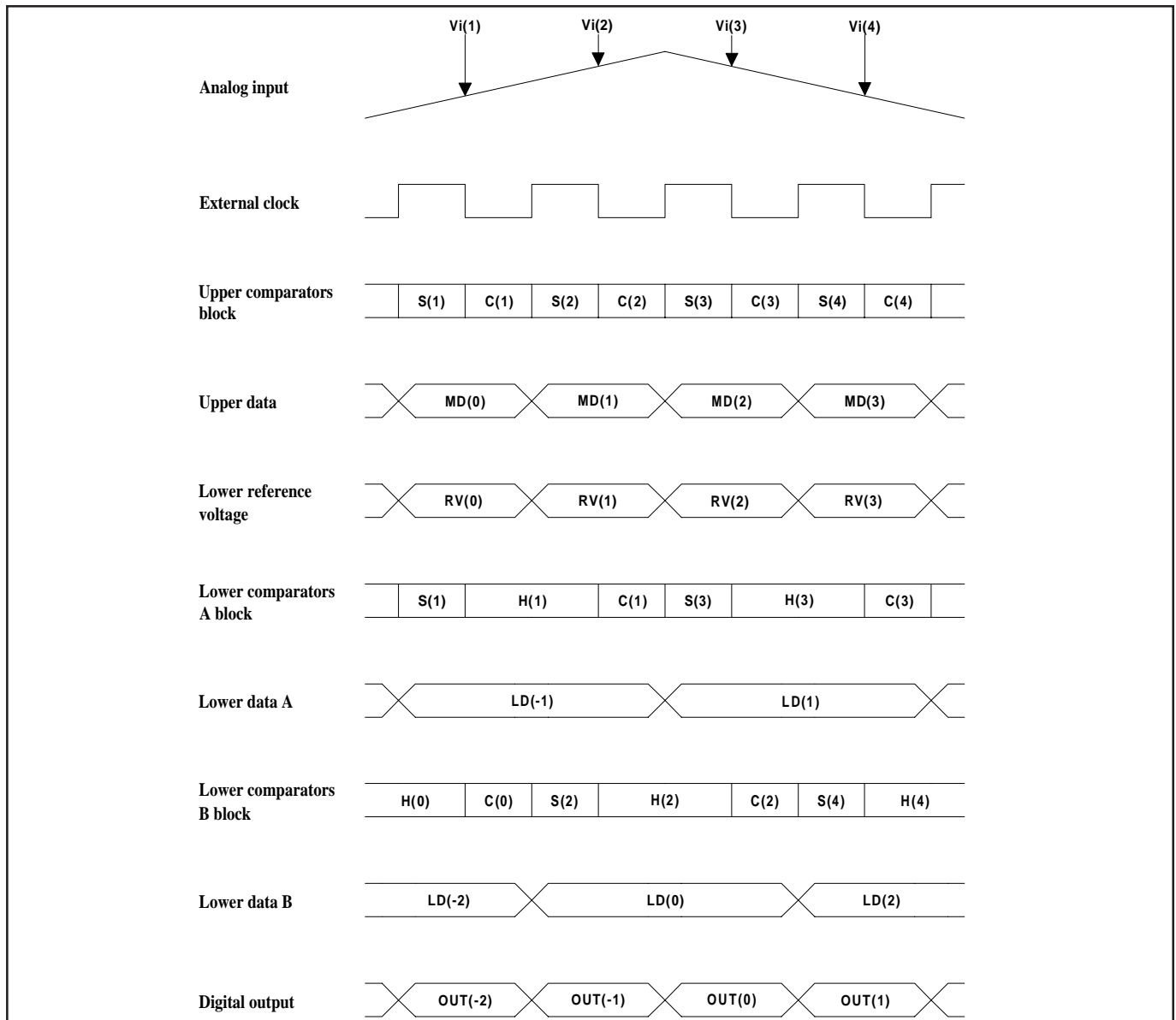
(F<sub>C</sub>=20MPS, V<sub>DD</sub>=5V, V<sub>RB</sub>=0.5V, V<sub>RT</sub>=2.5V, T<sub>a</sub>=25 deg.)

Parameter	Sym.	Conditions	Min.	Typ.	Max.	Unit
Maximum Conversion Speed	F <sub>C</sub>	V <sub>in</sub> =0.6V to 2.6V f <sub>in</sub> =1kHz ramp		20		MSPS
Supply current	I <sub>DD</sub>	F <sub>C</sub> =20MSPS NTSC ramp wave input		12	17	mA
Reference pin current	I <sub>REF</sub>		5.7	8.0	9.1	mA
Analog input bandwidth	BW			10		MHz
Analog input capacitance	C <sub>IN</sub>	V <sub>IN</sub> =1.5V+0.07Vrms		11		pF
Reference resistance	R <sub>REF</sub>		220	250	350	Ω
Internal bias	V <sub>RB</sub>	Short V <sub>RB</sub> and V <sub>RBS</sub>	0.55	0.6	0.65	V
	V <sub>RT</sub> -V <sub>RB</sub>	Short V <sub>RT</sub> and V <sub>RTS</sub>	1.9	2.0	2.1	
Offset Voltage	E <sub>OT</sub>		-10	-35	-60	mV
	E <sub>OB</sub>		0	15	45	
Digital input voltage	V <sub>IH</sub>		4.0			V
	V <sub>IL</sub>				1.0	
Digital input current	I <sub>IH</sub>	V <sub>DD</sub> =max. V <sub>IH</sub> =V <sub>DD</sub>			5	uA
	I <sub>IL</sub>	V <sub>IL</sub> =0V			5	

\* This specification are subject to be changed without notice.

Parameter	Sym.	Conditions	Min.	Typ.	Max.	Unit
Digital output current	$I_{OH}$	$OE=V_{SS}, V_{OH}=V_{DD}-0.5V$	-1.1			mA
	$I_{OL}$	$V_{DD}=\text{min.}, V_{OL}=0.4V$	3.7			
Digital output current	$I_{OZH}$	$OE=V_{DD}, V_{OH}=V_{DD}$			16	$\mu A$
		$V_{OL}=0V$			16	
Output data delay	$T_{DL}$			18	30	ns
Integral nonlinearity	EL	$F_C=20\text{MSPS}, V_{IN}=0.6V \text{ to } 2.6V$		0.5	1.3	LSB
Differential nonlinearity	ED	$F_C=20\text{MSPS}, V_{IN}=0.6V \text{ to } 2.6V$		$\pm 0.3$	$\pm 0.5$	LSB
Differential gain error	DG	NTSC 40 IRE mod ramp, $F_C=14.3\text{MSPS}$		1.0		%
Differential phase error	$D_P$			0.5		deg
Aperture jitter	$t_{AJ}$			30		ps
Sampling delay	$t_{DS}$			4		ns

### Timing



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## Timing explanation

EM19100 is a 2-step parallel system A/D converter featuring a 4-bit upper comparators group and 2 lower comparators groups of 4-bit each. The reference voltage that is equal to the voltage between  $V_{RT}-V_{RB}/16$  is constantly applied to the upper 4-bit comparator block. Voltage that corresponded to the upper data is fed through the reference supply to the lower data.  $V_{RTS}$  and  $V_{RBS}$  pins serve for the self generation of  $V_{RT}$  (Reference voltage top) and  $V_{RB}$  (Reference voltage bottom).

This IC uses an offset cancel type comparator and operates synchronously with an external clock. It features the following operating modes which are respectively indicated on the timing chart with S, H, C symbols. That is input sampling (auto zero) mode, input hold mode and comparison mode.

The operation of respective parts is as indicated in the chart. For instance input voltage  $V_i(1)$  is sampled with the falling edge of the first clock by means of the upper comparator block and the lower comparator A block. The upper comparators block finalizes comparison data MD(1) with the rising edge of the first clock. Simultaneously the reference supply generates the lower reference voltage RV(1) that corresponded to the upper results. The lower comparator block finalizes comparison data LD(1) with the rising edge of the second clock. MD(1) and LD(1) are combined and output as Out(1) with the rising edge the 3rd clock. Accordingly there is a 2.5 clock delay from the analog input sampling point to the digital data output.

## Application Note

$V_{DD}, V_{SS}$

To reduce noise effects, separate the analog and digital systems close to the device. For both the digital and analog  $V_{DD}$  pins, use a ceramic capacitor of about 0.1 $\mu$ F set as close as possible to the pin to bypass to the respective GND's.

### Analog input

Compared with the flash type A/D converter, the input capacitance of the analog input is rather small. However it is necessary to conduct the drive with an amplifier featuring sufficient band and drive capability. When driving with an amplifier of low output impedance, parasite oscillation may occur. That may be prevented by inserting a resistance of about 100 $\Omega$  in series between the amplifier output and A/D input.

### Clock input

The clock line wiring should be as short as possible also, to avoid any interference with other signals, separate it from other circuits

### Reference input

Voltage between  $V_{RT}$  to  $V_{RB}$  is compatible with the dynamic range of the analog input. Bypassing  $V_{RT}$  and  $V_{RB}$  pins to GND, by means of a capacitor about 0.1 $\mu$ F, stable characteristics are obtained. By shorting  $V_{RT}$  and  $V_{RTS}$ ,  $V_{RB}$  and  $VRBS$ , the self bias function that generates  $V_{RT}=2.6V$  and  $V_{RB}=0.6V$ , is activated.

### Timing

Analog input is sampled with the falling edge of CLK and output as digital data with a delay of 2.5 clocks and

with the following rising edge. The delay from the clock rising edge to the data output is about 18ns.

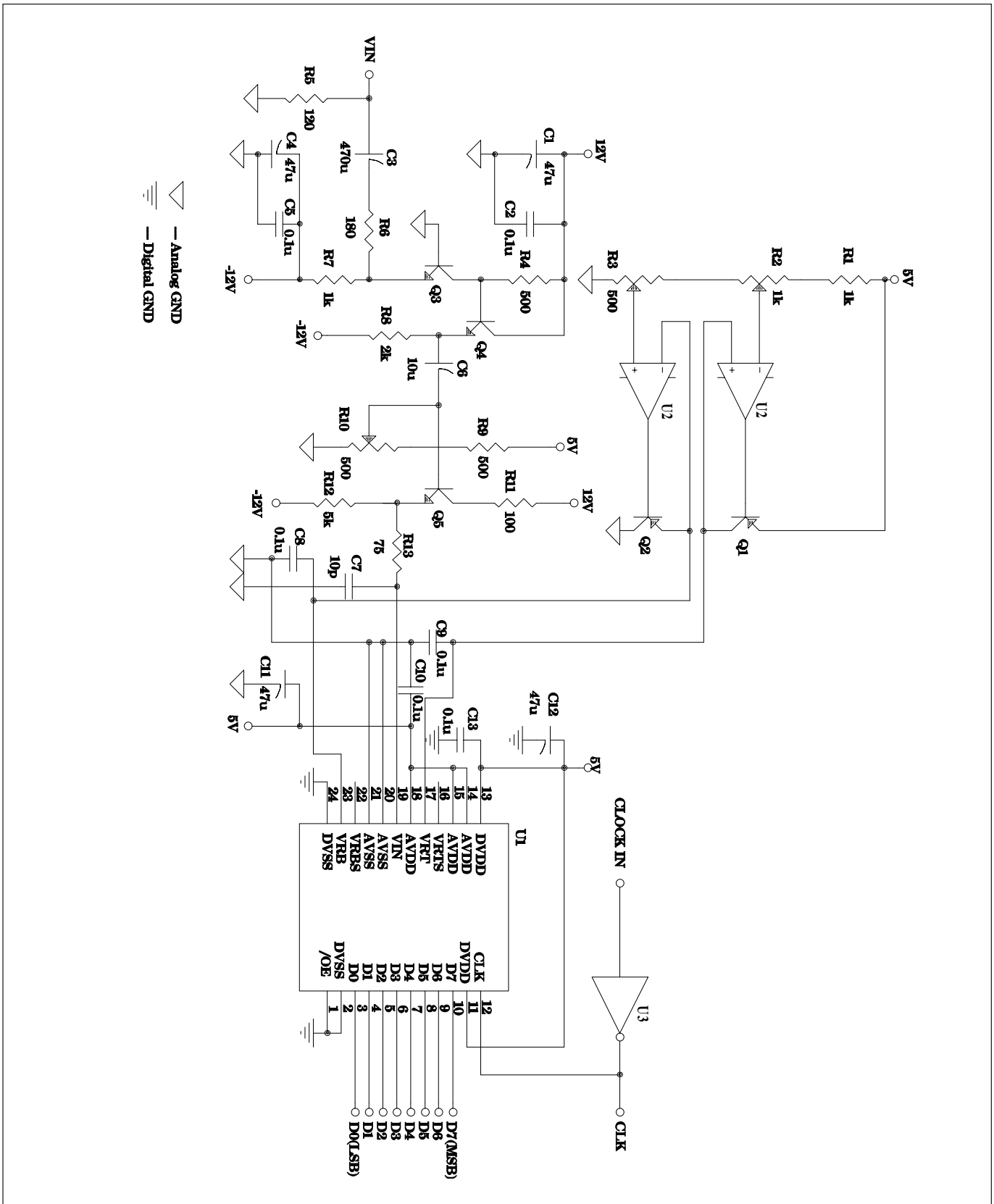
$\overline{\text{OE}}$  pin

By connecting  $\overline{\text{OE}}$  to GND output mode is obtained. By connecting to  $V_{\text{DD}}$  high impedance is obtained.

About latch up

It is necessary that  $\text{AV}_{\text{DD}}$  and  $\text{DV}_{\text{DD}}$  pins be the common source of power supply. This is to avoid latch up due to the voltage difference between  $\text{AV}_{\text{DD}}$  and  $\text{DV}_{\text{DD}}$  pins when power is ON.

Application Circuit



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