



# SPECIFICATION

## General Description

The EM39LV010 is a 1M bits Flash memory organized as 128K x 8 bits. The EM39LV010 uses 2.7-3.6V power supply for Program and Erase. Featuring high performance Flash memory technology, the EM39LV010 provides a typical Byte-Program time of 11  $\mu$ sec and a typical Sector-Erase time of 40 ms. The device uses Toggle Bit or Data# Polling to detect the completion of the Program or Erase operation. To protect against inadvertent write, the device has on-chip hardware and software data protection schemes. The device offers typical 100,000 cycles endurance and a greater than 10 years data retention. The EM39LV010 conforms to JEDEC standard pin outs for x8 memories. The EM39LV010 is offered in package types of 32-lead PLCC, 32-pin TSOP, 48-ball FBGA, and known good dice (KGD). For KGD, please contact ELAN Microelectronics or its representatives for detailed information (see Appendix at the bottom of this specification for Ordering Information).

The EM39LV010 devices are developed for applications that require memories with convenient and economical updating of program, data or configuration, e.g., Networking cards, Card Readers, Graphic cards, Digital TV, MP3, Wireless Phones, etc.

## Features

- **Single Power Supply**  
Full voltage range from 2.7 to 3.6 volts for both read and write operations
- **Sector-Erase Capability**  
Uniform 4Kbyte sectors
- **Read Access Time**  
Access time: 45, 70 and 90 ns
- **Power Consumption**  
Active current: 15 mA (Typical)  
Standby current: 1  $\mu$ A (Typical)
- **Erase/Program Features**  
Sector-Erase Time: 40 ms (Typical)  
Chip-Erase Time: 40 ms (Typical)  
Byte-Program Time: 11  $\mu$ s (Typical)  
Chip Rewrite Time: 1.5 seconds (Typical)
- **Automatic Write Timing**  
Internal  $V_{pp}$  Generation
- **End-of-Program or End-of-Erase Detection**  
Data# Polling  
Toggle Bit
- **CMOS I/O Compatibility**
- **JEDEC Standard**  
Pin-out and software command sets compatible with single-power supply Flash memory
- **High Reliability**  
Endurance cycles: 100K (Typical)  
Data retention: 10 years
- **Package Option**  
32-lead PLCC  
32-pin TSOP  
48-pin FBGA



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## Functional Block Diagram

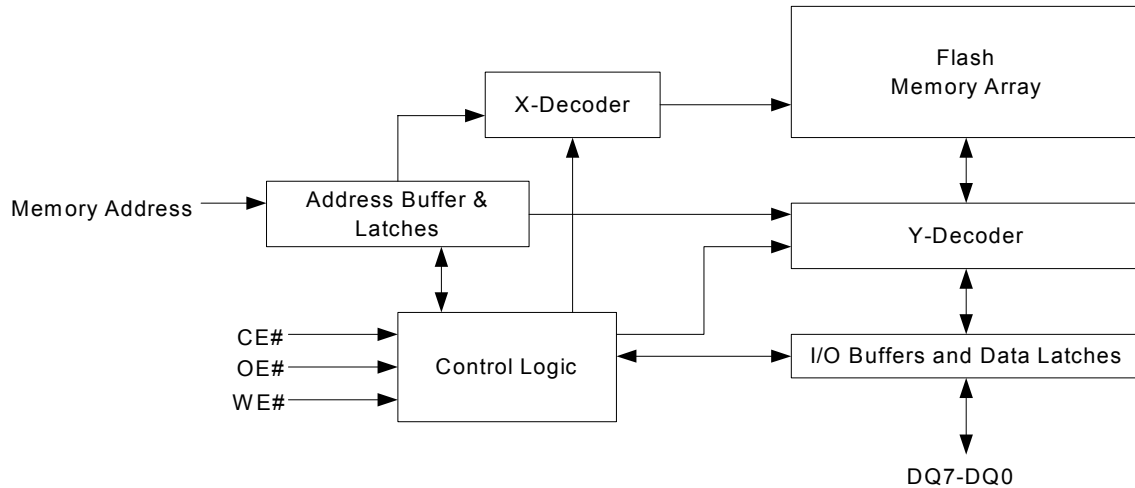


Figure 0a: Functional Block Diagram

## Pin Assignments

### PLCC

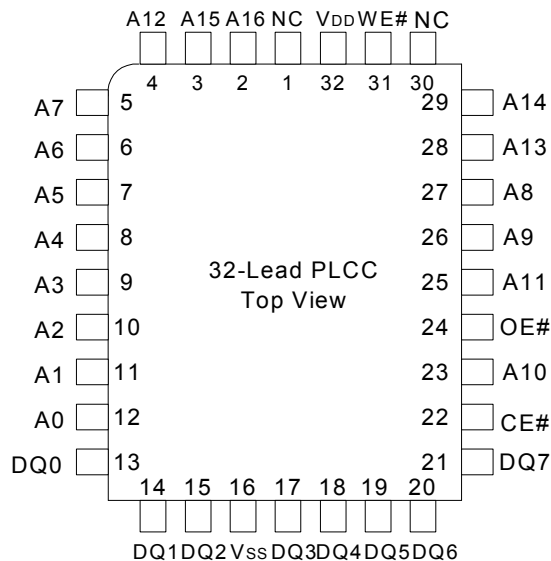
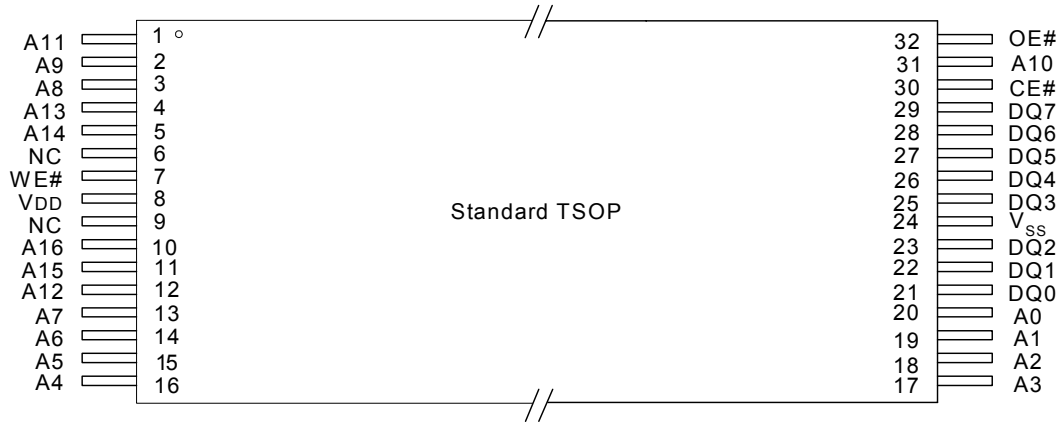


Figure 0b: 32-lead PLCC Pin Assignments



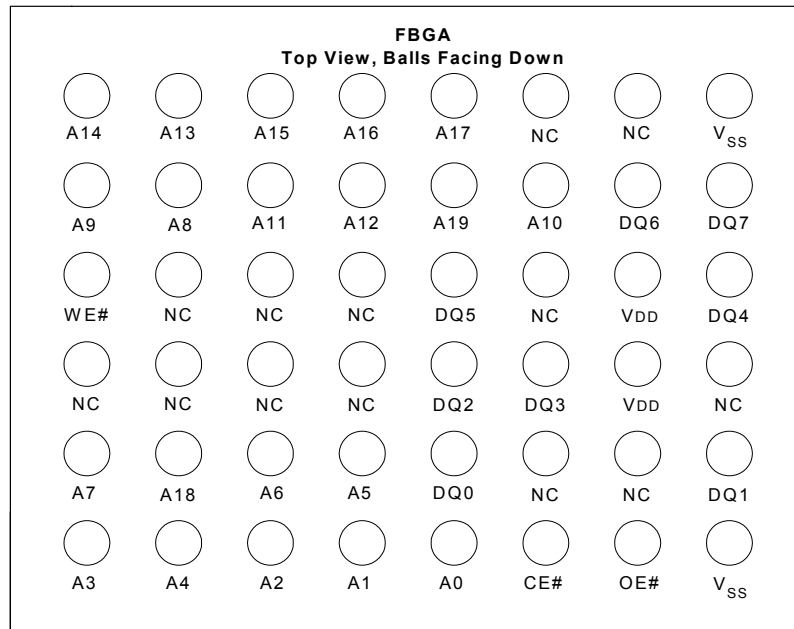
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**TSOP**



**Figure 0c: TSOP Pin Assignments**

**FBGA**



**Figure 0d: FBGA Pin Assignments**



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## Pin Description

Pin Name	Function
A0–A19	17 addresses
DQ7–DQ0	Data inputs/outputs
CE#	Chip enable
OE#	Output enable
WE#	Write enable
V <sub>DD</sub>	2.7-3.6 volt single power supply
V <sub>SS</sub>	Device ground
NC	Pin not connected internally

*Table 1: Pin Description*

## Device Operation

The EM39LV010 uses Commands to initiate the memory operation functions. The Commands are written to the device by asserting WE# Low while keeping CE# Low. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first.

### Read

The Read operation of the EM39LV010 is controlled by CE# and OE#. Both have to be Low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high. Refer to the Read Cycle Timing Diagram in Figure 1 for further details.

### Byte Program

The EM39LV010 is programmed on a byte-by-byte basis. Before programming, the sector where the byte is located; must be erased completely. The Program operation is accomplished in three steps:

- The first step is a three-byte load sequence for Software Data Protection.
- The second step is to load byte address and byte data. During the Byte Program operation, the addresses are latched on the falling edge of either CE# or WE#, whichever occurs last; and the data is latched on the rising edge of either CE# or WE#, whichever occurs first.
- The third step is the internal Program operation which is initiated after the rising edge of the fourth WE# or CE#, whichever occurs first. The Program operation, once initiated, will be completed within 16  $\mu$ s. See Figures 2 and 3 for WE# and CE# controlled Program operation timing diagrams respectively and Figure 12 for flowchart.



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During the Program operation, the only valid reads are Data# Polling and Toggle Bit. During internal Program operation, the host is free to perform additional tasks. Any command issued during the internal Program operation is ignored.

## EM39LV010 Device Operation

Operation	CE#	OE#	WE#	DQ	Address
Read	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	D <sub>OUT</sub>	A <sub>IN</sub>
Program	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	D <sub>IN</sub>	A <sub>IN</sub>
Erase	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	X*	Sector address, XXH for Chip-Erase
Standby	V <sub>IH</sub>	X	X	High Z	X
Write Inhibit	X	V <sub>IL</sub>	X	High Z/D <sub>OUT</sub>	X
Write Inhibit	X	X	V <sub>IH</sub>	High Z/D <sub>OUT</sub>	X
Software Mode	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>		See Table 3
Product Identification					

\* X can be V<sub>IL</sub> or V<sub>IH</sub>, but no other value.

**Table 2: EM39LV010 Device Operation**

## Write Command/Command Sequence

The EM39LV010 provides two software methods to detect the completion of a Program or Erase cycle in order to optimize the system write cycle time. The software detection includes two status bits: Data# Polling (DQ7) and Toggle Bit (DQ6). The End-of-Write detection mode is enabled after the rising edge of WE#, which initiates the internal Program or Erase operation. The actual completion of the write operation is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ7 or DQ6. In order to prevent such spurious rejection, when an erroneous result occurs, the software routine should include an additional two times loop to read the accessed location. If both reads are valid, then the device has completed the write cycle, otherwise the rejection is valid.

## Chip Erase

The EM39LV010 provides Chip-Erase feature, which allows the entire memory array to be erased to logic "1" state. The Chip-Erase operation is initiated by executing a six-byte command sequence with Chip-Erase command (10H) at address 5555H in the last byte sequence. The Erase operation begins with the rising edge of the sixth WE# or CE#, whichever occurs first. During the Erase operation, the only valid reads are Toggle Bit and Data# Polling. See Table 3 for the command sequence, Figure 6 for timing diagram, and Figure 15 for the flowchart. Any commands issued during the Chip-Erase operation are ignored.



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### **Sector Erase**

The EM39LV010 offers Sector-Erase mode. The Sector-Erase operation allows the system to erase the device on a sector-by-sector basis. The sector architecture is based on uniform sector size of 4 KByte. The Sector-Erase operation is initiated by executing a six-byte command sequence with Sector-Erase command (30H) and sector address (SA) in the last bus cycle. The sector address is latched on the falling edge of the sixth WE# pulse, while the command (30H) is latched on the rising edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse. The End-of-Erase operation can be determined by using either Data# Polling or Toggle Bit method. See Figures 7 for timing waveforms. Any commands issued during the Sector Erase operation are ignored.

### **Data# Polling (DQ7)**

When the EM39LV010 is in the internal Program operation, any attempt to read DQ7 will produce the complement of the true data. Once the Program operation is completed, DQ7 will produce the true data. Note that even though DQ7 may have valid data immediately following the completion of an internal Program operation, the remaining data outputs may still be invalid (valid data on the entire data bus will appear in subsequent successive Read cycles after an interval of 1  $\mu$ s). During internal Erase operation, any attempt to read DQ7 will produce a "0". Once the internal Erase operation is completed, DQ7 will produce a "1". The Data# Polling is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector-Erase or Chip-Erase, the Data# Polling is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 4 for Data# Polling timing diagram and Figure 13 for a flowchart.

### **Toggle Bit (DQ6)**

During the internal Program or Erase operation, any consecutive attempts to read DQ6 will produce alternating 1s and 0s, i.e., toggling between 1 and 0. When the internal Program or Erase operation is completed, the DQ6 bit will stop toggling. The device is then ready for the next operation. The Toggle Bit is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector-Erase or Chip-Erase, the Toggle Bit is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 5 for Toggle Bit timing diagram and Figure 13 for a flowchart.

### **Data Protection**

The EM39LV010 provides both hardware and software features to protect the data from inadvertent write.



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### **Hardware Data Protection**

Noise/Glitch Protection: A WE# or CE# pulse of less than 5 ns will not initiate a write cycle.

V<sub>DD</sub> Power Up/Down Detection: The Write operation is inhibited when V<sub>DD</sub> is less than 1.5V.

Write Inhibit Mode: Forcing OE# Low, CE# High, or WE# High will inhibit the Write operation. This prevents inadvertent write during power-up or power-down.

### **Software Data Protection (SDP)**

The EM39LV010 provides the JEDEC approved Software Data Protection (SDP) scheme for Program and Erase operations. Any Program operation requires the inclusion of the three-byte sequence. The three-byte load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, especially during the system power-up or power-down transition. Any Erase operation requires the inclusion of six-byte sequence. See Table 3 for the specific software command codes. During SDP command sequence, invalid commands will abort the device to Read mode within T<sub>RC</sub>.



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### Software Command Sequence

Command Sequence	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
	Addr <sup>1</sup>	Data	Addr <sup>1</sup>	Data	Addr <sup>1</sup>	Data	Addr <sup>1</sup>	Data	Addr <sup>1</sup>	Data	Addr <sup>1</sup>	Data
Byte Program	5555H	AAH	2AAAH	55H	5555H	A0H	BA <sup>2</sup>	Data				
Sector Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA <sub>X</sub> <sup>3</sup>	30H
Chip Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Software ID Entry <sup>4,6</sup>	5555H	AAH	2AAAH	55H	5555H	90H						
Manufacture ID	5555H	AAH	2AAAH	55H	5555H	90H	0000H	7FH				
Manufacture ID	5555H	AAH	2AAAH	55H	5555H	90H	0003H	7FH				
Manufacture ID	5555H	AAH	2AAAH	55H	5555H	90H	0040H	1FH				
Device ID	5555H	AAH	2AAAH	55H	5555H	90H	0001H	A8H				
Software ID Exit <sup>5</sup> /CFI Exit	XXH	F0H										
Software ID Exit <sup>5</sup> /CFI Exit	5555H	AAH	2AAAH	55H	5555H	F0H						

**Notes:**

1. Address format A15-A0 (Hex), Address A16 can be V<sub>IL</sub> or V<sub>IH</sub>, but no other value, for the Command sequence.
2. BA = Program byte address.
3. SA<sub>X</sub> for Sector-Erase; uses A16-A12 address lines.
4. The device does not remain in Software Product ID mode if powered down.
5. Both Software ID Exit operations are equivalent.
6. Refer to Figure 9 for more information.

**Table 3: Software Command Sequence**





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**Absolute Maximum Ratings**

**NOTE**

*Applied conditions greater than those listed under these ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this specification, are not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.*

Temperature Under Bias .....	-55°C to 125°C
Storage Temperature .....	-65°C to 150°C
D.C. Voltage on Any Pin to Ground Potential .....	-0.5 V to $V_{DD}+0.5V$
Transient Voltage (<20ns) on Any Pin to Ground Potential .....	-2.0V to $V_{DD} +2.0V$
Voltage on A9 Pin to Ground Potential .....	-0.5 V to 13.2V
Package Power Dissipation Capability (Ta=25°C).....	1.0W
Surface Mount Lead Soldering Temperature (3 Seconds).....	240°C
Output Short Circuit Current * .....	50mA

\* Output shorted for no more than one second.  
 No more than one output shorted at a time.

**Operating Range**

Model Name	Ambient Temperature	$V_{DD}$
EM39LV010	0°C to +70°C	2.7~3.6V

*Table 4: Operating Range*

**AC Conditions of Test**

Input Rise/Fall Time .....	5ns
Output Load .....	CL=30pF for 45Rns
Output Load .....	CL=100pF for 70ns/90ns
See Figures 10 and 11	



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## DC CHARACTERISTICS (CMOS Compatible)

Parameter	Description	Test Conditions	Min	Max	Unit
I <sub>DD</sub>	Power Supply Current	Address Input =V <sub>IL</sub> /V <sub>IH</sub> , at f=1/T <sub>RC</sub> Min, V <sub>DD</sub> =V <sub>DD</sub> Max			
	Read	CE#=OE#=V <sub>IL</sub> , WE#=V <sub>IH</sub> , all I/Os open		20	mA
	Program and Erase	CE#=WE#=V <sub>IL</sub> , OE#=V <sub>IH</sub> ,		30	mA
I <sub>SB</sub>	Standby V <sub>DD</sub> Current	CE#=V <sub>IHC</sub> , V <sub>DD</sub> =V <sub>DD</sub> Max		15	μA
I <sub>LI</sub>	Input Leakage Current	V <sub>IN</sub> =GND to V <sub>DD</sub> , V <sub>DD</sub> =V <sub>DD</sub> Max		1	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> =GND to V <sub>DD</sub> , V <sub>DD</sub> =V <sub>DD</sub> Max		10	μA
V <sub>IL</sub>	Input Low Voltage	V <sub>DD</sub> =V <sub>DD</sub> Min		0.8	V
V <sub>IH</sub>	Input High Voltage	V <sub>DD</sub> =V <sub>DD</sub> Max	0.7 V <sub>DD</sub>		V
V <sub>IHC</sub>	Input High Voltage (CMOS)	V <sub>DD</sub> =V <sub>DD</sub> Max	V <sub>DD</sub> -0.3		V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> =100μA, V <sub>DD</sub> =V <sub>DD</sub> Min		0.2	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> =-100μA, V <sub>DD</sub> =V <sub>DD</sub> Min	V <sub>DD</sub> -0.2		V

*Table 5: DC Characteristics (Cmos Compatible)*

## Recommended System Power-up Timing

Parameter	Description	Min	Unit
T <sub>PU-READ</sub> *	Power-up to Read Operation	100	μs
T <sub>PU-WRITE</sub> *	Power-up to Program/Erase Operation	100	μs

\* This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

*Table 6: Recommended System Power-up Timing*

## Capacitance (Ta=25°C, f=1Mhz, other pins open)

Parameter	Description	Test Conditons	Max
C <sub>I/O</sub> *	I/O Pin Capacitance	V <sub>I/O</sub> =0V	12pF
C <sub>IN</sub> *	Input Capacitance	V <sub>IN</sub> =0V	6pF

\* This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

*Table 7: Capacitance (Ta=25°C, f=1Mhz, Other Pins Open)*

## Reliability Characteristics

Symbol	Parameter	Min Specification	Unit	Test Method
N <sub>END</sub> *	Endurance	10,000	Cycles	JEDEC Standard A117
T <sub>DR</sub> *	Data Retention	10	Years	JEDEC Standard A103
I <sub>LTH</sub> *	Latch Up	100+I <sub>DD</sub>	mA	JEDEC Standard 78

\* This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

*Table 8: Reliability Characteristics*



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## AC Characteristics

### Read Cycle Timing Parameters

Symbol	Parameter	45REC		70REC		90REC		Unit
		Min	Max	Min	Max	Min	Max	
T <sub>RC</sub>	Read Cycle Time	45		70		90		ns
T <sub>CE</sub>	Chip Enable Access Time		45		70		90	ns
T <sub>AA</sub>	Address Access Time		45		70		90	ns
T <sub>OE</sub>	Output Enable Access Time		30		35		45	ns
T <sub>CLZ</sub> *	CE# Low to Active Output	0		0		0		ns
T <sub>OLZ</sub> *	OE# Low to Active Output	0		0		0		ns
T <sub>CHZ</sub> *	CE# High to High-Z Output		15		25		30	ns
T <sub>OHZ</sub> *	OE# High to High-Z Output		15		25		30	ns
T <sub>OH</sub> *	Output Hold from Address Change	0		0		0		ns

\* This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

**Table 9a: Read Cycle Timing Parameters**

Symbol	Parameter	45EC		70EC		90EC		Unit
		Min	Max	Min	Max	Min	Max	
T <sub>RC</sub>	Read Cycle Time	45		70		90		ns
T <sub>CE</sub>	Chip Enable Access Time		45		70		90	ns
T <sub>AA</sub>	Address Access Time		45		70		90	ns
T <sub>OE</sub>	Output Enable Access Time		30		35		45	ns
T <sub>CLZ</sub> *	CE# Low to Active Output	0		0		0		ns
T <sub>OLZ</sub> *	OE# Low to Active Output	0		0		0		ns
T <sub>CHZ</sub> *	CE# High to High-Z Output		15		25		30	ns
T <sub>OHZ</sub> *	OE# High to High-Z Output		15		25		30	ns
T <sub>OH</sub> *	Output Hold from Address Change	0		0		0		ns

\* This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

**Table 9b: Read Cycle Timing Parameters**

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## Program/Erase Cycle Timing Parameter

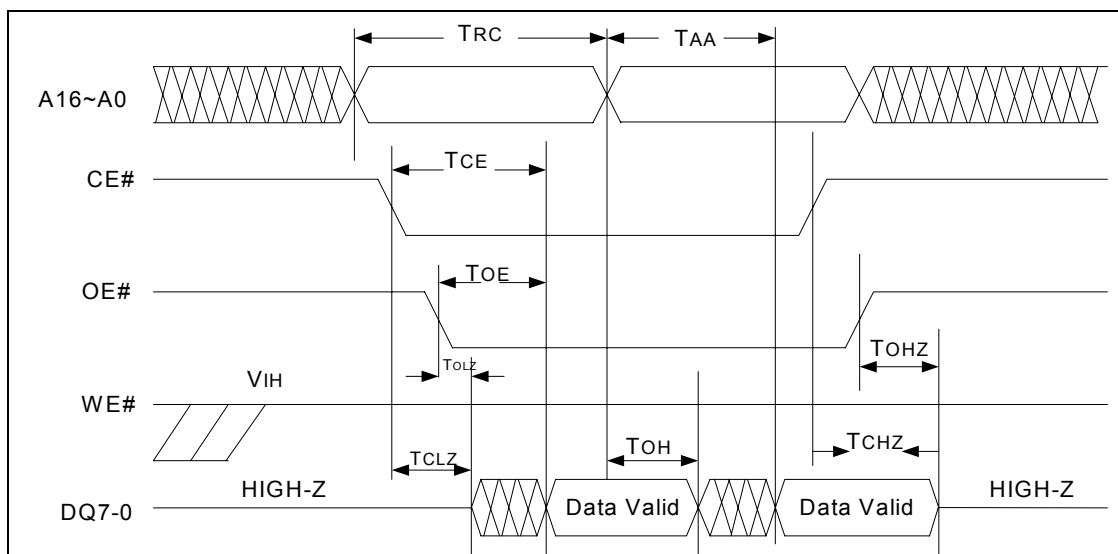
Symbol	Parameter	Min	Max	Unit
$T_{BP}$	Byte-Program Time		16	$\mu$ s
$T_{AS}$	Address Setup Time	0		ns
$T_{AH}$	Address Hold Time	30		ns
$T_{CS}$	WE# and CE# Setup Time	0		ns
$T_{CH}$	WE# and CE# Hold Time	0		ns
$T_{OES}$	OE# High Setup Time	0		ns
$T_{OEH}$	OE# High Hold Time	10		ns
$T_{CP}$	CE# Pulse Width	40		ns
$T_{WP}$	WE# Pulse Width	40		ns
$T_{WPH}^*$	WE# Pulse Width High	30		ns
$T_{CPH}^*$	CE# Pulse Width High	30		ns
$T_{DS}$	Data Setup Time	40		ns
$T_{DH}^*$	Data Hold Time	0		ns
$T_{IDA}^*$	Software ID Access and Exit Time		150	ns
$T_{SE}$	Sector Erase		30	ms
$T_{SCE}$	Chip Erase		60	ms

\* This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

**Table 10: Program/Erase Cycle Timing Parameter**

## Timing Diagrams

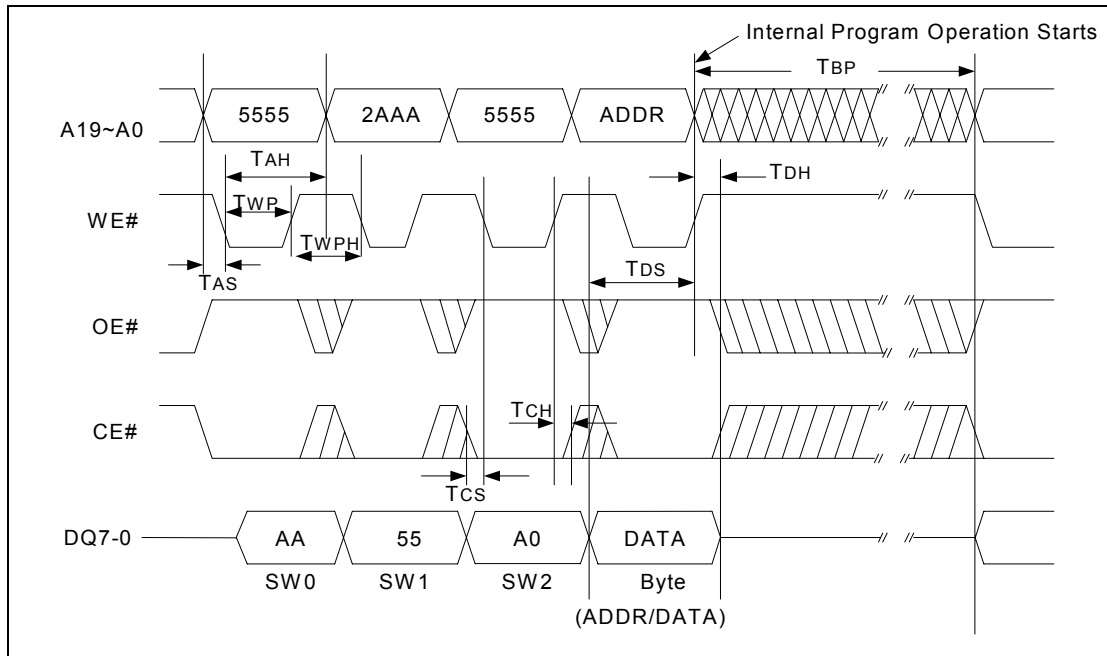
### Read Cycle Timing Diagram



**Figure 1: Read Cycle Timing Diagram**

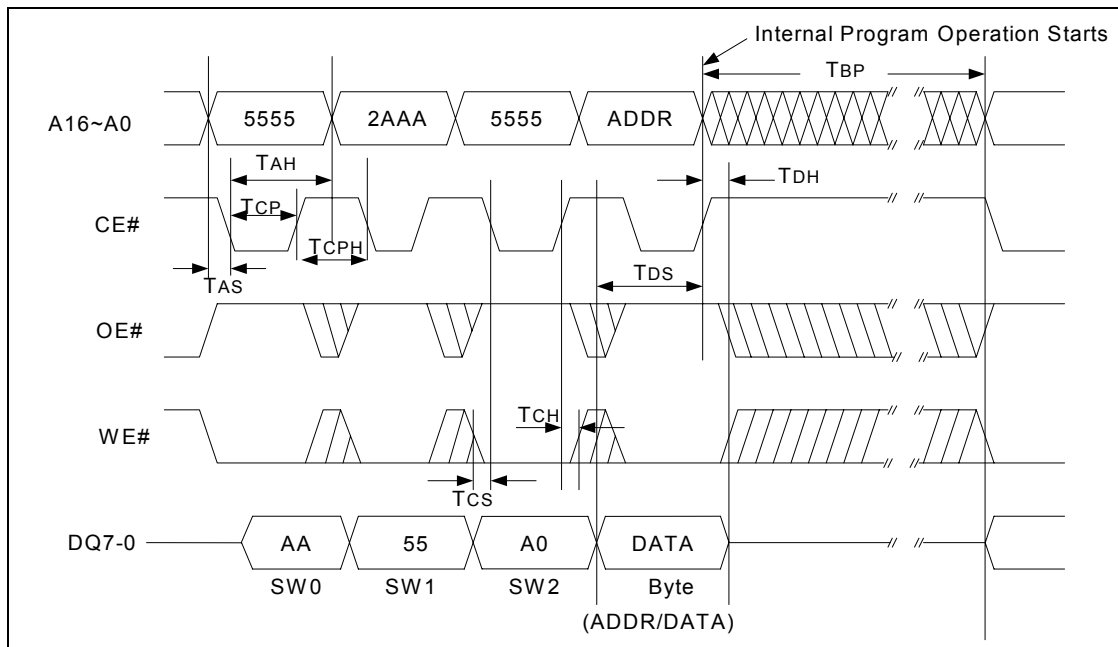
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## WE# Controlled Program Cycle Timing Diagram



**Figure 2: WE# Controlled Program Cycle Timing Diagram**

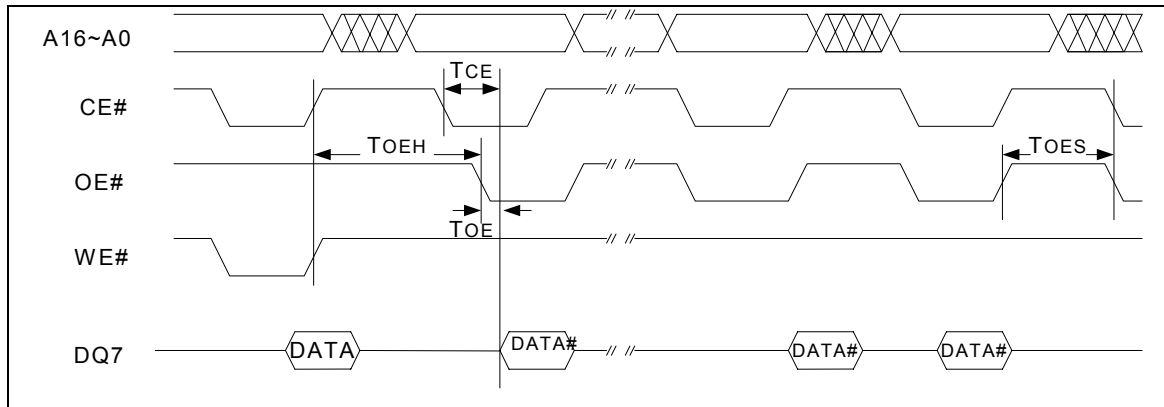
## CE# Controlled Program Cycle Timing Diagram



**Figure 3: CE# Controlled Program Cycle Timing Diagram**

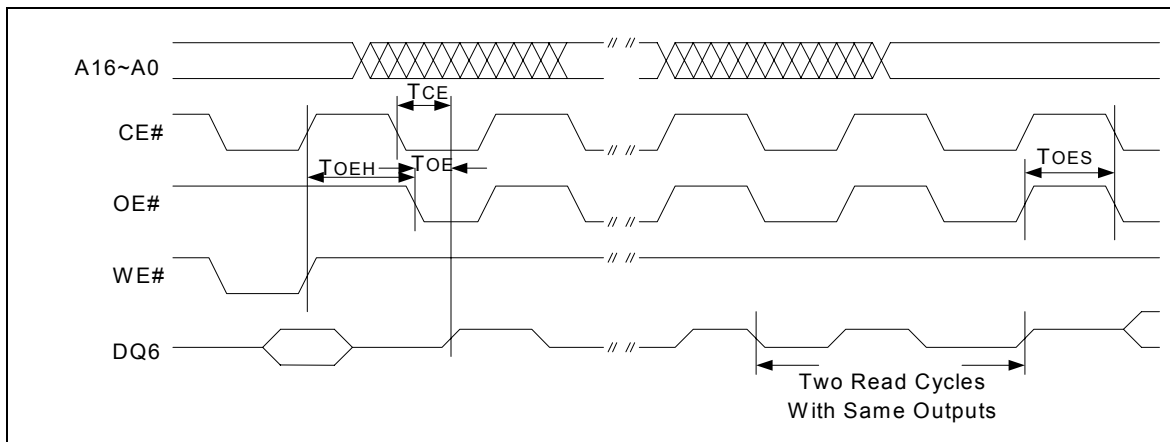
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## Data# Polling Timing Diagram



*Figure 4: Data# Polling Timing Diagram*

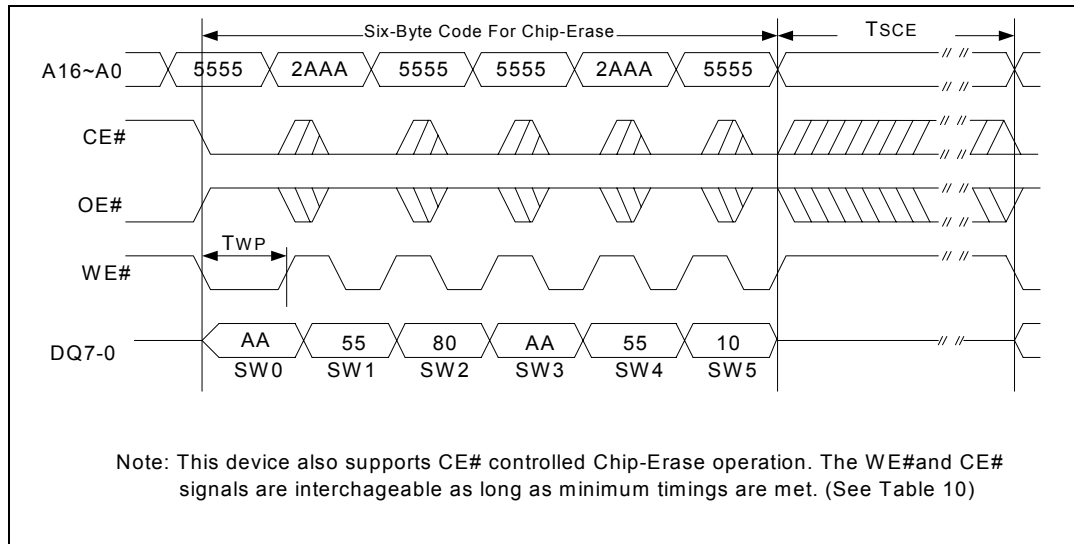
## Toggle Bit Timing Diagram



*Figure 5: Toggle Bit Timing Diagram*

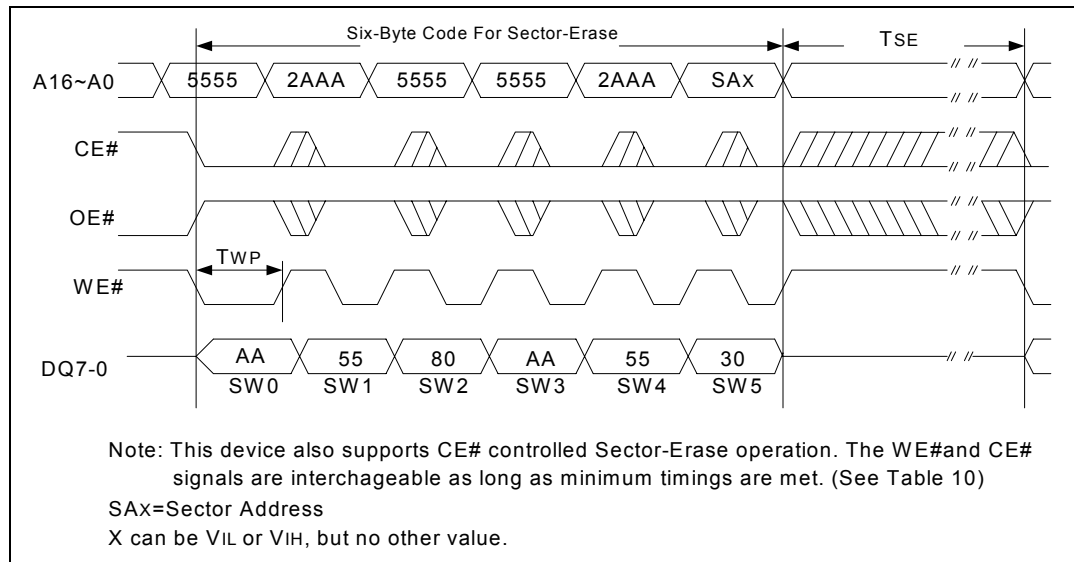
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## WE# Controlled Chip-Erase Timing Diagram



**Figure 6: WE# Controlled Chip-Erase Timing Diagram**

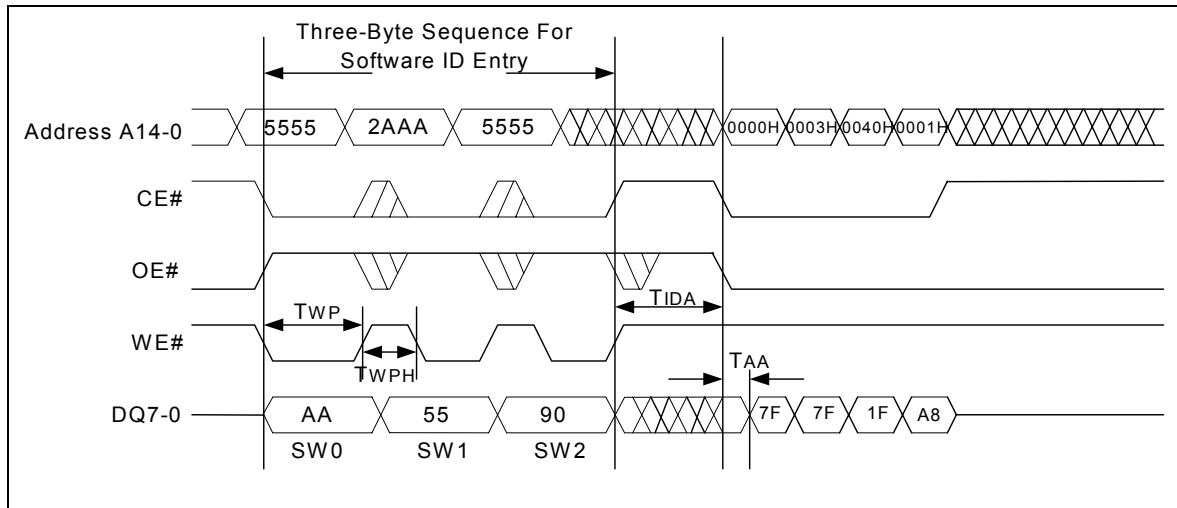
## WE# Controlled Sector-Erase Timing Diagram



**Figure 7: WE# Controlled Sector-Erase Timing Diagram**

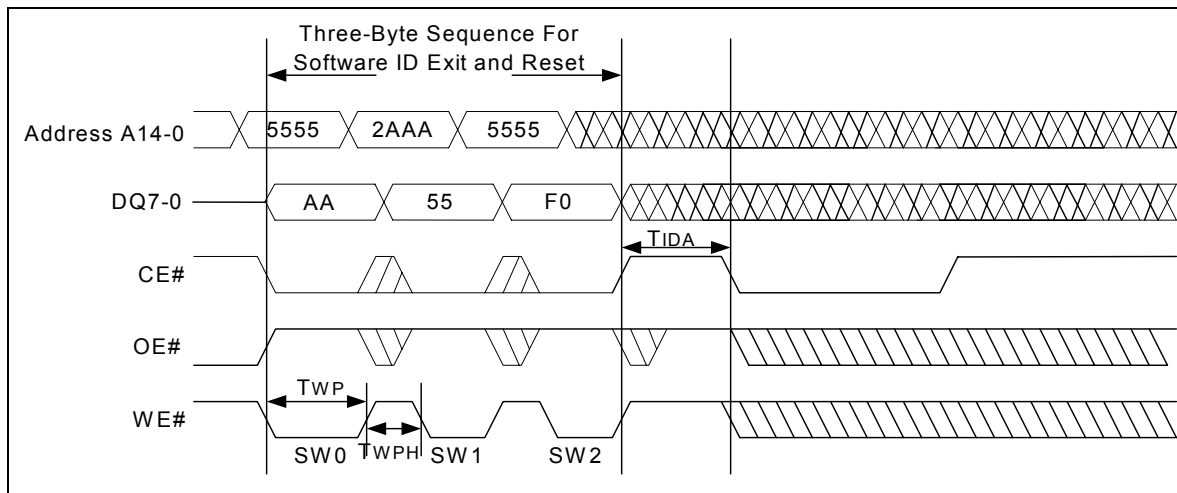
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## Software ID Entry and Read



**Figure 8: Software ID Entry and Read**

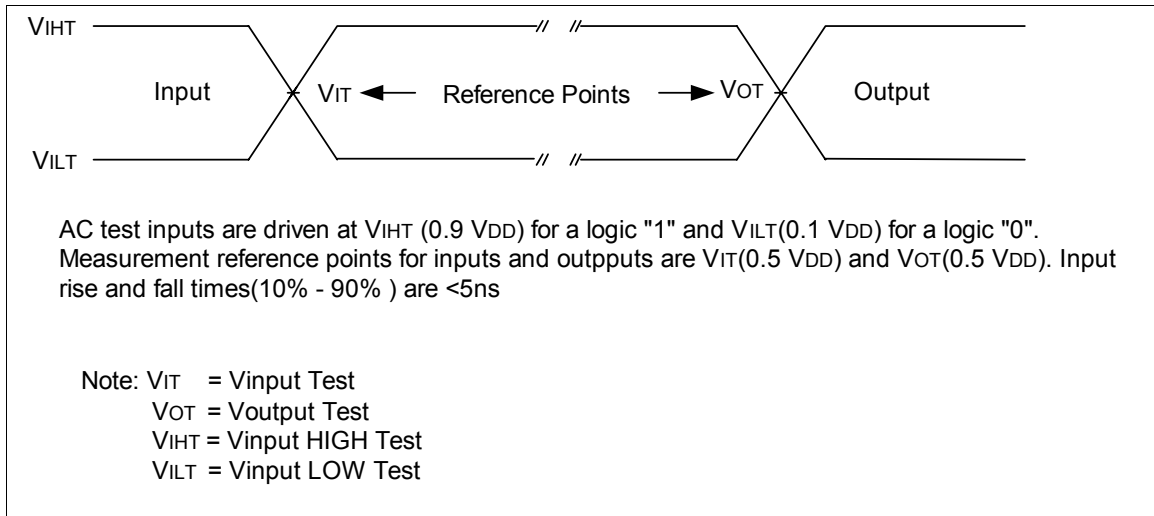
## Software ID Exit and Reset



**Figure 9: Software ID Exit and Reset**

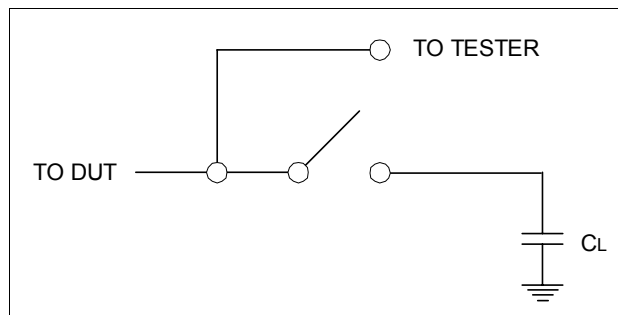


**AC Input/Output Reference Waveforms**



*Figure 10: AC Input/Output Reference Waveforms*

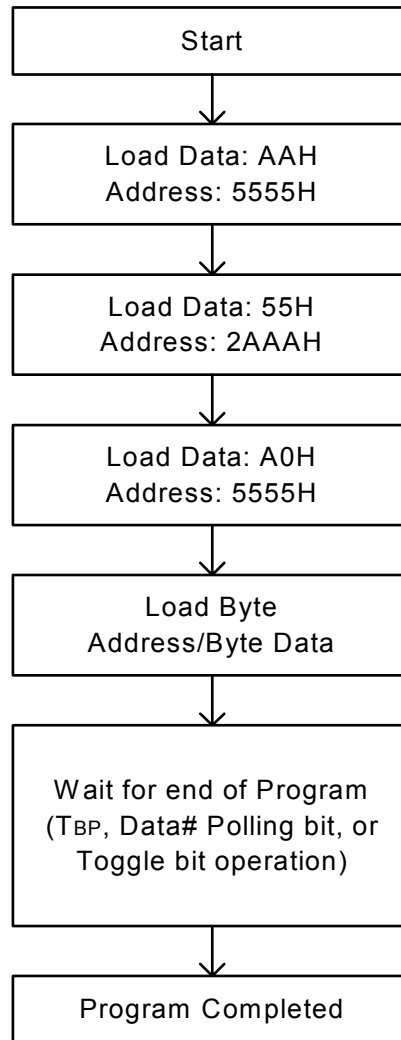
**A Test Load Example**



*Figure 11: A Test Load Example*

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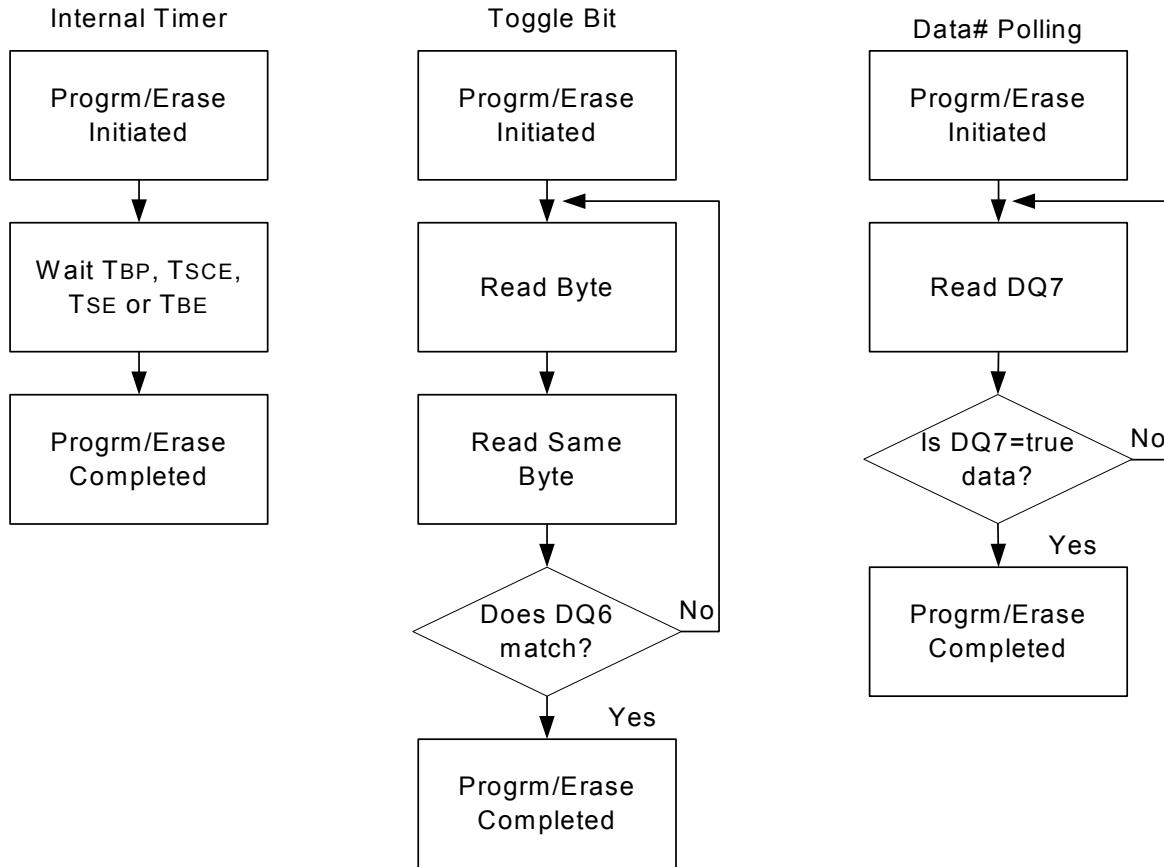
## Byte-Program Algorithm



**Figure 12:** Byte-Program Algorithm

**Flow Charts**

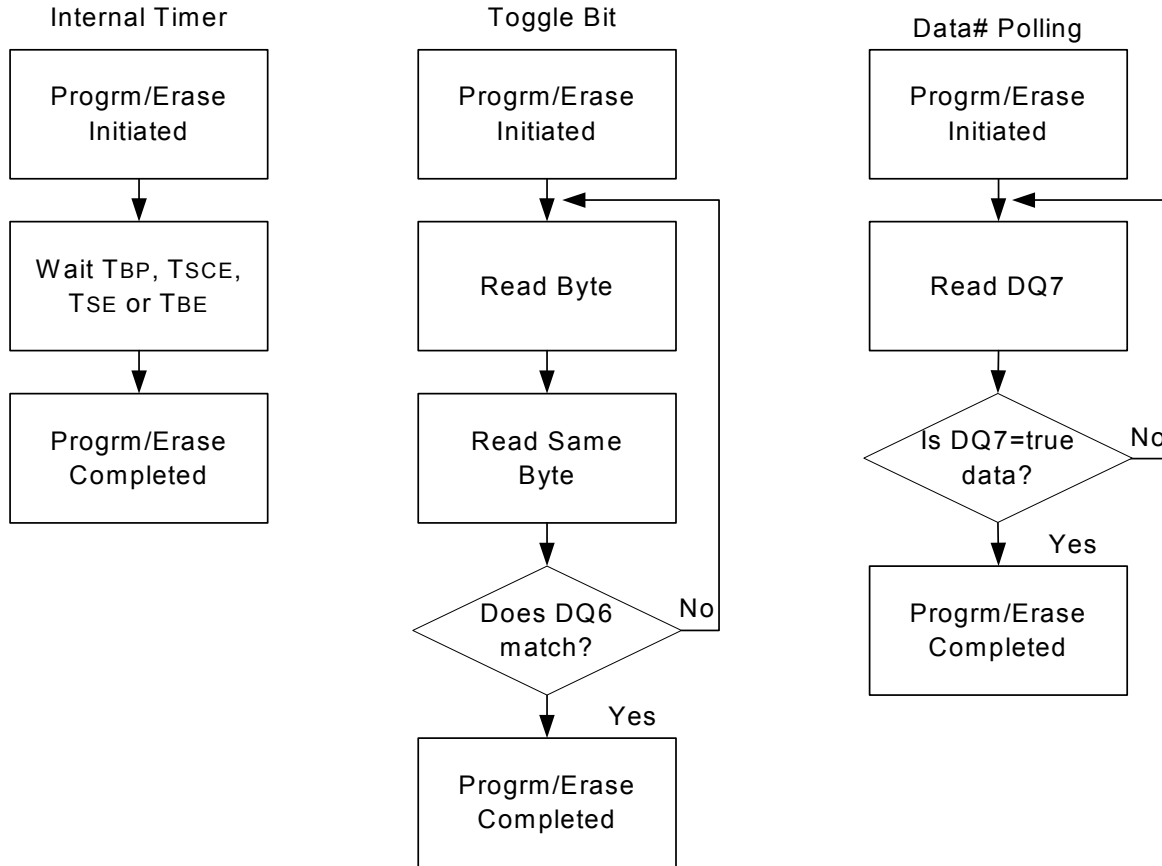
**Wait Options**



**Figure 13: Wait Options**

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## Software ID Command Flowcharts

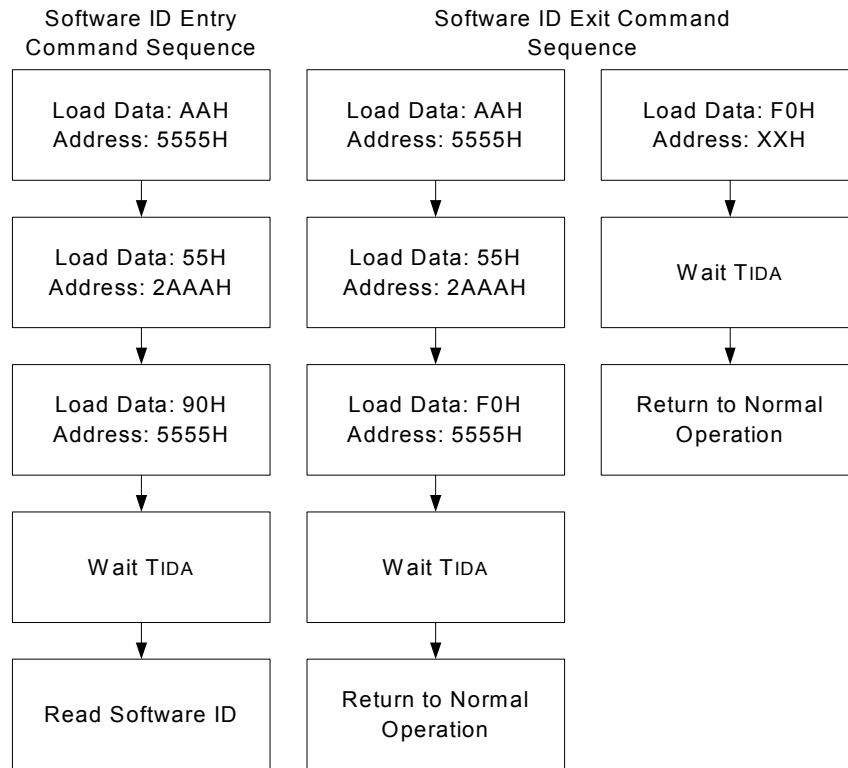


X can be VIL or VIH, but no other value.

**Figure 14:** Software ID Command Flowcharts

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## Erase Command Sequence



*X can be VIL or VIH, but no other value.*

**Figure 15: Erase Command Sequence**

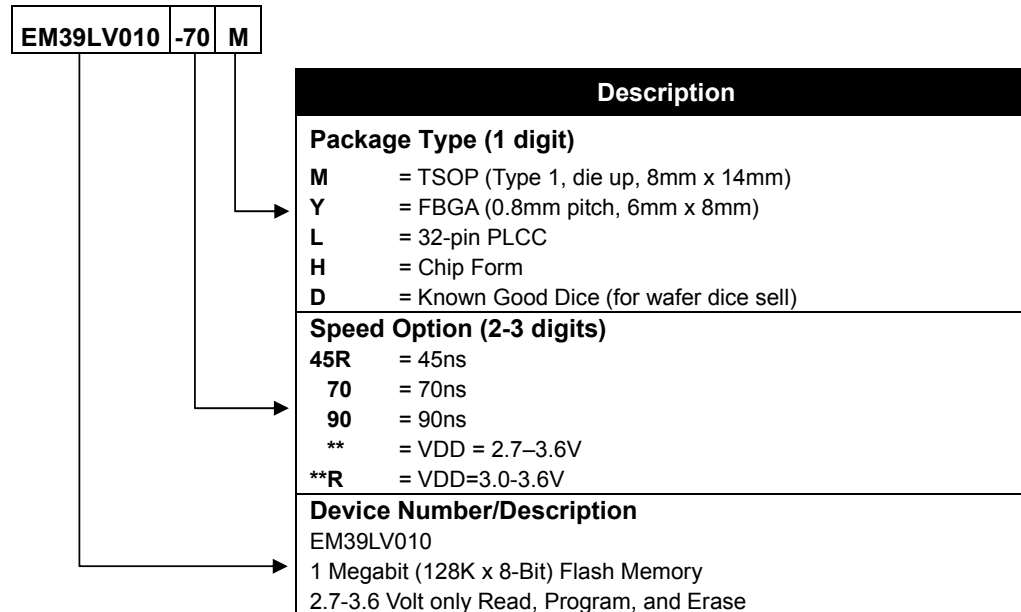


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## Appendix

### ORDERING INFORMATION (Standard Products)

The order number is defined by a combination of the following elements.





## **SPECIFICATION**

### **ORDERING INFORMATION (Non-Standard Products)**

For Known Good Dice (KGD), please contact ELAN Microelectronics at the following contact information or its representatives.

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