



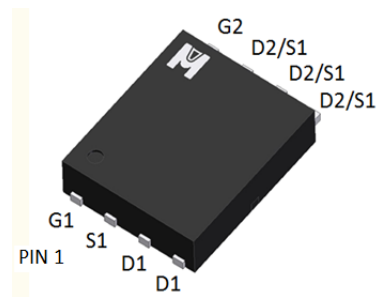
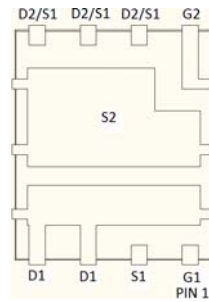
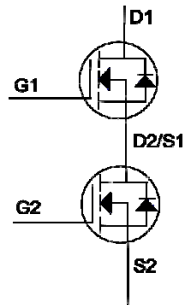
N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

	N-CH-Q1	N-CH-Q2
BV <sub>DSS</sub>	30V	30V
R <sub>DS(on)</sub> (MAX.)	5.0mΩ	2.0mΩ
I <sub>D</sub>	53A	95A

UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS		UNIT
			Q1	Q2	
Gate-Source Voltage		V <sub>GS</sub>	±20	±20	V
Continuous Drain Current <sup>3</sup>	T <sub>C</sub> = 25 °C	I <sub>D</sub>	53	95	A
	T <sub>C</sub> = 100 °C		33	60	
Pulsed Drain Current <sup>1</sup>		I <sub>DM</sub>	130	170	
Continuous Drain Current <sup>3</sup>	T <sub>A</sub> = 25 °C	I <sub>D</sub>	21	37	
	T <sub>A</sub> = 70 °C		17	30	
Avalanche Current		I <sub>AS</sub>	30	65	
Avalanche Energy	L = 0.1mH, R <sub>G</sub> =25Ω	E <sub>AS</sub>	45	211	mJ
Repetitive Avalanche Energy <sup>2</sup>	L = 0.05mH	E <sub>AR</sub>	22	105	
Power Dissipation	T <sub>C</sub> = 25 °C	P <sub>D</sub>	25	31	W
	T <sub>C</sub> = 100 °C		10	12.5	
Power Dissipation	T <sub>A</sub> = 25 °C	P <sub>D</sub>	1.8	1.9	W
	T <sub>A</sub> = 70 °C		1.1	1.2	
Operating Junction & Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	-55 to 150		°C



**THERMAL RESISTANCE RATINGS**

THERMAL RESISTANCE	SYMBOL		TYPICAL	MAXIMUM		UNIT
Junction-to-Case	$R_{\theta JC}$	Steady State		5	4	°C / W
Junction-to-Ambient	$R_{\theta JA}$	Steady State		70	65	
	$R_{\theta JA}$	$t \leq 10$ s		30	25	

<sup>1</sup>Pulse width limited by maximum junction temperature.

<sup>2</sup>Duty cycle  $\leq 1\%$

<sup>3</sup>Package limitation current, Q1=30A, Q2=36A

$R_{\theta JA}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT	
			MIN	TYP	MAX		
<b>STATIC</b>							
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	Q1	30		V	
			Q2	30			
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	Q1	1	1.5	3	
			Q2	1	1.5	3	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±20V	Q1			±100	nA
			Q2			±100	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 24V, V <sub>GS</sub> = 0V	Q1			1	μA
			Q2			1	
		V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125 °C	Q1			25	
			Q2			25	
On-State Drain Current <sup>1</sup>	I <sub>D(ON)</sub>	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 10V	Q1	53		A	
			Q2	95			
Drain-Source On-State Resistance <sup>1</sup>	R <sub>DS(ON)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 16A	Q1		4.0	5.0	mΩ
		V <sub>GS</sub> = 10V, I <sub>D</sub> = 25A	Q2		1.6	2.0	
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 10A	Q1		6.0	7.8	
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 15A	Q2		2.3	3.0	
Forward Transconductance <sup>1</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 5V, I <sub>D</sub> = 16A	Q1		50	S	
		V <sub>DS</sub> = 5V, I <sub>D</sub> = 25A	Q2		70		
<b>DYNAMIC</b>							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 15V, f = 1MHz	Q1		1508	pF	
			Q2		3813		
Output Capacitance	C <sub>oss</sub>		Q1		219		
			Q2		540		
Reverse Transfer Capacitance	C <sub>rss</sub>		Q1		167		
			Q2		440		
Gate Resistance	R <sub>g</sub>	V <sub>GS</sub> = 15mV, V <sub>DS</sub> = 0V, f = 1MHz	Q1		0.9	Ω	
			Q2		1.5		
Total Gate Charge <sup>1,2</sup>	Q <sub>g</sub> (V <sub>GS</sub> =10V)	Q1 V <sub>DD</sub> = 15V, V <sub>GS</sub> = 10V, I <sub>D</sub> = 16A	Q1		25	nC	
			Q2		59		
	Q <sub>g</sub> (V <sub>GS</sub> =4.5V)		Q1		13		
			Q2		28		



Gate-Source Charge <sup>1,2</sup>	$Q_{gs}$	Q2 $V_{DD} = 15V, V_{GS} = 10V,$ $I_D = 25A$	Q1		5		
			Q2		13		
Gate-Drain Charge <sup>1,2</sup>	$Q_{gd}$		Q1		5.3		
			Q2		11		
Turn-On Delay Time <sup>1,2</sup>	$t_{d(on)}$		Q1		20		nS
			Q2		25		
Rise Time <sup>1,2</sup>	$t_r$	$V_{DD} = 15V,$	Q1		15		
			Q2		16		
Turn-Off Delay Time <sup>1,2</sup>	$t_{d(off)}$	$I_D = 1A, V_{GS} = 10V, R_{GS} = 2.7\Omega$	Q1		55		
			Q2		60		
Fall Time <sup>1,2</sup>	$t_f$		Q1		20		
			Q2		25		
<b>SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (<math>T_J = 25\text{ }^\circ\text{C}</math>)</b>							
Continuous Current	$I_S$		Q1			20	A
			Q2			33	
Forward Voltage <sup>1</sup>	$V_{SD}$	$I_F = 10A, V_{GS} = 0V$	Q1			1.2	V
			Q2			1.2	
Reverse Recovery Time	$t_{rr}$	Q1 $I_F = 16A, di_F/dt = 100A / \mu S$	Q1		30		nS
			Q2		35		
Reverse Recovery Charge	$Q_{rr}$	Q2 $I_F = 25A, di_F/dt = 100A / \mu S$	Q1		18		nC
			Q2		25		

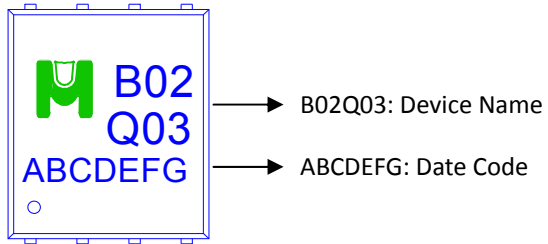
<sup>1</sup>Pulse test : Pulse Width  $\leq 300\ \mu\text{sec}$ , Duty Cycle  $\leq 2\%$ .

<sup>2</sup>Independent of operating temperature.

<sup>3</sup>Pulse width limited by maximum junction temperature.

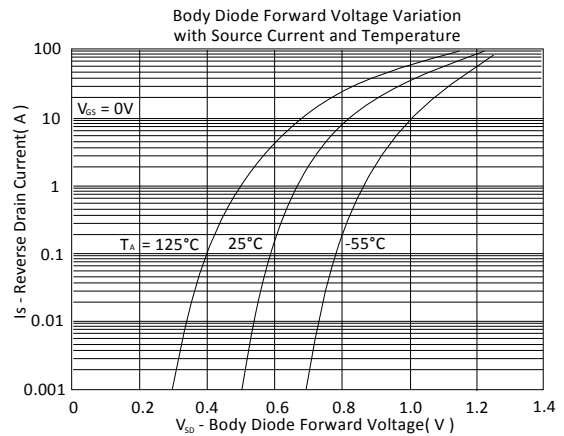
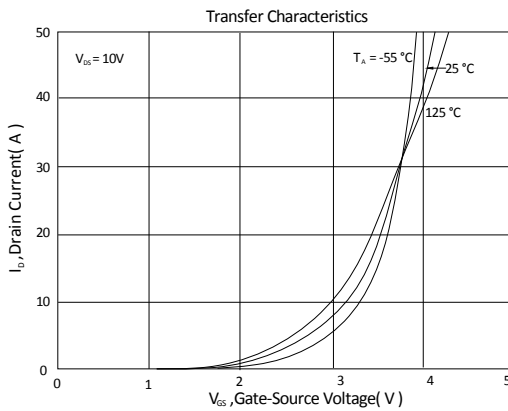
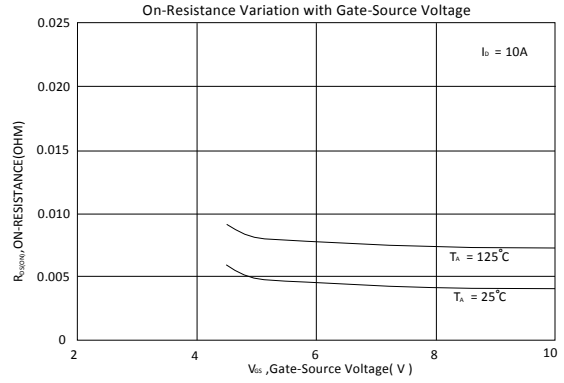
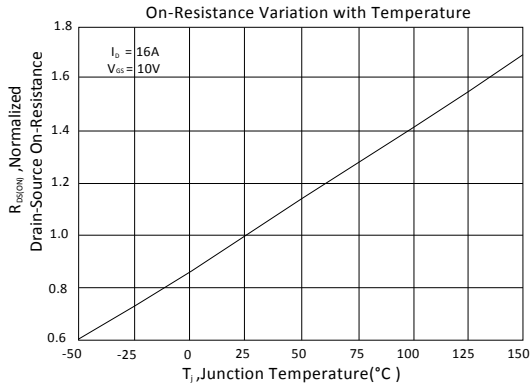
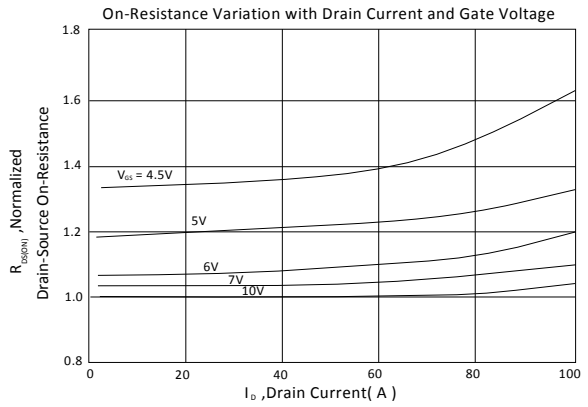
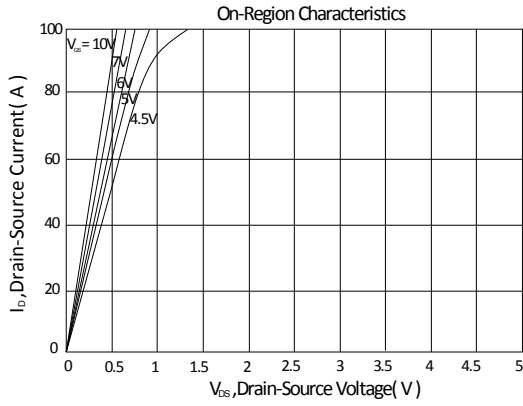
**Ordering & Marking Information:**

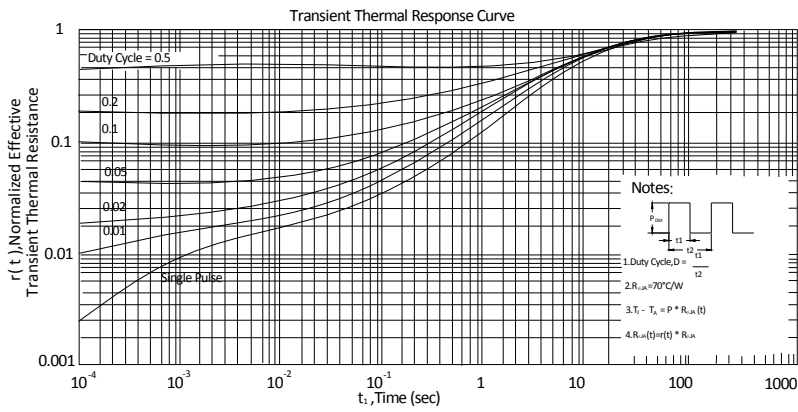
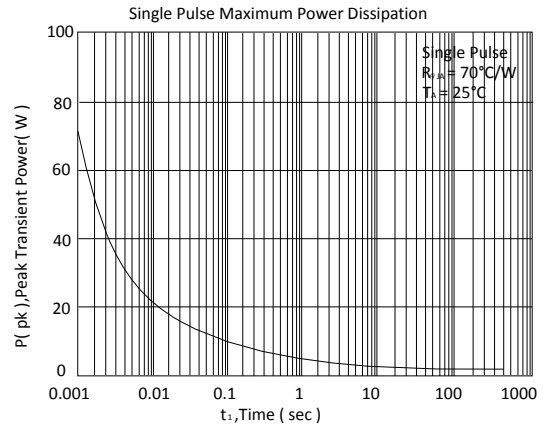
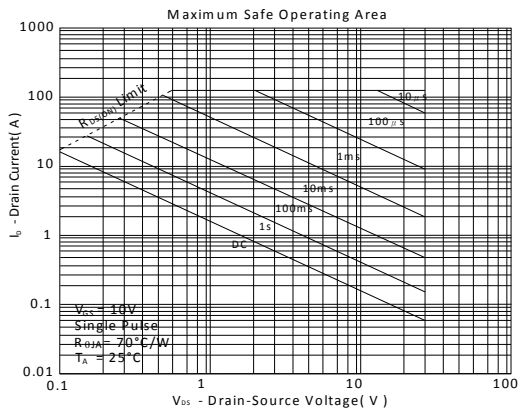
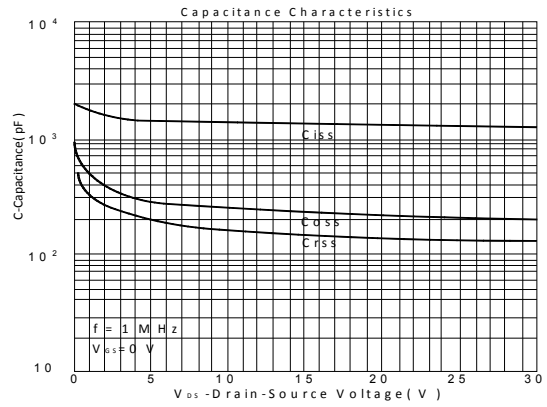
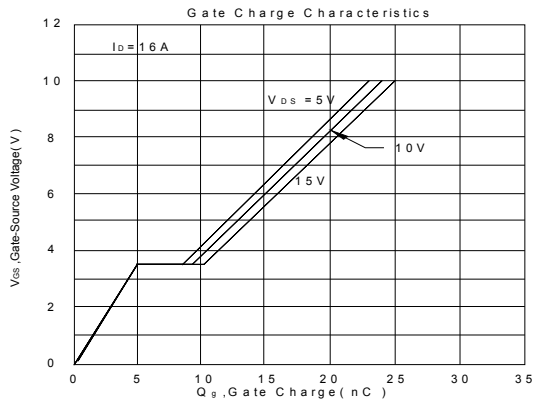
Device Name: EMB02Q03HP for Asymmetric Dual EDFN 5 x 6





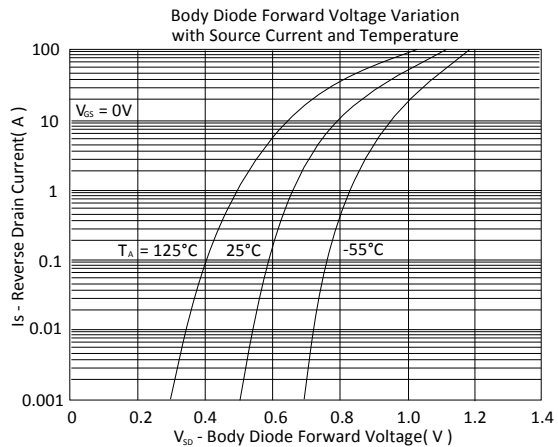
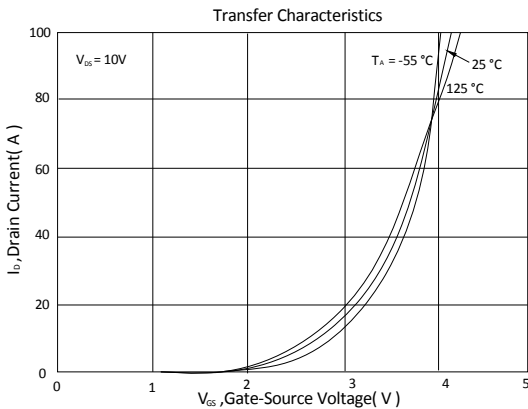
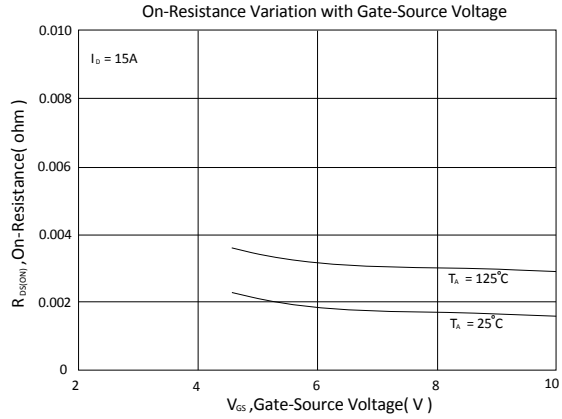
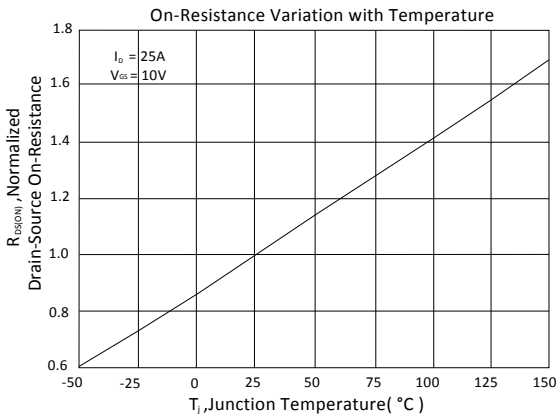
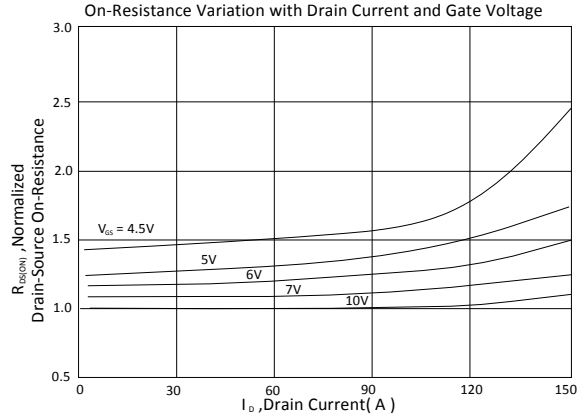
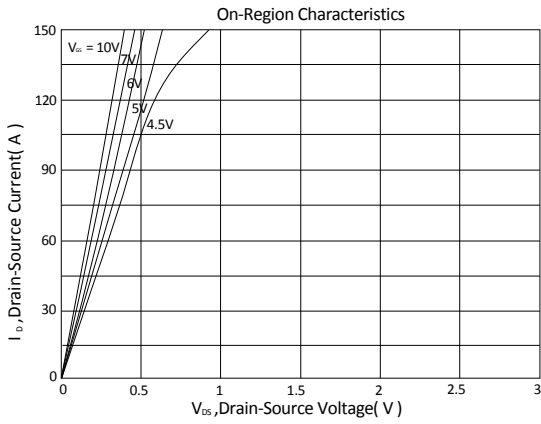
Q1 TYPICAL CHARACTERISTICS



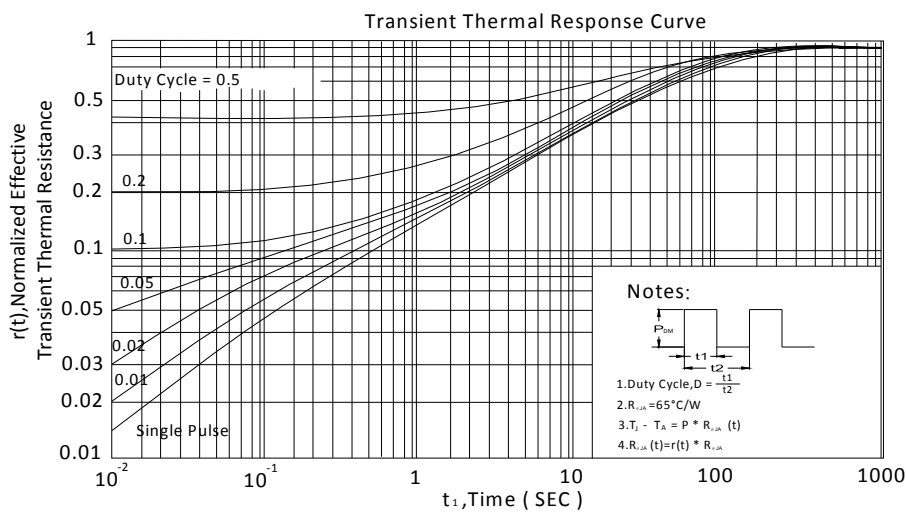
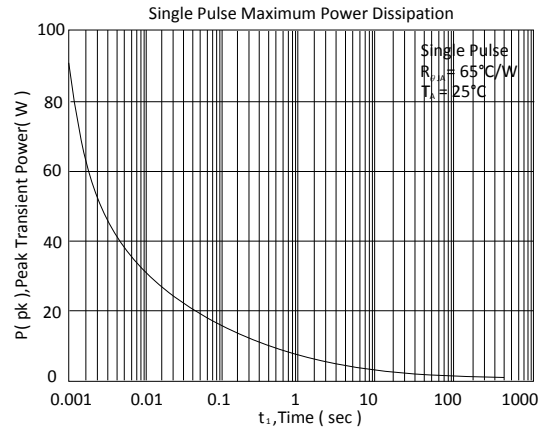
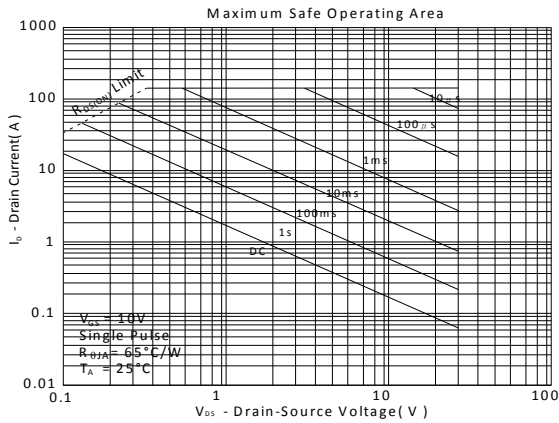
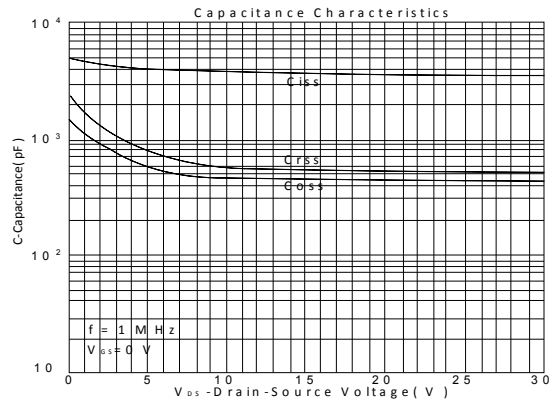
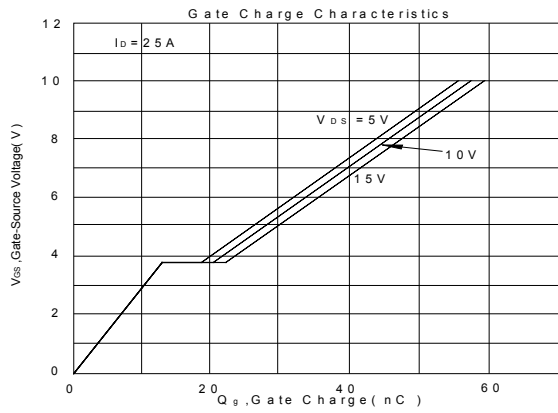




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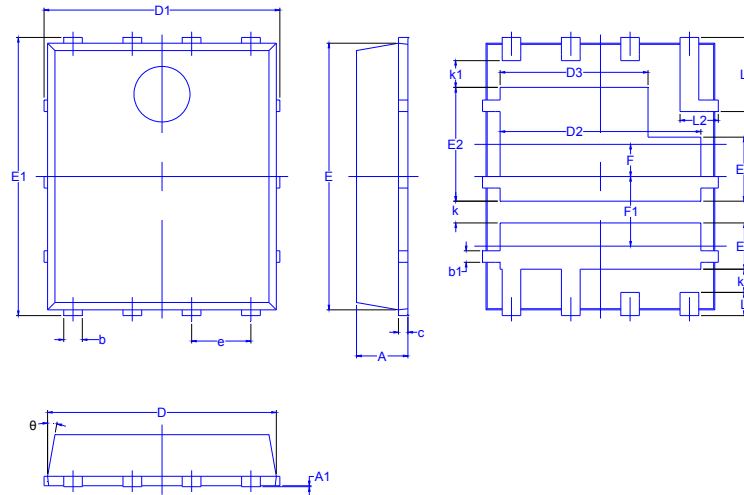








Outline Drawing



Dimension in mm

Dimension	A	A1	b	b1	c	D	D1	D2	D3	E	E1	E2	E3	E4	e	
Min.	1.00	0.00	0.30	0.15	0.15	4.80	5.05BSC	4.15	3.02	5.65	6.00BSC	2.3	0.85	1.23	1.27BSC	
Typ.																
Max.	1.20	0.05	0.50	0.35	0.25	5.00			4.45	3.32		5.85		2.60		1.15

Dimension	L	L1	L2	k	k1	k2	F	F1	θ
Min.	0.40	1.50	0.72	0.47BSC	0.58BSC	0.50BSC	0.695REF	1.50REF	10° REF
Typ.									
Max.	0.60	1.70	0.92						

Recommended minimum pads

