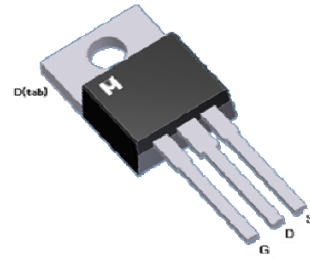
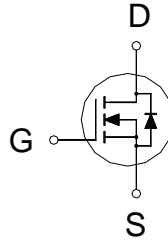


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	100V
$R_{DS(on)}$ (MAX.)	11.5m Ω
I_D	95A



UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 30	V
Continuous Drain Current	$T_C = 25\text{ }^\circ\text{C}$	I_D	95	A
	$T_C = 100\text{ }^\circ\text{C}$		67	
Pulsed Drain Current ¹		I_{DM}	280	
Avalanche Current		I_{AS}	90	
Avalanche Energy	$L = 0.1\text{mH}, I_D=90\text{A}, R_G=25\Omega$	E_{AS}	405	mJ
Repetitive Avalanche Energy ²	$L = 0.05\text{mH}$	E_{AR}	202	
Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	P_D	166	W
	$T_C = 100\text{ }^\circ\text{C}$		66	
Operating Junction & Storage Temperature Range		T_{j}, T_{stg}	-55 to 150	$^\circ\text{C}$

100% UIS testing in condition of $V_D=50\text{V}, L=0.1\text{mH}, V_G=10\text{V}, I_L=60\text{A}$, Rated $V_{DS}=100\text{V}$ N-CH

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		0.75	$^\circ\text{C} / \text{W}$
Junction-to-Ambient	$R_{\theta JA}$		62.5	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	100			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	2.0	3.0	4.0	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±30V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 80V, V _{GS} = 0V			1	μA
		V _{DS} = 70V, V _{GS} = 0V, T _J = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	95			A
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = 10V, I _D = 32A		9.7	11.5	mΩ
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 32A		48		S
DYNAMIC						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = 50V, f = 1MHz		3226		pF
Output Capacitance	C _{oss}			252		
Reverse Transfer Capacitance	C _{rss}			29		
Gate Resistance	R _g	V _{GS} = 15mV, V _{DS} = 0V, f = 1MHz		1.7		Ω
Total Gate Charge ^{1,2}	Q _g	V _{DS} = 50V, V _{GS} = 10V, I _D = 32A		39		nC
Gate-Source Charge ^{1,2}	Q _{gs}			20		
Gate-Drain Charge ^{1,2}	Q _{gd}			8.2		
Turn-On Delay Time ^{1,2}	t _{d(on)}	V _{DS} = 50V, I _D = 1A, V _{GS} = 10V, R _{GS} = 6Ω		30		nS
Rise Time ^{1,2}	t _r			150		
Turn-Off Delay Time ^{1,2}	t _{d(off)}			110		
Fall Time ^{1,2}	t _f			180		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I _S				95	A
Pulsed Current ³	I _{SM}				280	
Forward Voltage ¹	V _{SD}	I _F = 32A, V _{GS} = 0V			1.3	V
Reverse Recovery Time	t _{rr}	I _F = 20A, dI _F /dt = 100A / μS		120		nS
Reverse Recovery Charge	Q _{rr}				420	

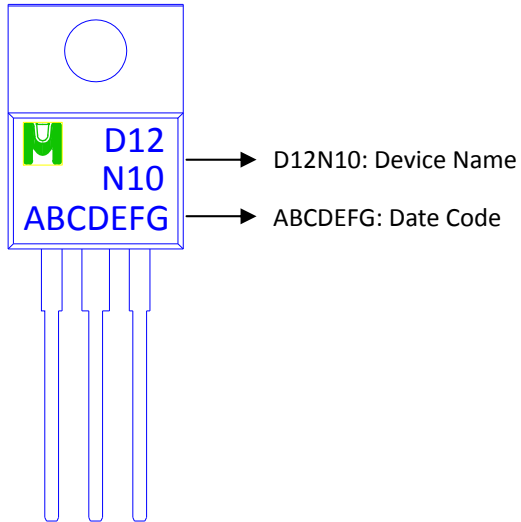
¹Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

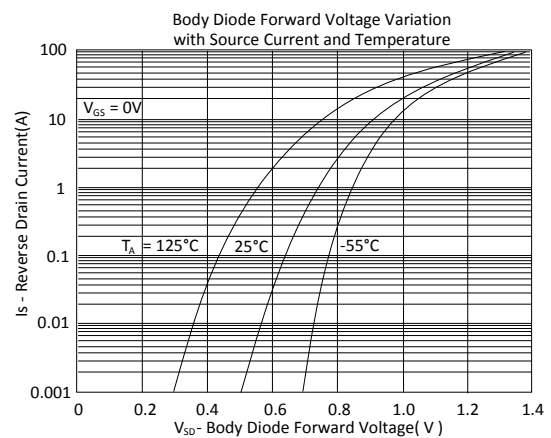
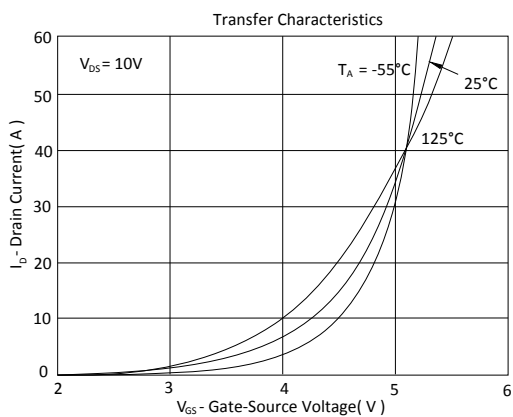
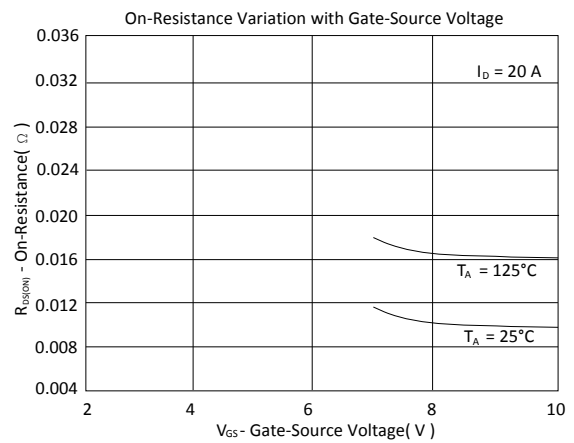
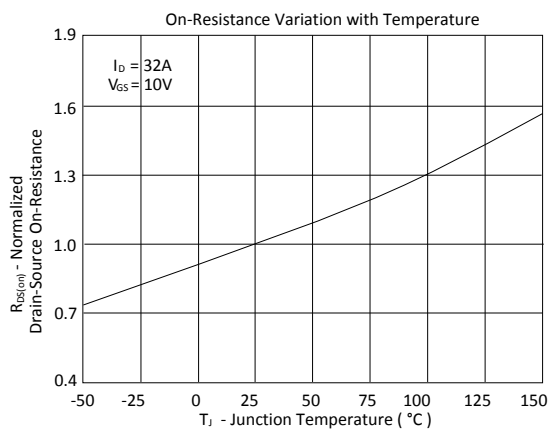
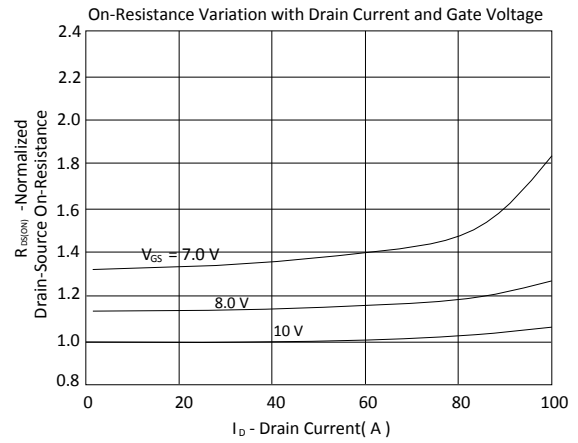
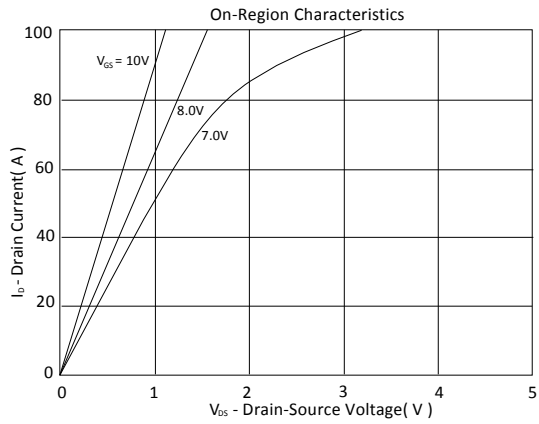
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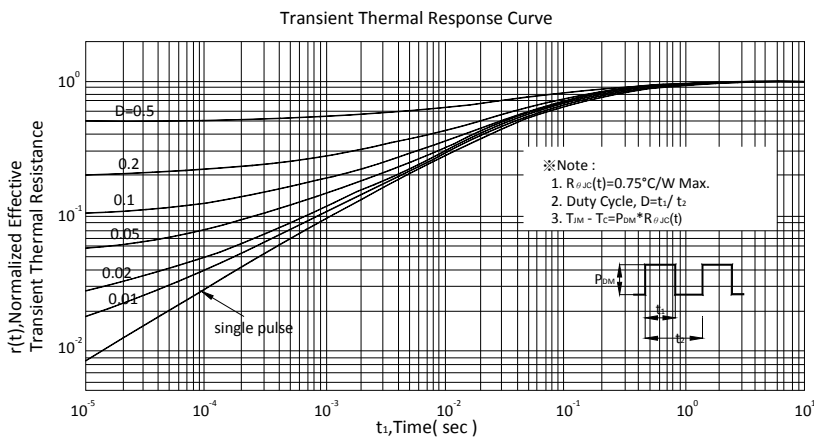
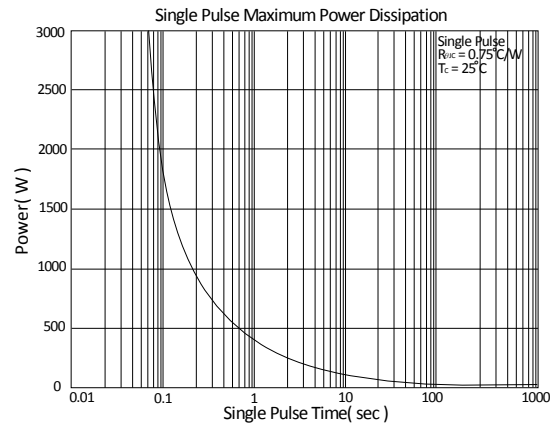
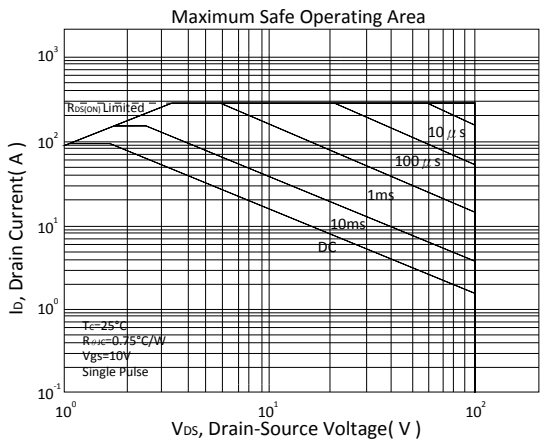
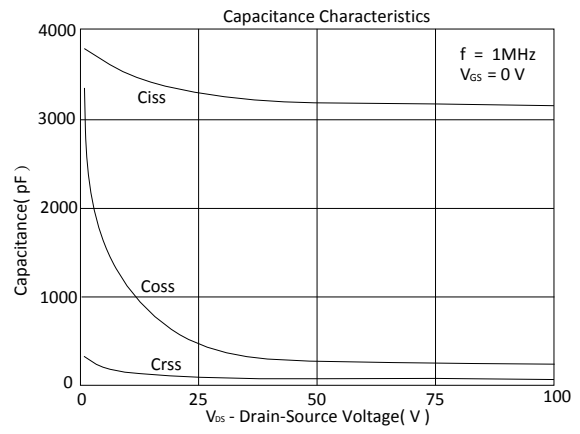
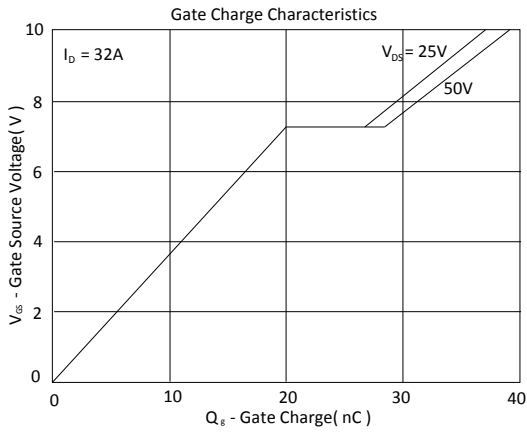
Device Name: EMD12N10E for TO-220





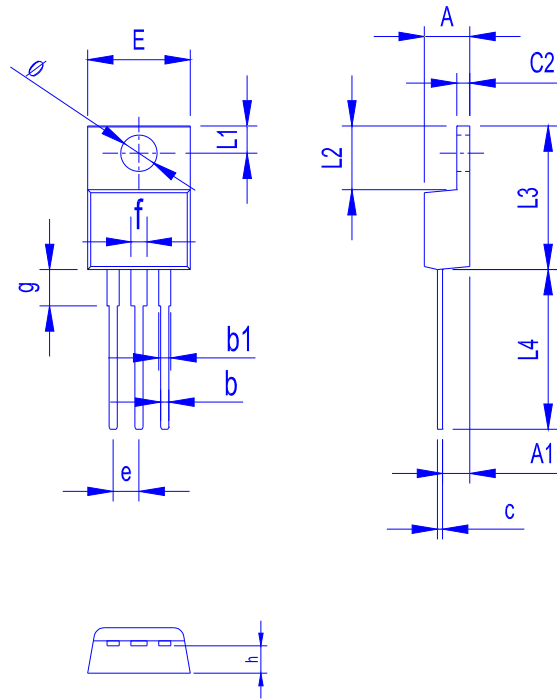
TYPICAL CHARACTERISTICS







Outline Drawing



Dimension in mm

Dimension	A	b	b1	c	c2	E	L1	L2	L3	L4	ø	e	f	g	h
Min.	4.20	0.70	0.90	0.30	1.10	9.80	2.55	6.10	14.80	13.50	3.40	2.35	1.30	3.40	2.40
Max.	4.80	1.10	1.50	0.70	1.50	10.50	2.85	6.50	15.40	14.50	3.80	2.75	1.90	3.80	3.00