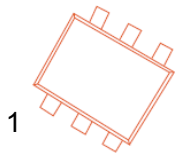
digital transistor (NPN+NPN)

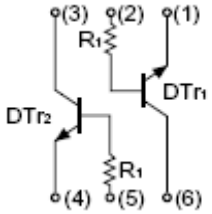
SOT-563



FEATURES

- Two DTC114T chips in a package
- Transistor elements are independent, eliminating interference
- Mounting cost and area can be cut in half.

External circuit



MARKING: H4

Absolute maximum ratings (Ta=25℃)

Parameter	Symbol	Limits	Unit
Collector-base voltage	$V_{(BR)CBO}$	50	V
Collector-emitter voltage	$V_{(BR)CEO}$	50	V
Emitter-base voltage	$V_{(BR)EBO}$	5	V
Collector current	I_C	100	mA
Collector Power dissipation	P_C	150	mW
Junction temperature	Tj	150	℃
Storage temperature	Tstg	-55~150	℃

Electrical characteristics (Ta=25℃)

Parameter	Symbol	Min.	Typ	Max.	Unit	Conditions
Collector-base breakdown voltage	$V_{(BR)CBO}$	50			V	I_C=50μA
Collector-emitter breakdown voltage	$V_{(BR)CEO}$	50			V	I_C=1mA
Emitter-base breakdown voltage	$V_{(BR)EBO}$	5			V	I_E=50μA
Collector cut-off current	I_{CBO}			0.5	μA	V_{CB}=50V
Emitter cut-off current	I_{EBO}			0.5	μA	V_{EB}=4V
Collector-emitter saturation voltage	$V_{CE(sat)}$			0.3	V	I_C=10mA,I_B=1mA
DC current transfer ratio	h_{FE}	100		600		V_{CE}=5V,I_C=1mA
Input resistance	R_1	7	10	13	KΩ	
Transition frequency	f_T		250		MHz	V_{CE}=10V ,I_E=-5mA,f=100MHz