EN29GL064AT/B
64 Megabit (8192K x 8-bit / 4096K x 16-bit) Flash Memory
Page mode Flash Memory, CMOS 3.0 Volt-only

FEATURES

- Single power supply operation
- Full voltage range: 2.7 to 3.6 volts read and write operations
- High performance
- Access times as fast as 70 ns
- 8-word/16-byte page read buffer
- 16-word/32-byte write buffer reduces overall programming time for multiple-word updates
- Secured Silicon Sector region
- 128-word/256-byte sector for permanent, secure identification through an 8-word/16-byte random Electronic Serial Number
- Can be programmed and locked at the factory or by the customer
- Flexible Sector Architecture:
- Boot sector models:
  Eight 8-Kbyte boot sectors on Top or Bottom and one hundred twenty-seven 32Kword / 64Kbyte sectors.
- Suspend and Resume commands for Program and Erase operations
- Write operation status bits indicate program and erase operation completion
- Support for CFI (Common Flash Interface)
- Persistent methods of Advanced Sector Protection
- WP#/ACC input
- Accelerates programming time (when V_{HH} is applied) for greater throughput during system production
- Protects first or last sector regardless of sector protection settings
- Hardware reset input (RESET#) resets device
- Ready/Busy# output (RY/BY#) detects program or erase cycle completion
- Minimum 100K program/erase endurance cycles.
- Package Options
- 48-pin TSOP (Type 1)
- 48 ball 6mm x 8mm TFBGA
- Industrial Temperature Range.

GENERAL DESCRIPTION

The EN29GL064AT/B offers a fast page access time of 25 ns with a corresponding random access time as fast as 70 ns. It features a Write Buffer that allows a maximum of 16 words/32 bytes to be programmed in one operation, resulting in faster effective programming time than standard programming algorithms. This makes the device ideal for today's embedded applications that require higher density, better performance and lower power consumption.

CONNECTION DIAGRAMS

Figure 1. 48-pin Standard TSOP (Top View)

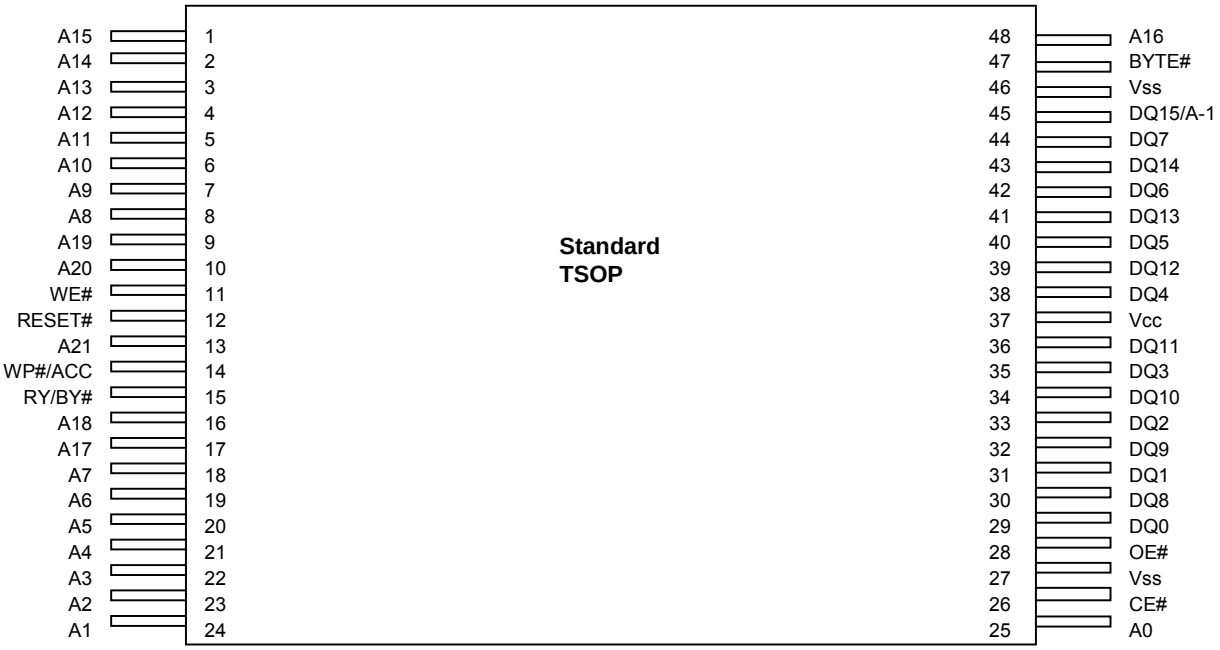


Figure 2. 48-Ball TFBGA (Top View, Balls Facing Down)

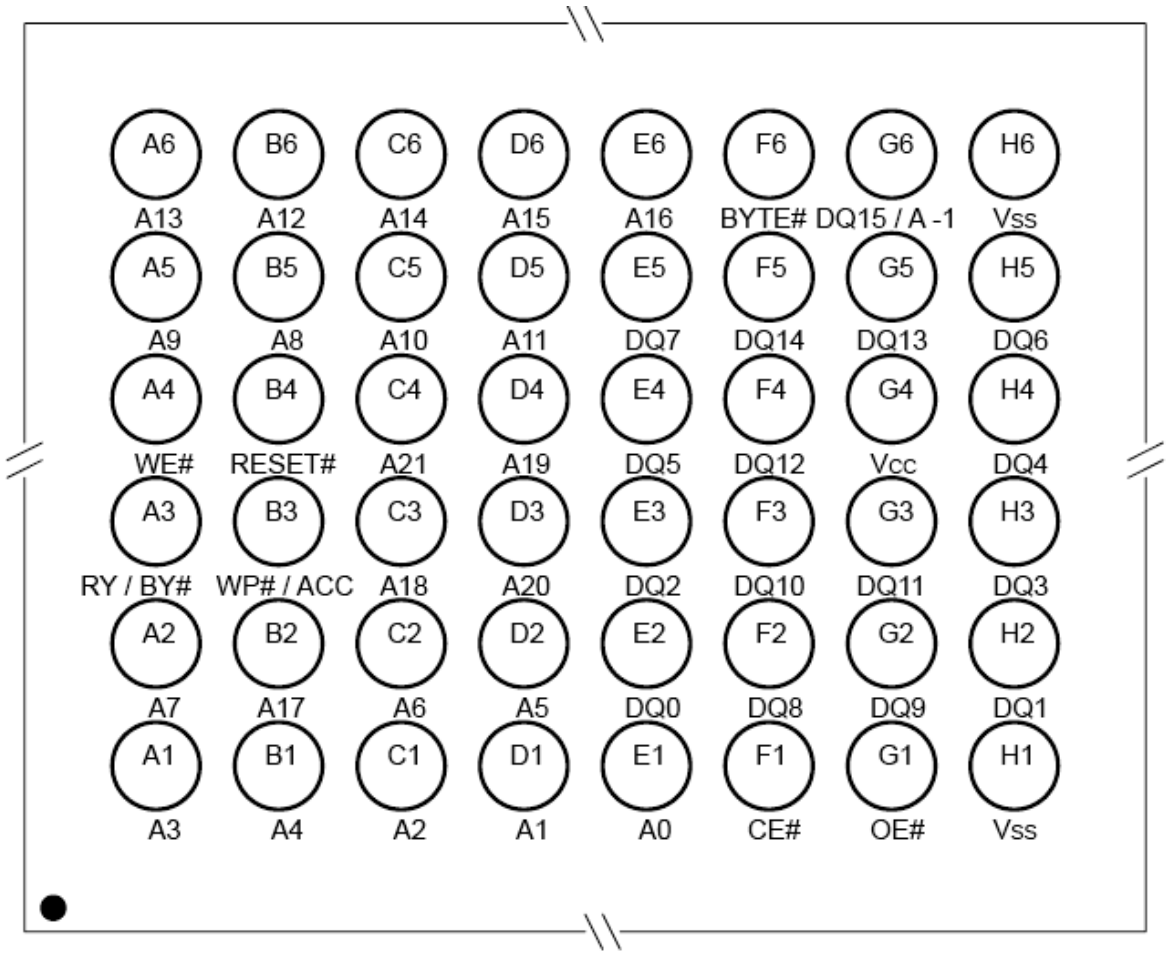


TABLE 1. PIN DESCRIPTION

Pin Name	Function
A21–A0	A21–A0
DQ0-DQ14	Data input/output.
DQ15 / A-1	DQ15 (data input/output, word mode), A-1 (LSB address input, byte mode)
CE#	Chip Enable
OE#	Output Enable
RESET#	Hardware Reset Pin
RY/BY#	Ready/Busy Output
WE#	Write Enable
Vcc	Supply Voltage (2.7-3.6V)
Vss	Ground
BYTE#	Byte/Word mode selection
WP#/ACC	Write Protect / Acceleration Pin (WP# has an internal pull-up; when unconnected, WP# is at V_{IH}.)
RFU	Reserved for future use. Not Connected to anything

FIGURE 3. LOGIC DIAGRAM

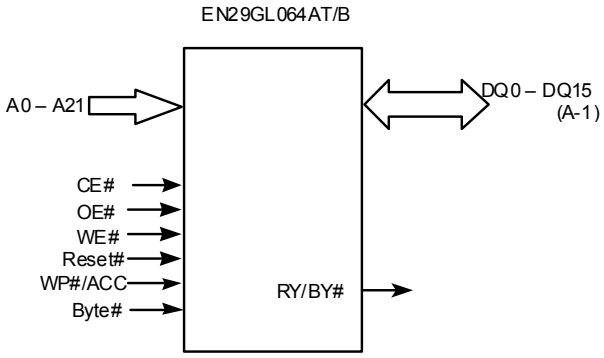
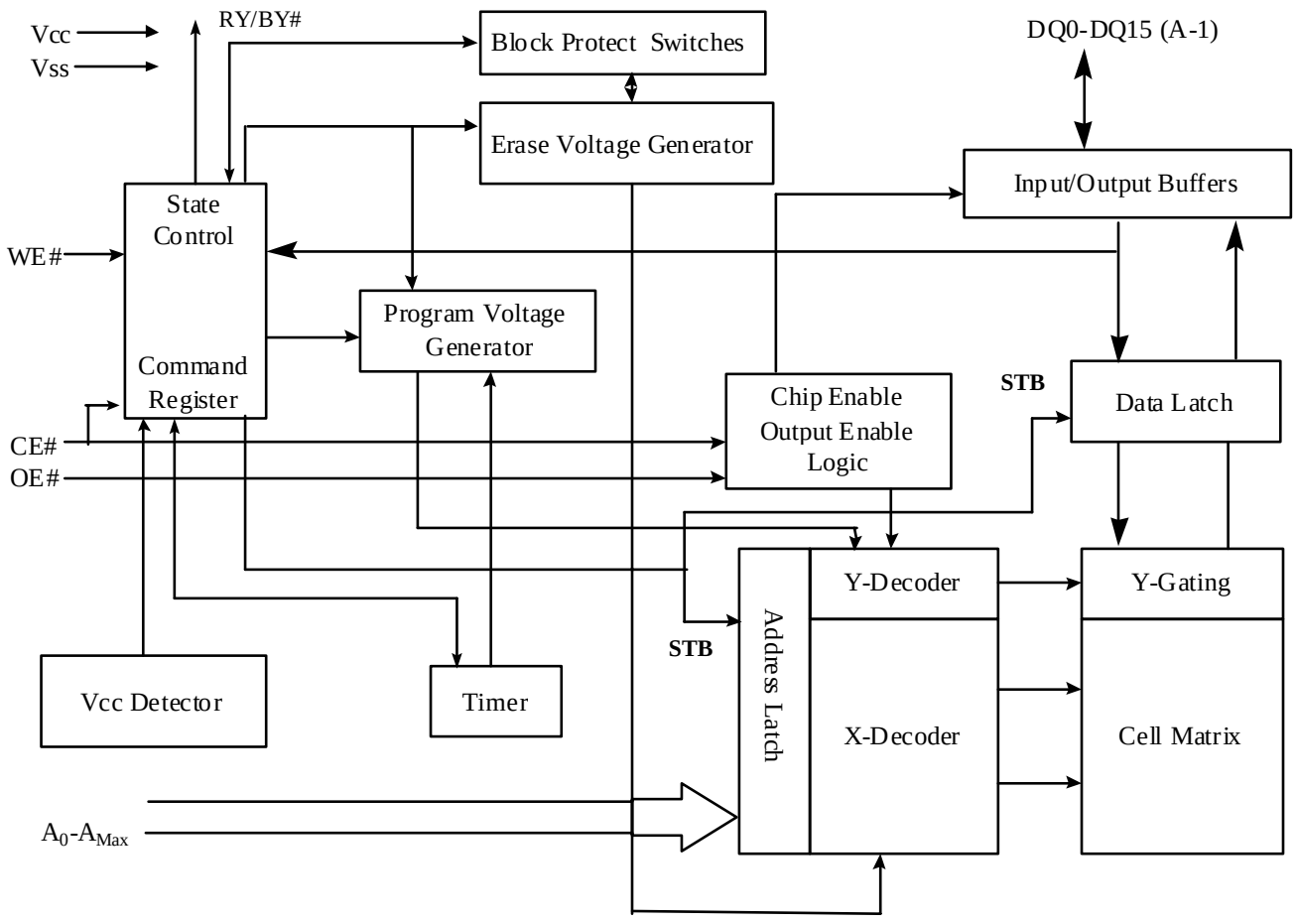


Table 2. PRODUCT SELECTOR GUIDE

Product Number		EN29GL064AT/B
Speed Option	Full Voltage Range: Vcc=2.7 – 3.6 V	-70
Max Access Time, ns (t_{acc})		70
Max Page Read Access, ns(t_{pacc})		25
Max CE# Access, ns (t_{ce})		70
Max OE# Access, ns (t_{oe})		25

BLOCK DIAGRAM



Product Overview

EN29GL064AT/B is 64 Mb, 3.0-volt-only, page mode Flash devices optimized for today's embedded designs that demand a large storage array and rich functionality. The feature of V I/O control allowing control and I/O signals to operate from 1.65 V to V_{CC}. Additional features include:

- Single word programming or a 16-word buffer for an increased programming speed
- Program Suspend/Resume and Erase Suspend/Resume
- Advanced Sector Protection methods for protecting sectors as required
- 128 words/256 bytes of Secured Silicon area for storing customer and factory secured information. The Secured Silicon Sector is One Time Programmable.

Table 3A. Top Boot Sector / Persistent Protection Sector Group Address Tables (EN29GL064AT)

PPB Group	Sector	A21 – A12	Sector Size (Kbytes / Kwords)	Address Range (h) Byte mode (x8)	Address Range (h) Word Mode (x16)
PPB 0	SA0	0000000xxx	64/32	000000–00FFFF	000000–007FFF
	SA1	0000001xxx	64/32	010000–01FFFF	008000–00FFFF
	SA2	0000010xxx	64/32	020000–02FFFF	010000–017FFF
	SA3	0000011xxx	64/32	030000–03FFFF	018000–01FFFF
PPB 1	SA4	0000100xxx	64/32	040000–04FFFF	020000–027FFF
	SA5	0000101xxx	64/32	050000–05FFFF	028000–02FFFF
	SA6	0000110xxx	64/32	060000–06FFFF	030000–037FFF
	SA7	0000111xxx	64/32	070000–07FFFF	038000–03FFFF
PPB 2	SA8	0001000xxx	64/32	080000–08FFFF	040000–047FFF
	SA9	0001001xxx	64/32	090000–09FFFF	048000–04FFFF
	SA10	0001010xxx	64/32	0A0000–0AFFFF	050000–057FFF
	SA11	0001011xxx	64/32	0B0000–0BFFFF	058000–05FFFF
PPB 3	SA12	0001100xxx	64/32	0C0000–0CFFFF	060000–067FFF
	SA13	0001101xxx	64/32	0D0000–0DFFFF	068000–06FFFF
	SA14	0001110xxx	64/32	0E0000–0EFFFF	070000–077FFF
	SA15	0001111xxx	64/32	0F0000–0FFFFF	078000–07FFFF
PPB 4	SA16	0010000xxx	64/32	100000–10FFFF	080000–087FFF
	SA17	0010001xxx	64/32	110000–11FFFF	088000–08FFFF
	SA18	0010010xxx	64/32	120000–12FFFF	090000–097FFF
	SA19	0010011xxx	64/32	130000–13FFFF	098000–09FFFF
PPB 5	SA20	0010100xxx	64/32	140000–14FFFF	0A0000–0A7FFF
	SA21	0010101xxx	64/32	150000–15FFFF	0A8000–0AFFFF
	SA22	0010110xxx	64/32	160000–16FFFF	0B0000–0B7FFF
	SA23	0010111xxx	64/32	170000–17FFFF	0B8000–0BFFFF
PPB 6	SA24	0011000xxx	64/32	180000–18FFFF	0C0000–0C7FFF
	SA25	0011001xxx	64/32	190000–19FFFF	0C8000–0CFFFF
	SA26	0011010xxx	64/32	1A0000–1AFFFF	0D0000–0D7FFF
	SA27	0011011xxx	64/32	1B0000–1BFFFF	0D8000–0DFFFF
PPB 7	SA28	0011100xxx	64/32	1C0000–1CFFFF	0E0000–0E7FFF
	SA29	0011101xxx	64/32	1D0000–1DFFFF	0E8000–0EFFFF
	SA30	0011110xxx	64/32	1E0000–1EFFFF	0F0000–0F7FFF
	SA31	0011111xxx	64/32	1F0000–1FFFFF	0F8000–0FFFFF
PPB 8	SA32	0100000xxx	64/32	200000–20FFFF	100000–107FFF
	SA33	0100001xxx	64/32	210000–21FFFF	108000–10FFFF
	SA34	0100010xxx	64/32	220000–22FFFF	110000–117FFF
	SA35	0100011xxx	64/32	230000–23FFFF	118000–11FFFF
PPB 9	SA36	0100100xxx	64/32	240000–24FFFF	120000–127FFF
	SA37	0100101xxx	64/32	250000–25FFFF	128000–12FFFF
	SA38	0100110xxx	64/32	260000–26FFFF	130000–137FFF

	SA39	0100111xxx	64/32	270000–27FFFF	138000–13FFFF
PPB 10	SA40	0101000xxx	64/32	280000–28FFFF	140000–147FFF
	SA41	0101001xxx	64/32	290000–29FFFF	148000–14FFFF
	SA42	0101010xxx	64/32	2A0000–2AFFFF	150000–157FFF
	SA43	0101011xxx	64/32	2B0000–2BFFFF	158000–15FFFF
PPB 11	SA44	0101100xxx	64/32	2C0000–2CFFFF	160000–167FFF
	SA45	0101101xxx	64/32	2D0000–2DFFFF	168000–16FFFF
	SA46	0101110xxx	64/32	2E0000–2EFFFF	170000–177FFF
	SA47	0101111xxx	64/32	2F0000–2FFFFF	178000–17FFFF
PPB 12	SA48	0110000xxx	64/32	300000–30FFFF	180000–187FFF
	SA49	0110001xxx	64/32	310000–31FFFF	188000–18FFFF
	SA50	0110010xxx	64/32	320000–32FFFF	190000–197FFF
	SA51	0110011xxx	64/32	330000–33FFFF	198000–19FFFF
PPB 13	SA52	0110100xxx	64/32	340000–34FFFF	1A0000–1A7FFF
	SA53	0110101xxx	64/32	350000–35FFFF	1A8000–1AFFFF
	SA54	0110110xxx	64/32	360000–36FFFF	1B0000–1B7FFF
	SA55	0110111xxx	64/32	370000–37FFFF	1B8000–1BFFFF
PPB 14	SA56	0111000xxx	64/32	380000–38FFFF	1C0000–1C7FFF
	SA57	0111001xxx	64/32	390000–39FFFF	1C8000–1CFFFF
	SA58	0111010xxx	64/32	3A0000–3AFFFF	1D0000–1D7FFF
	SA59	0111011xxx	64/32	3B0000–3BFFFF	1D8000–1DFFFF
PPB 15	SA60	0111100xxx	64/32	3C0000–3CFFFF	1E0000–1E7FFF
	SA61	0111101xxx	64/32	3D0000–3DFFFF	1E8000–1EFFFF
	SA62	0111110xxx	64/32	3E0000–3EFFFF	1F0000–1F7FFF
	SA63	0111111xxx	64/32	3F0000–3FFFFF	1F8000–1FFFFF
PPB 16	SA64	1000000xxx	64/32	400000–40FFFF	200000–207FFF
	SA65	1000001xxx	64/32	410000–41FFFF	208000–20FFFF
	SA66	1000010xxx	64/32	420000–42FFFF	210000–217FFF
	SA67	1000011xxx	64/32	430000–43FFFF	218000–21FFFF
PPB 17	SA68	1000100xxx	64/32	440000–44FFFF	220000–227FFF
	SA69	1000101xxx	64/32	450000–45FFFF	228000–22FFFF
	SA70	1000110xxx	64/32	460000–46FFFF	230000–237FFF
	SA71	1000111xxx	64/32	470000–47FFFF	238000–23FFFF
PPB 18	SA72	1001000xxx	64/32	480000–48FFFF	240000–247FFF
	SA73	1001001xxx	64/32	490000–49FFFF	248000–24FFFF
	SA74	1001010xxx	64/32	4A0000–4AFFFF	250000–257FFF
	SA75	1001011xxx	64/32	4B0000–4BFFFF	258000–25FFFF
PPB 19	SA76	1001100xxx	64/32	4C0000–4CFFFF	260000–267FFF
	SA77	1001101xxx	64/32	4D0000–4DFFFF	268000–26FFFF
	SA78	1001110xxx	64/32	4E0000–4EFFFF	270000–277FFF
	SA79	1001111xxx	64/32	4F0000–4FFFFF	278000–27FFFF
PPB 20	SA80	1010000xxx	64/32	500000–50FFFF	280000–287FFF
	SA81	1010001xxx	64/32	510000–51FFFF	288000–28FFFF

	SA82	1010010xxx	64/32	520000–52FFFF	290000–297FFF
	SA83	1010011xxx	64/32	530000–53FFFF	298000–29FFFF
PPB 21	SA84	1010100xxx	64/32	540000–54FFFF	2A0000–2A7FFF
	SA85	1010101xxx	64/32	550000–55FFFF	2A8000–2AFFFF
	SA86	1010110xxx	64/32	560000–56FFFF	2B0000–2B7FFF
	SA87	1010111xxx	64/32	570000–57FFFF	2B8000–2BFFFF
PPB 22	SA88	1011000xxx	64/32	580000–58FFFF	2C0000–2C7FFF
	SA89	1011001xxx	64/32	590000–59FFFF	2C8000–2CFFFF
	SA90	1011010xxx	64/32	5A0000–5AFFFF	2D0000–2D7FFF
	SA91	1011011xxx	64/32	5B0000–5BFFFF	2D8000–2DFFFF
PPB 23	SA92	1011100xxx	64/32	5C0000–5CFFFF	2E0000–2E7FFF
	SA93	1011101xxx	64/32	5D0000–5DFFFF	2E8000–2EFFFF
	SA94	1011110xxx	64/32	5E0000–5EFFFF	2F0000–2F7FFF
	SA95	1011111xxx	64/32	5F0000–5FFFFF	2F8000–2FFFFF
PPB 24	SA96	1100000xxx	64/32	600000–60FFFF	300000–307FFF
	SA97	1100001xxx	64/32	610000–61FFFF	308000–30FFFF
	SA98	1100010xxx	64/32	620000–62FFFF	310000–317FFF
	SA99	1100011xxx	64/32	630000–63FFFF	318000–31FFFF
PPB 25	SA100	1100100xxx	64/32	640000–64FFFF	320000–327FFF
	SA101	1100101xxx	64/32	650000–65FFFF	328000–32FFFF
	SA102	1100110xxx	64/32	660000–66FFFF	330000–337FFF
	SA103	1100111xxx	64/32	670000–67FFFF	338000–33FFFF
PPB 26	SA104	1101000xxx	64/32	680000–68FFFF	340000–347FFF
	SA105	1101001xxx	64/32	690000–69FFFF	348000–34FFFF
	SA106	1101010xxx	64/32	6A0000–6AFFFF	350000–357FFF
	SA107	1101011xxx	64/32	6B0000–6BFFFF	358000–35FFFF
PPB 27	SA108	1101100xxx	64/32	6C0000–6CFFFF	360000–367FFF
	SA109	1101101xxx	64/32	6D0000–6DFFFF	368000–36FFFF
	SA110	1101110xxx	64/32	6E0000–6EFFFF	370000–377FFF
	SA111	1101111xxx	64/32	6F0000–6FFFFF	378000–37FFFF
PPB 28	SA112	1110000xxx	64/32	700000–70FFFF	380000–387FFF
	SA113	1110001xxx	64/32	710000–71FFFF	388000–38FFFF
	SA114	1110010xxx	64/32	720000–72FFFF	390000–397FFF
	SA115	1110011xxx	64/32	730000–73FFFF	398000–39FFFF
PPB 29	SA116	1110100xxx	64/32	740000–74FFFF	3A0000–3A7FFF
	SA117	1110101xxx	64/32	750000–75FFFF	3A8000–3AFFFF
	SA118	1110110xxx	64/32	760000–76FFFF	3B0000–3B7FFF
	SA119	1110111xxx	64/32	770000–77FFFF	3B8000–3BFFFF
PPB 30	SA120	1111000xxx	64/32	780000–78FFFF	3C0000–3C7FFF
	SA121	1111001xxx	64/32	790000–79FFFF	3C8000–3CFFFF
	SA122	1111010xxx	64/32	7A0000–7AFFFF	3D0000–3D7FFF
	SA123	1111011xxx	64/32	7B0000–7BFFFF	3D8000–3DFFFF
PPB 31	SA124	1111100xxx	64/32	7C0000–7CFFFF	3E0000–3E7FFF

PPB 32	SA125	1111101xxx	64/32	7D0000–7DFFFF	3E8000–3EFFFF
PPB 33	SA126	1111110xxx	64/32	7E0000–7EFFFF	3F0000–3F7FFF
PPB 34	SA127	1111111000	8/4	7F0000–7F1FFF	3F8000–3F8FFF
PPB 35	SA128	1111111001	8/4	7F2000–7F3FFF	3F9000–3F9FFF
PPB 36	SA129	1111111010	8/4	7F4000–7F5FFF	3FA000–3FAFFF
PPB 37	SA130	1111111011	8/4	7F6000–7F7FFF	3FB000–3FBFFF
PPB 38	SA131	1111111100	8/4	7F8000–7F9FFF	3FC000–3FCFFF
PPB 39	SA132	1111111101	8/4	7FA000–7FBFFF	3FD000–3FDFFF
PPB 40	SA133	1111111110	8/4	7FC000–7FDFFF	3FE000–3FEFFF
PPB 41	SA134	1111111111	8/4	7FE000–7FFFFF	3FF000–3FFFFF

Table 3B. Bottom Boot Sector / Persistent Protection Sector Group Address Tables (EN29GL064AB)

PPB Group	Sector	A21 – A12	Sector Size (Kbytes / Kwords)	Address Range (h) Byte mode (x8)	Address Range (h) Word Mode (x16)
PPB 0	SA0	0000000000	8/4	000000–001FFF	000000–000FFF
PPB 1	SA1	0000000001	8/4	002000–003FFF	001000–001FFF
PPB 2	SA2	0000000010	8/4	004000–005FFF	002000–002FFF
PPB 3	SA3	0000000011	8/4	006000–007FFF	003000–003FFF
PPB 4	SA4	0000000100	8/4	008000–009FFF	004000–004FFF
PPB 5	SA5	0000000101	8/4	00A000–00BFFF	005000–005FFF
PPB 6	SA6	0000000110	8/4	00C000–00DFFF	006000–006FFF
PPB 7	SA7	0000000111	8/4	00E000–00FFFF	007000–007FFF
PPB 8	SA8	0000001xxx	64/32	010000–01FFFF	008000–00FFFF
PPB 9	SA9	0000010xxx	64/32	020000–02FFFF	010000–017FFF
PPB 10	SA10	0000011xxx	64/32	030000–03FFFF	018000–01FFFF
PPB 11	SA11	0000100xxx	64/32	040000–04FFFF	020000–027FFF
	SA12	0000101xxx	64/32	050000–05FFFF	028000–02FFFF
	SA13	0000110xxx	64/32	060000–06FFFF	030000–037FFF
	SA14	0000111xxx	64/32	070000–07FFFF	038000–03FFFF
PPB 12	SA15	0001000xxx	64/32	080000–08FFFF	040000–047FFF
	SA16	0001001xxx	64/32	090000–09FFFF	048000–04FFFF
	SA17	0001010xxx	64/32	0A0000–0AFFFF	050000–057FFF
	SA18	0001011xxx	64/32	0B0000–0BFFFF	058000–05FFFF
PPB 13	SA19	0001100xxx	64/32	0C0000–0CFFFF	060000–067FFF
	SA20	0001101xxx	64/32	0D0000–0DFFFF	068000–06FFFF
	SA21	0001110xxx	64/32	0E0000–0EFFFF	070000–077FFF
	SA22	0001111xxx	64/32	0F0000–0FFFFF	078000–07FFFF
PPB 14	SA23	0010000xxx	64/32	100000–10FFFF	080000–087FFF
	SA24	0010001xxx	64/32	110000–11FFFF	088000–08FFFF
	SA25	0010010xxx	64/32	120000–12FFFF	090000–097FFF
	SA26	0010011xxx	64/32	130000–13FFFF	098000–09FFFF
PPB 15	SA27	0010100xxx	64/32	140000–14FFFF	0A0000–0A7FFF
	SA28	0010101xxx	64/32	150000–15FFFF	0A8000–0AFFFF

	SA29	0010110xxx	64/32	160000–16FFFF	0B0000–0B7FFF
	SA30	0010111xxx	64/32	170000–17FFFF	0B8000–0BFFFF
PPB 16	SA31	0011000xxx	64/32	180000–18FFFF	0C0000–0C7FFF
	SA32	0011001xxx	64/32	190000–19FFFF	0C8000–0CFFFF
	SA33	0011010xxx	64/32	1A0000–1AFFFF	0D0000–0D7FFF
	SA34	0011011xxx	64/32	1B0000–1BFFFF	0D8000–0DFFFF
PPB 17	SA35	0011100xxx	64/32	1C0000–1CFFFF	0E0000–0E7FFF
	SA36	0011101xxx	64/32	1D0000–1DFFFF	0E8000–0EFFFF
	SA37	0011110xxx	64/32	1E0000–1EFFFF	0F0000–0F7FFF
	SA38	0011111xxx	64/32	1F0000–1FFFFF	0F8000–0FFFFF
PPB 18	SA39	0100000xxx	64/32	200000–20FFFF	100000–107FFF
	SA40	0100001xxx	64/32	210000–21FFFF	108000–10FFFF
	SA41	0100010xxx	64/32	220000–22FFFF	110000–117FFF
	SA42	0100011xxx	64/32	230000–23FFFF	118000–11FFFF
PPB 19	SA43	0100100xxx	64/32	240000–24FFFF	120000–127FFF
	SA44	0100101xxx	64/32	250000–25FFFF	128000–12FFFF
	SA45	0100110xxx	64/32	260000–26FFFF	130000–137FFF
	SA46	0100111xxx	64/32	270000–27FFFF	138000–13FFFF
PPB 20	SA47	0101000xxx	64/32	280000–28FFFF	140000–147FFF
	SA48	0101001xxx	64/32	290000–29FFFF	148000–14FFFF
	SA49	0101010xxx	64/32	2A0000–2AFFFF	150000–157FFF
	SA50	0101011xxx	64/32	2B0000–2BFFFF	158000–15FFFF
PPB 21	SA51	0101100xxx	64/32	2C0000–2CFFFF	160000–167FFF
	SA52	0101101xxx	64/32	2D0000–2DFFFF	168000–16FFFF
	SA53	0101110xxx	64/32	2E0000–2EFFFF	170000–177FFF
	SA54	0101111xxx	64/32	2F0000–2FFFFF	178000–17FFFF
PPB 22	SA55	0110000xxx	64/32	300000–30FFFF	180000–187FFF
	SA56	0110001xxx	64/32	310000–31FFFF	188000–18FFFF
	SA57	0110010xxx	64/32	320000–32FFFF	190000–197FFF
	SA58	0110011xxx	64/32	330000–33FFFF	198000–19FFFF
PPB 23	SA59	0110100xxx	64/32	340000–34FFFF	1A0000–1A7FFF
	SA60	0110101xxx	64/32	350000–35FFFF	1A8000–1AFFFF
	SA61	0110110xxx	64/32	360000–36FFFF	1B0000–1B7FFF
	SA62	0110111xxx	64/32	370000–37FFFF	1B8000–1BFFFF
PPB 24	SA63	0111000xxx	64/32	380000–38FFFF	1C0000–1C7FFF
	SA64	0111001xxx	64/32	390000–39FFFF	1C8000–1CFFFF
	SA65	0111010xxx	64/32	3A0000–3AFFFF	1D0000–1D7FFF
	SA66	0111011xxx	64/32	3B0000–3BFFFF	1D8000–1DFFFF
PPB 25	SA67	0111100xxx	64/32	3C0000–3CFFFF	1E0000–1E7FFF
	SA68	0111101xxx	64/32	3D0000–3DFFFF	1E8000–1EFFFF
	SA69	0111110xxx	64/32	3E0000–3EFFFF	1F0000–1F7FFF
	SA70	0111111xxx	64/32	3F0000–3FFFFF	1F8000–1FFFFF
PPB 26	SA71	1000000xxx	64/32	400000–40FFFF	200000–207FFF

	SA72	1000001xxx	64/32	410000–41FFFF	208000–20FFFF
	SA73	1000010xxx	64/32	420000–42FFFF	210000–217FFF
	SA74	1000011xxx	64/32	430000–43FFFF	218000–21FFFF
PPB 27	SA75	1000100xxx	64/32	440000–44FFFF	220000–227FFF
	SA76	1000101xxx	64/32	450000–45FFFF	228000–22FFFF
	SA77	1000110xxx	64/32	460000–46FFFF	230000–237FFF
	SA78	1000111xxx	64/32	470000–47FFFF	238000–23FFFF
PPB 28	SA79	1001000xxx	64/32	480000–48FFFF	240000–247FFF
	SA80	1001001xxx	64/32	490000–49FFFF	248000–24FFFF
	SA81	1001010xxx	64/32	4A0000–4AFFFF	250000–257FFF
	SA82	1001011xxx	64/32	4B0000–4BFFFF	258000–25FFFF
PPB 29	SA83	1001100xxx	64/32	4C0000–4CFFFF	260000–267FFF
	SA84	1001101xxx	64/32	4D0000–4DFFFF	268000–26FFFF
	SA85	1001110xxx	64/32	4E0000–4EFFFF	270000–277FFF
	SA86	1001111xxx	64/32	4F0000–4FFFFF	278000–27FFFF
PPB 30	SA87	1010000xxx	64/32	500000–50FFFF	280000–287FFF
	SA88	1010001xxx	64/32	510000–51FFFF	288000–28FFFF
	SA89	1010010xxx	64/32	520000–52FFFF	290000–297FFF
	SA90	1010011xxx	64/32	530000–53FFFF	298000–29FFFF
PPB 31	SA91	1010100xxx	64/32	540000–54FFFF	2A0000–2A7FFF
	SA92	1010101xxx	64/32	550000–55FFFF	2A8000–2AFFFF
	SA93	1010110xxx	64/32	560000–56FFFF	2B0000–2B7FFF
	SA94	1010111xxx	64/32	570000–57FFFF	2B8000–2BFFFF
PPB 32	SA95	1011000xxx	64/32	580000–58FFFF	2C0000–2C7FFF
	SA96	1011001xxx	64/32	590000–59FFFF	2C8000–2CFFFF
	SA97	1011010xxx	64/32	5A0000–5AFFFF	2D0000–2D7FFF
	SA98	1011011xxx	64/32	5B0000–5BFFFF	2D8000–2DFFFF
PPB 33	SA99	1011100xxx	64/32	5C0000–5CFFFF	2E0000–2E7FFF
	SA100	1011101xxx	64/32	5D0000–5DFFFF	2E8000–2EFFFF
	SA101	1011110xxx	64/32	5E0000–5EFFFF	2F0000–2F7FFF
	SA102	1011111xxx	64/32	5F0000–5FFFFF	2F8000–2FFFFF
PPB 34	SA103	1100000xxx	64/32	600000–60FFFF	300000–307FFF
	SA104	1100001xxx	64/32	610000–61FFFF	308000–30FFFF
	SA105	1100010xxx	64/32	620000–62FFFF	310000–317FFF
	SA106	1100011xxx	64/32	630000–63FFFF	318000–31FFFF
PPB 35	SA107	1100100xxx	64/32	640000–64FFFF	320000–327FFF
	SA108	1100101xxx	64/32	650000–65FFFF	328000–32FFFF
	SA109	1100110xxx	64/32	660000–66FFFF	330000–337FFF
	SA110	1100111xxx	64/32	670000–67FFFF	338000–33FFFF
PPB 36	SA111	1101000xxx	64/32	680000–68FFFF	340000–347FFF
	SA112	1101001xxx	64/32	690000–69FFFF	348000–34FFFF
	SA113	1101010xxx	64/32	6A0000–6AFFFF	350000–357FFF
	SA114	1101011xxx	64/32	6B0000–6BFFFF	358000–35FFFF

PPB 37	SA115	1101100xxx	64/32	6C0000–6CFFFF	360000–367FFF
	SA116	1101101xxx	64/32	6D0000–6DFFFF	368000–36FFFF
	SA117	1101110xxx	64/32	6E0000–6EFFFF	370000–377FFF
	SA118	1101111xxx	64/32	6F0000–6FFFFF	378000–37FFFF
PPB 38	SA119	1110000xxx	64/32	700000–70FFFF	380000–387FFF
	SA120	1110001xxx	64/32	710000–71FFFF	388000–38FFFF
	SA121	1110010xxx	64/32	720000–72FFFF	390000–397FFF
	SA122	1110011xxx	64/32	730000–73FFFF	398000–39FFFF
PPB 39	SA123	1110100xxx	64/32	740000–74FFFF	3A0000–3A7FFF
	SA124	1110101xxx	64/32	750000–75FFFF	3A8000–3AFFFF
	SA125	1110110xxx	64/32	760000–76FFFF	3B0000–3B7FFF
	SA126	1110111xxx	64/32	770000–77FFFF	3B8000–3BFFFF
PPB 40	SA127	1111000xxx	64/32	780000–78FFFF	3C0000–3C7FFF
	SA128	1111001xxx	64/32	790000–79FFFF	3C8000–3CFFFF
	SA129	1111010xxx	64/32	7A0000–7AFFFF	3D0000–3D7FFF
	SA130	1111011xxx	64/32	7B0000–7BFFFF	3D8000–3DFFFF
PPB 41	SA131	1111100xxx	64/32	7C0000–7CFFFF	3E0000–3E7FFF
	SA132	1111101xxx	64/32	7D0000–7DFFFF	3E8000–3EFFFF
	SA133	1111110xxx	64/32	7E0000–7EFFFF	3F0000–3F7FFF
	SA134	1111111xxx	64/32	7F0000–7FFFFF	3F8000–3FFFFF

Table 4. Device OPERATING MODES

64M FLASH USER MODE TABLE

Operation	CE#	OE#	WE#	RESET #	WP#/ACC	A0-A21	DQ0-DQ7	DQ8-DQ15	
								BYTE# = V_{IH}	BYTE# = V_{IL}
Read	L	L	H	H	L/H	A_{IN}	D_{OUT}	D_{OUT}	DQ8-DQ14= High-Z, DQ15 = A-1
Write	L	H	L	H	(Note 1)	A_{IN}	D_{IN}	D_{IN}	
Accelerated Program	L	H	L	H	V_{HH}	A_{IN}	D_{IN}	D_{IN}	
CMOS Standby	V_{CC} ±0.3V	X	X	V_{CC}±0.3V	H	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	L/H	X	High-Z	High-Z	High-Z
Hardware Reset	X	X	X	L	L/H	X	High-Z	High-Z	High-Z

Notes:
1. Addresses are A21:A0 in word mode; A21:A-1 in byte mode.
2. If WP# = VIL, on the outermost sector remains protected. If WP# = VIH, the outermost sector is unprotected. WP# has an internal pull-up; when unconnected, WP# is at VIH. All sectors are unprotected when shipped from the factory (The Secured Silicon Sector can be factory protected depending on version ordered.)
3. DIN or DOUT as required by command sequence, data polling, or sector protect algorithm.

Legend
L = Logic Low = VIL, H = Logic High = VIH, VHH = 8.5–9.5V, X = Don't Care, AIN = Address In, DIN = Data In, DOUT = Data Out

USER MODE DEFINITIONS

Word / Byte Configuration

The BYTE# pin controls whether the device data I/O pins operate in the byte or word configuration. If the
BYTE# pin is set at logic '1', the device is in word configuration, DQ0-DQ15 are active and controlled by CE# and OE#.

If the BYTE# pin is set at logic '0', the device is in byte configuration, and only data I/O pins DQ0-DQ7 are active and controlled by CE# and OE#. The data I/O pins DQ8-DQ14 are tri-stated, and the DQ15 pin is used as an input for the LSB (A-1) address function.

Read

All memories require access time to output array data. In a read operation, data is read from one memory location at a time. Addresses are presented to the device in random order, and the propagation delay through the device causes the data on its outputs to arrive with the address on its inputs.

The device defaults to reading array data after device power-up or hardware reset. To read data from the memory array, the system must first assert a valid address on A21-A0, while driving OE# and CE# to VIL. WE# must remain at VIH. All addresses are latched on the falling edge of CE#. Data will appear on DQ15-DQ0 after address access time (tACC), which is equal to the delay from stable addresses to valid output data.The OE# signal must be driven to VIL. Data is output on DQ15-DQ0 pins after the access time (tOE) has elapsed from the falling edge of OE#, assuming the tACC access time has been meet.

Page Read Mode

The device is capable of fast page mode read and is compatible with the page mode Mask ROM read operation. This mode provides faster read access speed for random locations within a page. The page size of the device is 8 words/16 bytes. The appropriate page is selected by the higher address bits A21-A3. Address bits A2-A0 in word mode (A2 to A-1 in byte mode) determine the specific word within a page. The microprocessor supplies the specific word location.

The random or initial page access is equal to tACC or tCE and subsequent page read accesses (as long as the locations specified by the microprocessor falls within that page) is equivalent to tPACC. When CE# is deasserted and reasserted for a subsequent access, the access time is tACC or tCE. Fast page mode accesses are obtained by keeping the "read-page addresses" constant and changing the "intra-read page" addresses.

Autoselect

The Autoselect mode provides manufacturer ID, Device identification, and sector protection information, through identifier codes output from the internal register (separate from the memory array) on DQ7-DQ0.

The device only support to use autoselect command to access autoselect codes. It does not support to apply VID on address pin A9.

- The Autoselect command sequence may be written to an address within a sector that is either in the read or **erase-suspend-read mode.**
- The Autoselect command may not be written while the device is actively programming or erasing.
- The system must write the reset command to return to the read mode (or erase-suspend-read mode if the sector was previously in Erase Suspend).
- When verifying sector protection, the sector address must appear on the appropriate highest order address bits. The remaining address bits are don't care and then read the corresponding identifier code on DQ15-DQ0.

Program/Erase Operations

These devices are capable of several modes of programming and or erase operations which are described in detail in the following sections.
During a write operation, the system must drive CE# and WE# to VIL and OE# to VIH when providing address, command, and data. Addresses are latched on the last falling edge of WE# or CE#, while data is latched on the 1st rising edge of WE# or CE#.

Note the following:

- When the Embedded Program algorithm is complete, the device returns to the read mode.
- The system can determine the status of the program operation by reading the DQ status bits. Refer to the Write Operation Status on page 28 for information on these status bits.
- An “0” cannot be programmed back to a “1.” A succeeding read shows that the data is still “0.”
- Only erase operations can convert a “0” to a “1.”
- Any commands written to the device during the Embedded Program/Erase are ignored except the Suspend commands.
- Secured Silicon Sector, Autoselect, and CFI functions are unavailable when a program operation is in progress.
- A hardware reset and/or power removal immediately terminates the Program/Erase operation and the Program/Erase command sequence should be reinitiated once the device has returned to the read mode to ensure data integrity.
- Programming is allowed in any sequence and across sector boundaries for single word programming
  operation.
- Programming to the same word address multiple times without intervening erases is permitted.

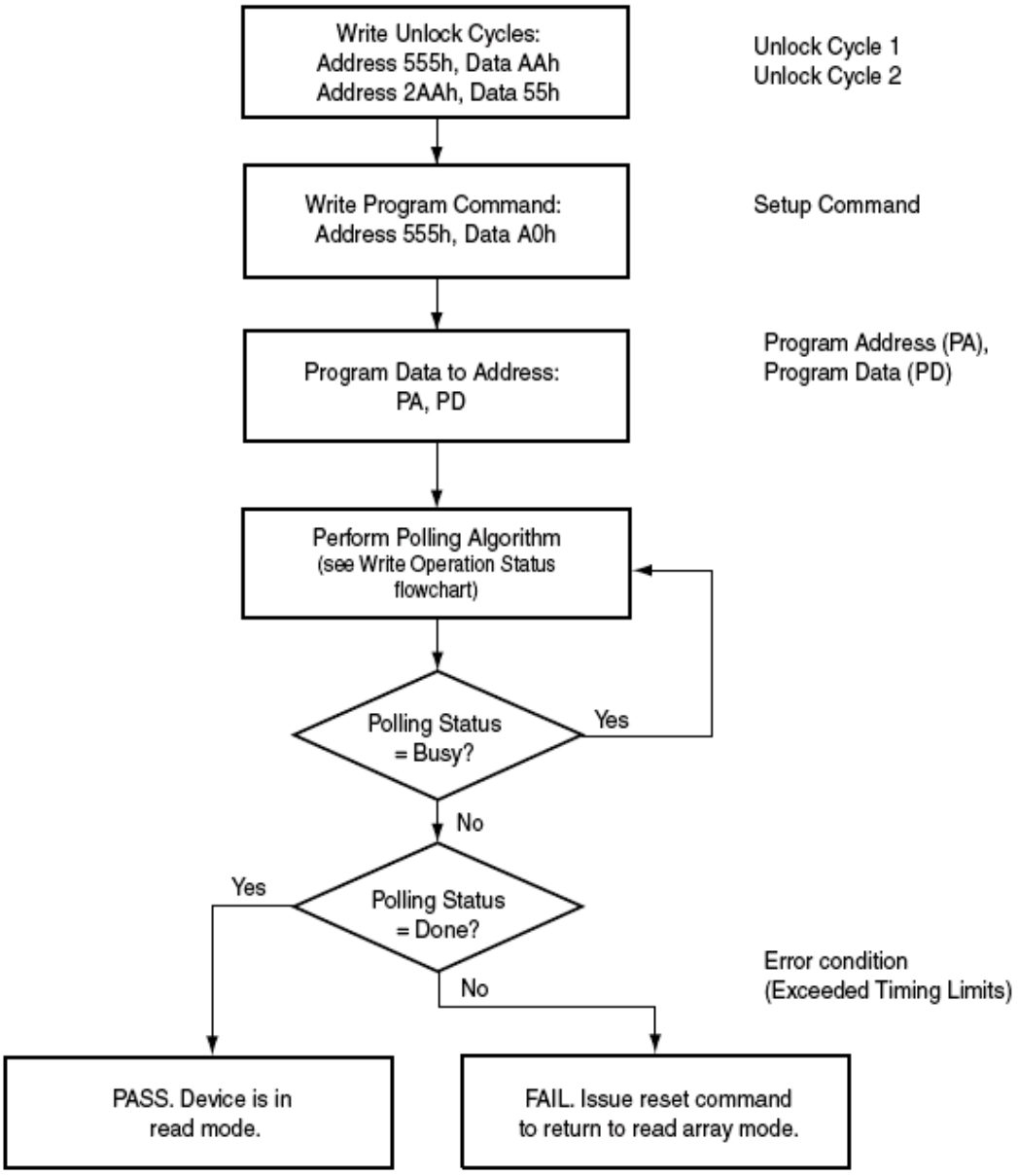
Single Word Programming

Single word programming mode is one method of programming the Flash. In this mode, four Flash command write cycles are used to program an individual Flash address. The data for this programming operation could be 8 or 16-bits wide.

While the single word programming method is supported by most devices, in general Single Word Programming is not recommended for devices that support Write Buffer Programming.
When the Embedded Program algorithm is complete, the device then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by reading the DQ status bits.

- During programming, any command (except the Suspend Program command) is ignored.
- The Secured Silicon Sector, Autoselect, and CFI functions are unavailable when a program operation is in progress.
- A hardware reset immediately terminates the program operation. The program command sequence should be reinitiated once the device has returned to the read mode, to ensure data integrity.
- Programming to the same address multiple times continuously (for example, “walking” a bit within a word) is permitted.

Figure 4. Single Word Program



Write Buffer Programming

Write Buffer Programming allows the system to write a maximum of 16 words in one programming operation. This results in a faster effective word programming time than the standard "word" programming algorithms. The Write Buffer Programming command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the Write Buffer Load command written at the Sector Address in which programming occurs. At this point, the system writes the number of "word locations minus 1" that are loaded into the page buffer at the Sector Address in which programming occurs. This tells the device how many write buffer addresses are loaded with data and therefore when to expect the "Program Buffer to Flash" confirm command. The number of locations to program cannot exceed the size of the write buffer or the operation aborts. (Number loaded = the number of locations to program minus 1. For example, if the system programs 6 address locations, then 05h should be written to the device.)

The system then writes the starting address/data combination. This starting address is the first address/data pair to be programmed, and selects the "write-buffer-page" address. All subsequent address/data pairs must fall within the elected-write-buffer-page.

The "write-buffer-page" is selected by using the addresses A21–A4.

The "write-buffer-page" addresses must be the same for all address/data pairs loaded into the write buffer. (This means Write Buffer Programming cannot be performed across multiple "write-buffer-pages." This also means that Write Buffer Programming cannot be performed across multiple sectors. If the system attempts to load programming data outside of the selected "write-buffer-page", the operation ABORTs.)

After writing the Starting Address/Data pair, the system then writes the remaining address/data pairs into the write buffer.

Note that if a Write Buffer address location is loaded multiple times, the "address/data pair" counter is decremented for every data load operation. Also, the last data loaded at a location before the "Program Buffer to Flash" confirm command is the data programmed into the device. It is the software's responsibility to comprehend ramifications of loading a write-buffer location more than once. The counter decrements for each data load operation, NOT for each unique write-buffer-address location. Once the specified number of write buffer locations have been loaded, the system must then write the "Program Buffer to Flash" command at the Sector Address. Any other address/data write combinations abort the Write Buffer Programming operation. The Write Operation Status bits should be used while monitoring the last address location loaded into the write buffer. This eliminates the need to store an address in memory because the system can load the last address location, issue the program confirm command at the last loaded address location, and then check the write operation status at that same address. DQ7, DQ6, DQ5, DQ2, and DQ1 should be monitored to determine the device status during Write Buffer Programming.

The write-buffer "embedded" programming operation can be suspended using the standard suspend/resume commands. Upon successful completion of the Write Buffer Programming operation, the device returns to READ mode.

The Write Buffer Programming Sequence is ABORTED under any of the following conditions:

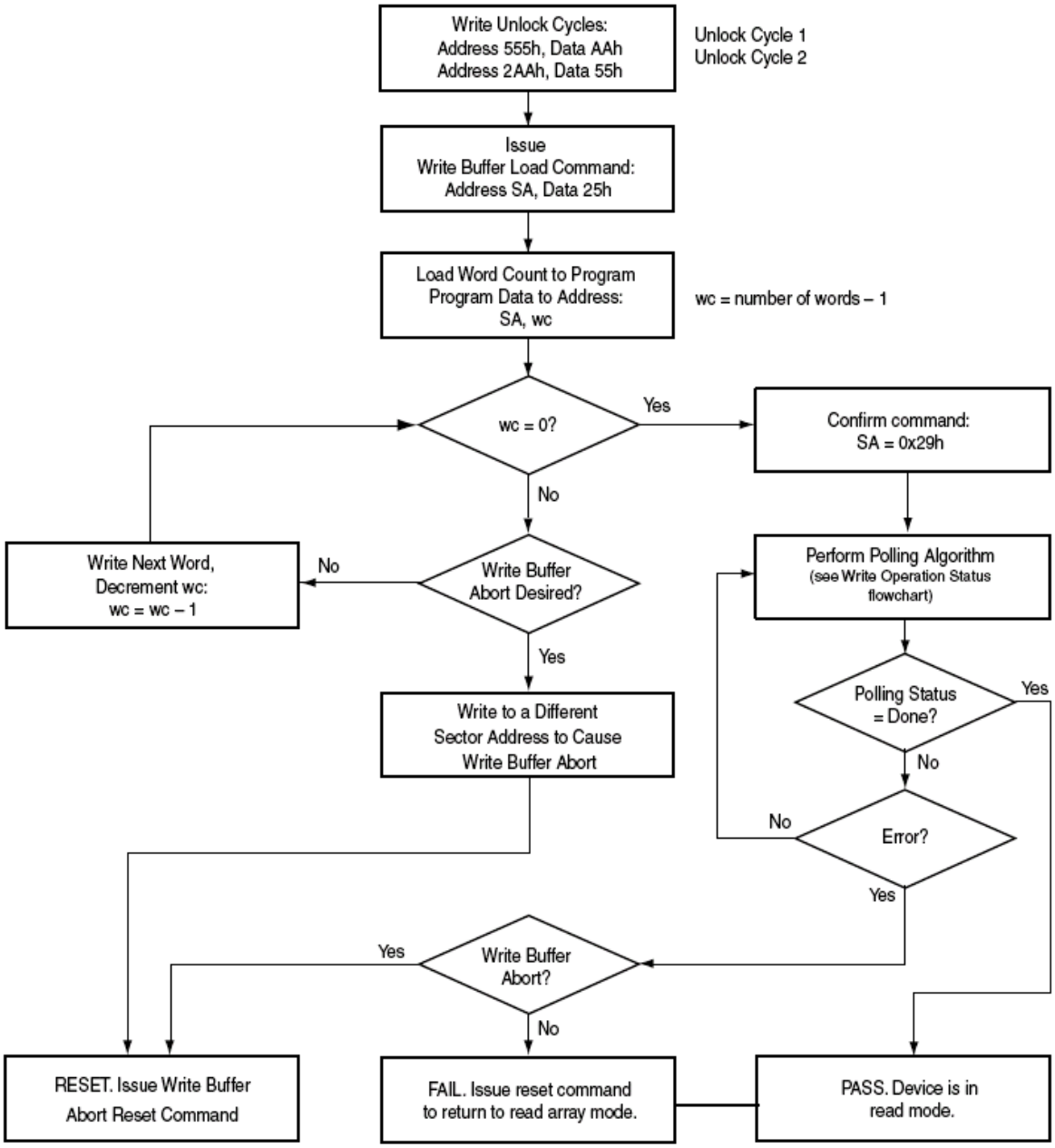
- Load a value that is greater than the page buffer size during the "Number of Locations to Program" step.
- Write to an address in a sector different than the one specified during the Write-Buffer-Load command.
- Write an Address/Data pair to a different write-buffer-page than the one selected by the "Starting Address" during the "write buffer data loading" stage of the operation.
- Writing anything other than the Program to Buffer Flash Command after the specified number of "data load" cycles.

The ABORT condition is indicated by DQ1 = 1, DQ6 = TOGGLE, DQ5 = 0. This indicates that the Write Buffer Programming Operation was ABORTED. Note that the Secured Silicon sector, autoselect, and CFI functions are unavailable when a program operation is in progress.

Write buffer programming is allowed in any sequence of memory (or address) locations. These flash devices are capable of handling multiple write buffer programming operations on the same write buffer address range without intervening erases.

Use of the write buffer is strongly recommended for programming when multiple words are to be programmed.

Figure 5. Write Buffer Programming Operation



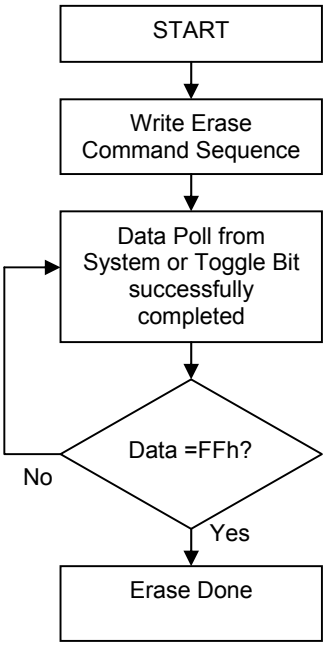
Sector Erase

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two un-lock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the address of the sector to be erased, and the sector erase command. The Command Definitions table shows the address and data requirements for the sector erase command sequence.

Once the sector erase operation has begun, only the Sector Erase Suspend command is valid. All other commands are ignored. If there are several sectors to be erased, Sector Erase Command sequences must be issued for each sector. That is, only **a sector address can be specified for each Sector Erase command**. Users must issue another Sector Erase command for the next sector to be erased after the previous one is completed.

When the Embedded Erase algorithm is completed, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, or DQ2. Refer to “Write Operation Status” for information on these status bits. Flowchart 4 illustrates the algorithm for the erase operation. Refer to the Erase/Program Operations tables in the “AC Characteristics” section for parameters, and to the Sector Erase Operations Timing diagram for timing waveforms.

Figure 6. Sector Erase Operation



Chip Erase Command Sequence

Chip erase is a six-bus cycle operation as indicated by Table 13. These commands invoke the Embedded Erase algorithm, which does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory to an all zero data pattern prior to electrical erase. After a successful chip erase, all locations of the chip contain FFFFh. The system is not required to provide any controls or timings during these operations.

When the Embedded Erase algorithm is complete, that sector returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7 or DQ6/DQ2. Refer to “Write Operation Status” for information on these status bits.

Any commands written during the chip erase operation are ignored. However, note that a hardware reset immediately terminates the erase operation. If that occurs, the chip erase command sequence should be reinitiated once that sector has returned to reading array data, to ensure the entire array is properly erased.

Erase Suspend/Erase Resume Commands

The Erase Suspend command allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. The sector address is required when writing this command. This command is valid only during the sector erase operation. The Sector Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm. Addresses are don’t-cares when writing the Sector Erase Suspend command.

When the Erase Suspend command is written during the sector erase operation, the device requires a maximum of 20 μs to suspend the erase operation.

After the erase operation has been suspended, the device enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device “erase suspends” all sectors selected for erasure.) Reading at any address within erase-suspended sectors produces status information on DQ7-DQ0. The system can use DQ7, or DQ6, and DQ2 together, to determine if a sector is actively erasing or is erase-suspended.

After an erase-suspended program operation is complete, the device returns to the erase-suspend-read
mode. The system can determine the status of the program operation using write operation status bits, just as in the standard program operation.

In the erase-suspend-read mode, the system can also issue the Autoselect command sequence. Refer to Write Buffer Programming and the Autoselect for details.
To resume the sector erase operation, the system must write the Erase Resume command. The address of the erase-suspended sector is required when writing this command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

Program Suspend/Program Resume Commands

The Program Suspend command allows the system to interrupt an embedded programming operation or a “Write to Buffer” programming operation so that data can read from any non-suspended sector. When the Program Suspend command is written during a programming process, the device halts the programming operation within 15 μs maximum (5 μs typical) and updates the status bits. Addresses are “don't-cares” when writing the Program Suspend command.

After the programming operation has been suspended, the system can read array data from any nonsuspended sector. The Program Suspend command may also be issued during a programming operation while an erase is suspended. In this case, data may be read from any addresses not within a sector in Erase Suspend or Program Suspend. If a read is needed from the Secured Silicon Sector area, then user must use the proper command sequences to enter and exit this region.

The system may also write the Autoselect Command Sequence when the device is in Program Suspend mode. The device allows reading Autoselect codes in the suspended sectors, since the codes are not stored in the memory array. When the device exits the Autoselect mode, the device reverts to Program Suspend mode, and is ready for another valid operation.

After the Program Resume command is written, the device reverts to programming. The system can determine the status of the program operation using the write operation status bits, just as in the standard program operation.

The system must write the Program Resume command (address bits are “don't care”) to exit the Program Suspend mode and continue the programming operation. Further writes of the Program Resume command are ignored. Another Program Suspend command can be written after the device has resumed programming.

Accelerated Program

Accelerated single word programming and write buffer programming operations are enabled through the
WP#/ACC pin. This method is faster than the standard program command sequences.

If the system asserts V_{HH} on this input, the device automatically enters the Accelerated Program mode and uses the higher voltage on the input to reduce the time required for program operations. The system can then use the Write Buffer Load command sequence provided by the Accelerated Program mode. Note that if a “Write-to-Buffer-Abort Reset” is required while in Accelerated Program mode, the full 3-cycle RESET command sequence must be used to reset the device. Removing V_{HH} from the ACC input, upon completion of the embedded program operation, returns the device to normal operation.

- Sectors must be unlocked prior to raising WP#/ACC to V_{HH}.
- The WP#/ACC pin must not be at V_{HH} for operations other than accelerated programming, or device damage may result.
- It is recommended that WP#/ACC apply V_{HH} after power-up sequence is completed. In addition, it is recommended that WP#/ACC apply from V_{HH} to VIH/VIL before powering down V_{CC} .

Write Operation Status

The device provides several bits to determine the status of a program or erase operation. The following subsections describe the function of DQ1, DQ2, DQ3, DQ5, DQ6, and DQ7.

DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether the device is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence. Note that the Data# Polling is valid only for the last word being programmed in the write-buffer-page during Write Buffer Programming. Reading Data# Polling status on any word other than the last word to be programmed in the write-buffer-page returns false status information.

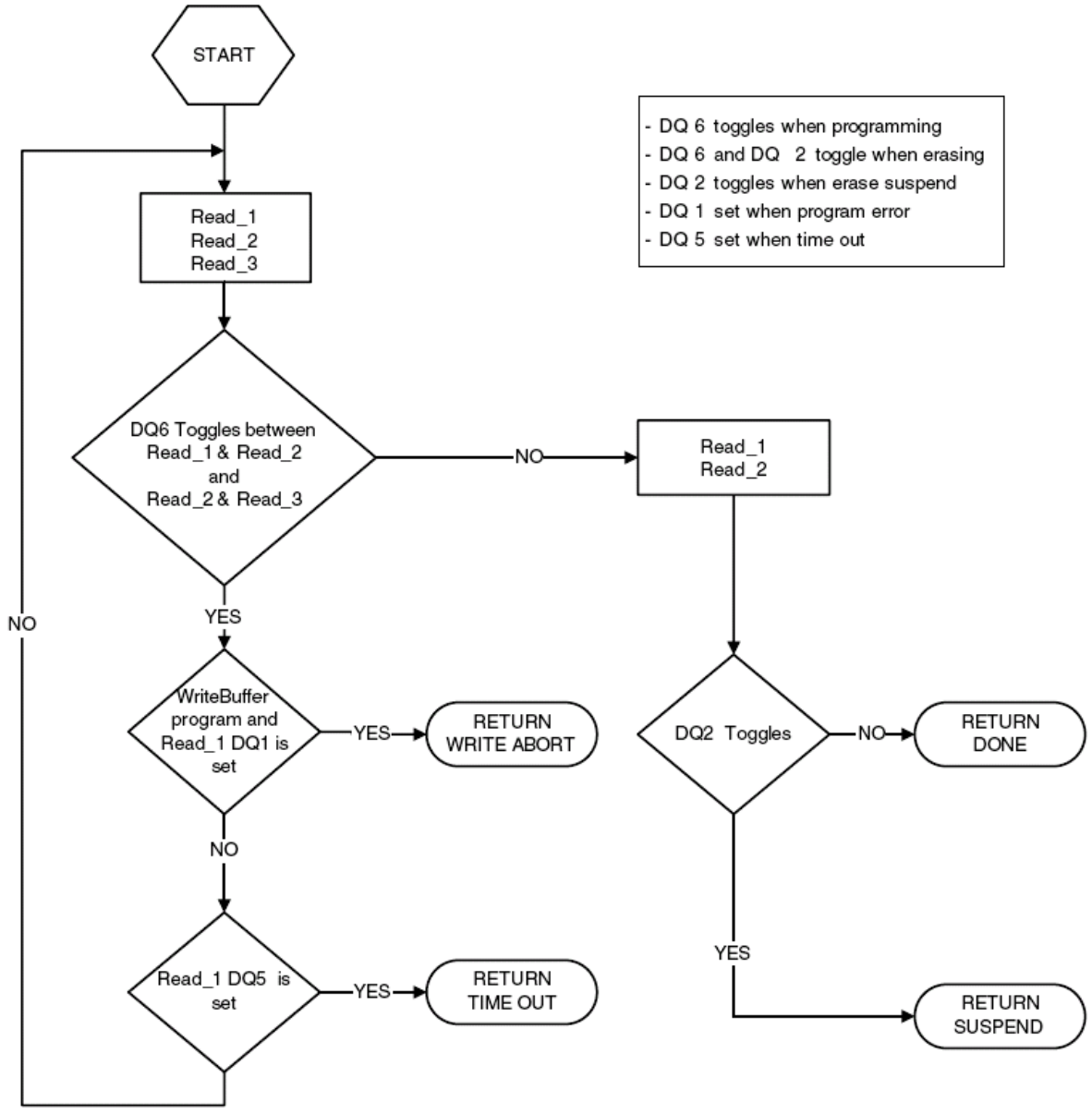
During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# polling on DQ7 is active, then that sector returns to the read mode.

During the Embedded Erase Algorithm, Data# polling produces a “0” on DQ7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a “1” on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.
After an erase command sequence is written, if all sectors selected for erasing are protected, Data#

Polling on DQ7 is active for approximately 100 µs, then the device returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ6-DQ0 while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ6-DQ0 may be still invalid. Valid data on DQ7-D00 appears on successive read cycles.

Figure 7. Write Operation Status Flowchart



DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address that is being programmed or erased causes DQ6 to toggle. When the operation is complete, DQ6 stops toggling.
After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase 2suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7.

If a program address falls within a protected sector, DQ6 toggles for approximately 1µs after the program command sequence is written, then returns to reading array data. DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program Algorithm is complete. Toggle Bit I on DQ6 requires either OE# or CE# to be de-asserted and reasserted to show the change in state.

DQ2: Toggle Bit II

The “Toggle Bit II” on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence. DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information.

Reading Toggle Bits DQ6/DQ2

Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erases operation. The system can read array data on DQ7–DQ0 on the following read cycle. However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high. If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erases operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data. The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation.

Note
When verifying the status of a write operation (embedded program/erase) of a memory sector, DQ6 and DQ2 toggle between high and low states in a series of consecutive and contiguous status read cycles. In order for this toggling behavior to be properly observed, the consecutive status bit reads must not be interleaved with read accesses to other memory sectors. If it is not possible to temporarily prevent reads to other memory sectors, then it is recommended to use the DQ7 status bit as the alternative method of determining the active or inactive status of the write operation.

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a "1," indicating that the program or erase cycle was not successfully completed. The device does not output a 1 on DQ5 if the system tries to program a 1 to a location that was previously programmed to 0. Only an erase operation can change a 0 back to a 1. Under this condition, the device ignores the bit that was incorrectly instructed to be programmed from a 0 to a 1, while any other bits that were correctly requested to be changed from 1 to 0 are programmed. Attempting to program a 0 to a 1 is masked during the programming operation. Under valid DQ5 conditions, the system must write the reset command to return to the read mode (or to the erase-suspend-read mode if a sector was previously in the erase-suspend-program mode).

DQ3: Sector Erase Timeout State Indicator

After writing a sector erase command sequence, the output on DQ3 can be checked to determine whether or not an erase operation has begun. (The sector erase timer does not apply to the chip erase command.) When sector erase starts, DQ3 switches from "0" to "1". This device does not support multiple sector erase (continuous sector erase) command sequences so it is not very meaningful since it immediately shows as a "1" after the first 30h command. Future devices may support this feature.

DQ1: Write to Buffer Abort

DQ1 indicates whether a Write to Buffer operation was aborted. Under these conditions DQ1 produces a "1". The system must issue the "Write to Buffer Abort Reset" command sequence to return the device to reading array data.

Table 5. Write Operation Status

Status			DQ7 (note 2)	DQ6	DQ5 (note 1)	DQ3	DQ2 (note 2)	DQ1	RY/BY#
Standard Mode	Embedded Program Algorithm		DQ7#	Toggle	0	N/A	No Toggle	0	0
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle	N/A	0
Program Suspend Mode	Program Suspend Read	Program Suspended Sector	Invalid (Not allowed)						1
		Non-Program Suspended Sector	Data						1
Erase Suspend Mode	Erase Suspend Read	Erase Suspended Sector	1	No Toggle	0	N/A	Toggle	N/A	1
		Non-Erase Suspended Sector	Data						0
	Erase Suspend Program (Embedded Program)		DQ7#	Toggle	0	N/A	N/A	N/A	0
Write to Buffer	Busy(note 3)		DQ7#	Toggle	0	N/A	N/A	0	0
	Abort(note 4)		N/A	Toggle	0	N/A	N/A	1	0

Notes

1. DQ5 switches to 1 when an Embedded Program, Embedded Erase, or Write-to-Buffer operation has exceeded the maximum timing limits.
2. DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.
3. The Data# Polling algorithm should be used to monitor the last loaded write-buffer address location.
4. DQ1 switches to 1 when the device has aborted the write-to-buffer operation

Writing Commands/Command Sequences

During a write operation, the system must drive CE# and WE# to VIL and OE# to VIH when providing an address, command, and data. Addresses are latched on the last falling edge of WE# or CE#, while data is latched on the 1st rising edge of WE# or CE#. An erase operation can erase one sector or the

entire device. Table 3 indicates the address space that each sector occupies. The device address space is divided into uniform 32KW/64KB sectors. A sector address is the set of address bits required to uniquely select a sector. ICC2 in "DC Characteristics" represents the active current specification for the write mode. "AC Characteristics" contains timing specification tables and timing diagrams for write operations.

RY/BY#

The RY/BY# is a dedicated, open-drain output pin that indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to V_{CC}. This feature allows the host system to detect when data is ready to be read by simply monitoring the RY/BY# pin, which is a dedicated output and controlled by CE# (not OE#).

Hardware Reset

The RESET# input provides a hardware method of resetting the device to reading array data. When RESET# is driven low for at least a period of tRP (RESET# Pulse Width), the device immediately terminates any operation in progress, tristates all outputs, resets the configuration register, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data.

To ensure data integrity Program/Erase operations that were interrupted should be reinitiated once the device is ready to accept another command sequence.

When RESET# is held at VSS, the device draws V_{CC} reset current (ICC5). If RESET# is held at VIL, but not at VSS, the standby current is greater. RESET# may be tied to the system reset circuitry which enables the system to read the boot-up firmware from the Flash memory upon a system reset.

Software Reset

Software reset is part of the command set that also returns the device to array read mode and must be used for the following conditions:

1. To exit Autoselect mode
2. When DQ5 goes high during write status operation that indicates program or erase cycle was not successfully completed
3. Exit sector lock/unlock operation.
4. To return to erase-suspend-read mode if the device was previously in Erase Suspend mode.
5. After any aborted operations

The following are additional points to consider when using the reset command:

- This command resets the sectors to the read and address bits are ignored.
- Reset commands are ignored during program and erase operations.
- The reset command may be written between the cycles in a program command sequence before programming begins (prior to the third cycle). This resets the sector to which the system was writing to the read mode.
- If the program command sequence is written to a sector that is in the Erase Suspend mode, writing the reset command returns that sector to the erase-suspend-read mode.
- The reset command may be written during an Autoselect command sequence.
- If a sector has entered the Autoselect mode while in the Erase Suspend mode, writing the reset command returns that sector to the erase-suspend-read mode.
- If DQ1 goes high during a Write Buffer Programming operation, the system must write the "Write to Buffer Abort Reset" command sequence to RESET the device to reading array data. The standard RESET command does not work during this condition.

Advanced Sector Protection/Unprotection

The Advanced Sector Protection/Unprotection feature disables or enables programming or erase operations in any or all sectors and can be implemented through software and/or hardware methods, which are independent of each other. This section describes the various methods of protecting data stored in the memory array. An overview of these methods in shown in Figure 8.

Figure 8a. Advanced Sector Protection/Unprotection for Top Boot Sector

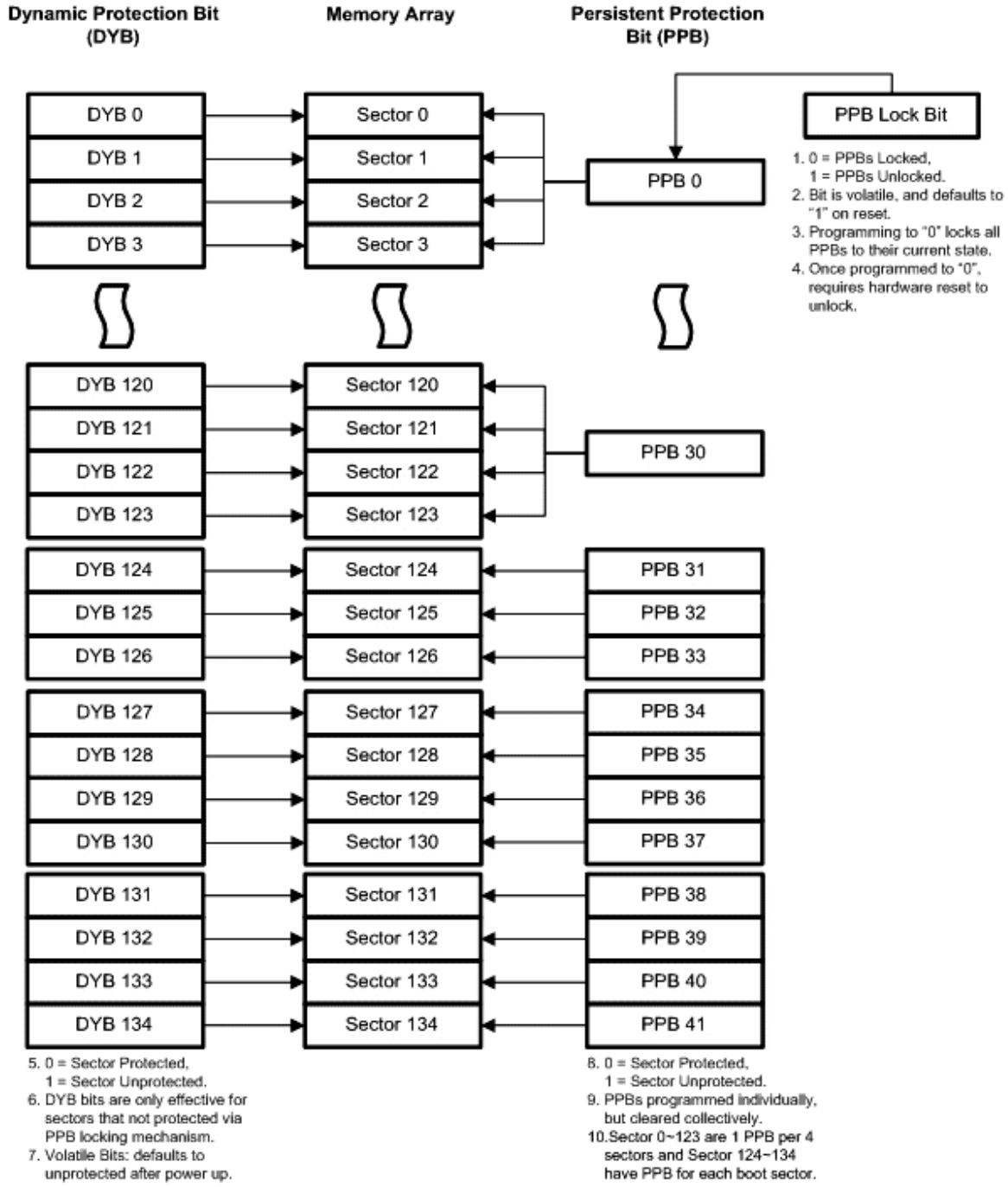
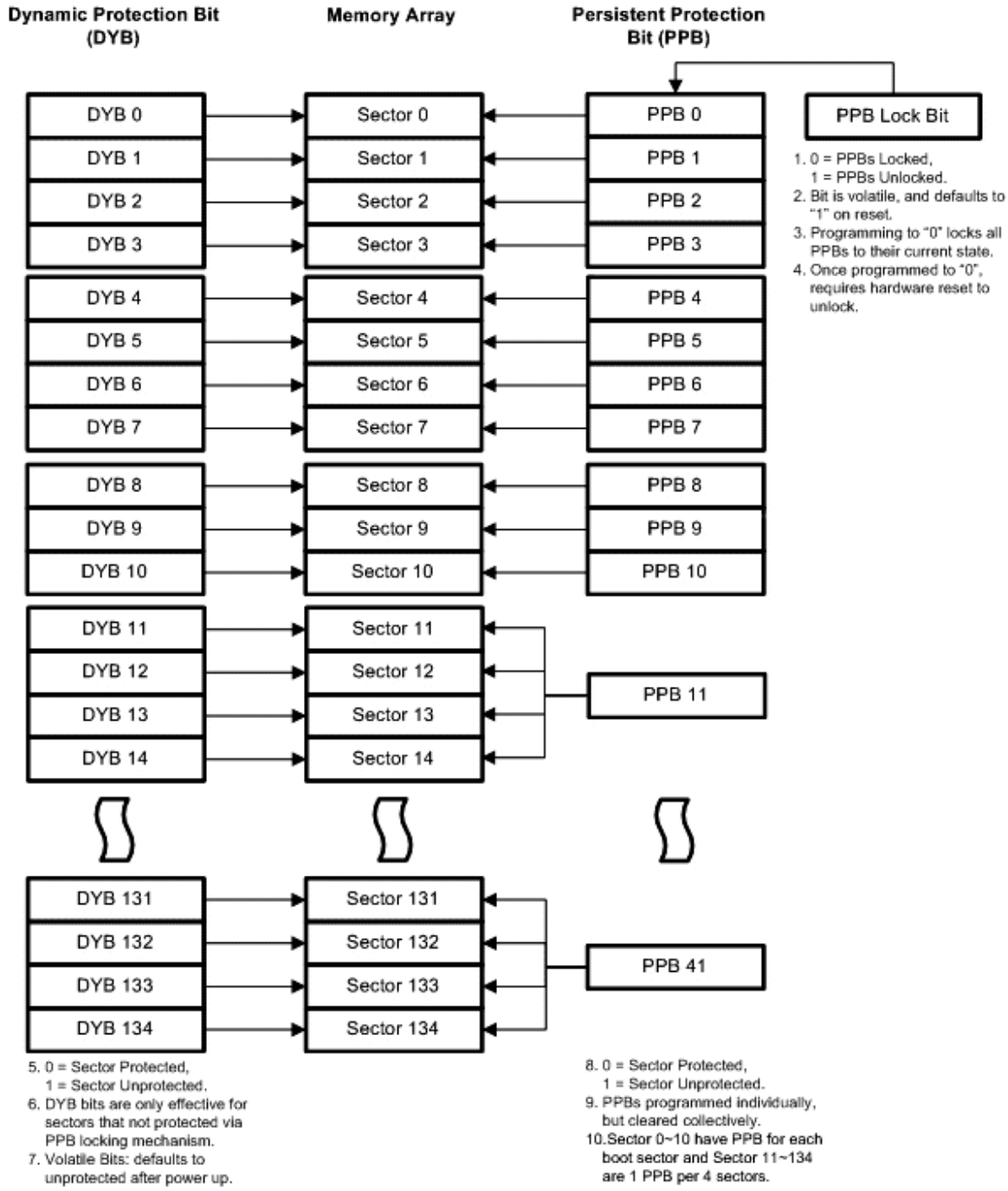


Figure 8b. Advanced Sector Protection/Unprotection for Bottom Boot Sector



Lock Register

The Lock Register consists of 4 bits. The Secured Silicon Sector Protection Bit is DQ0, Persistent Protection Mode Lock Bit is DQ1, Persistent Sector Protection OTP bit is DQ3 and DYB Lock Boot Bit is DQ4. If DQ0 is '0', it means that the Customer Secured Silicon area is locked and if DQ0 is '1', it means that it is unlocked. When DQ1 is set to '0', the device is used in the Persistent Protection Mode. DQ3 is programmed in the EON factory. When the device is programmed to disable all PPB erase command,

DQ3 outputs a '0', when the lock register bits are read. Similarly, if the device is programmed to enable all PPB erase command, DQ3 outputs a '1' when the lock register bits are read. Likewise the DQ4 bit is also programmed in the EON Factory. DQ4 is the bit which indicates whether Volatile Sector Protection Bit (DYB) is protected or not after boot-up. When the device is programmed to set all Volatile Sector Protection Bit protected after power-up, DQ4 outputs a '0' when the lock register bits are read. Similarly, when the device is programmed to set all Volatile Sector Protection Bit unprotected after power-up, DQ4 outputs a '1'. Each of these bits in the lock register are non-volatile. DQ15- DQ5 are reserved and will be 1's.

Table 6. Lock Register

DQ15-5	DQ4	DQ3	DQ2	DQ1	DQ0
Reserved	DYB Lock Boot Bit	PPB One Time Programmable Bit	Reserved	Persistent Protection Mode Lock Bit	Secured Silicon Sector Protection Bit
(default = 1)	0 = protected all DYB after boot-up 1 = unprotected all DYB after boot-up (default = 1)	0 = All PPB Erase Command disabled 1 = All PPB Erase Command enabled (default = 1)	(default = 1)	0 = Persistent Protection enabled (default = 0)	0 = protected 1 = unprotect (default = 1)

Notes:
1. After the Lock Register Bits Command Set Entry command sequence is written, reads and writes for Sector 0 are disabled, while read from other sectors are allowed until exiting this mode.
2. Only DQ0 could be change by Lock Register Bits Command for user. Others bits were set by Factory.
3. If user needs the product of DQ3 = 0, please chose the EN29GA064AT/B. For the detail information of EN29GA064AT/B please contact with Eon directly.

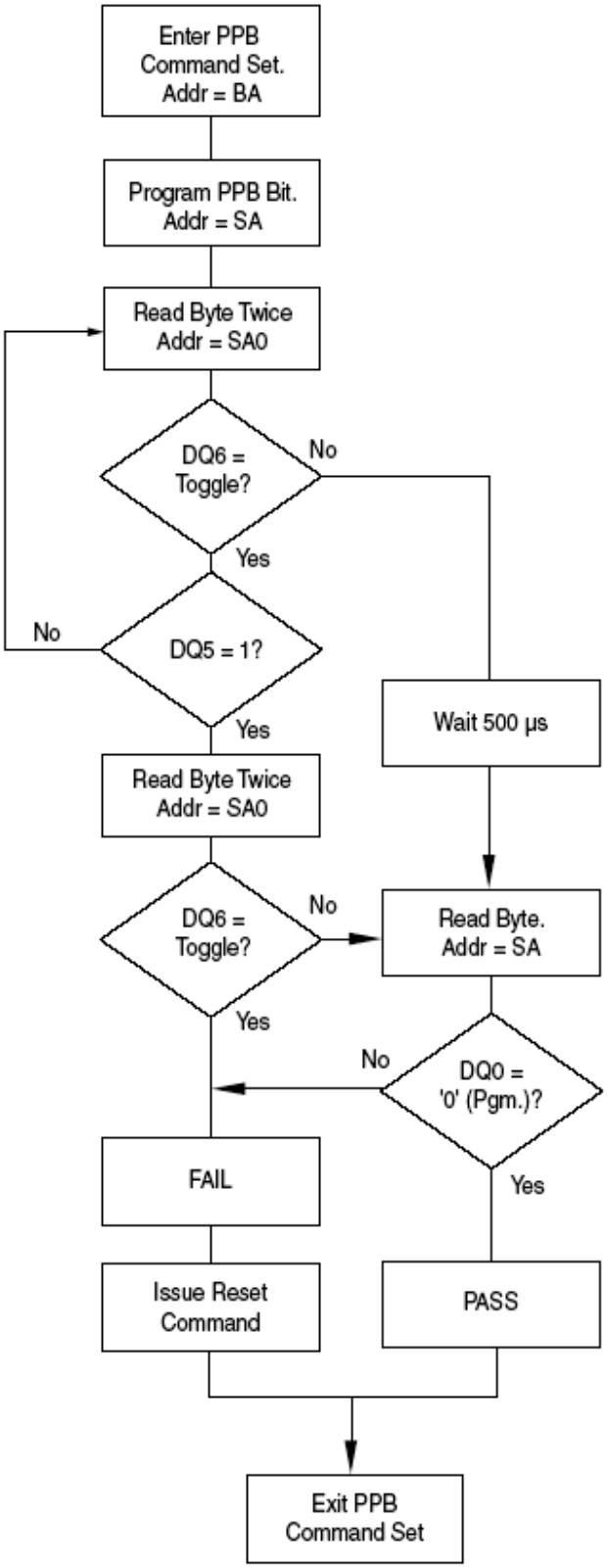
After selecting a sector protection method, each sector can operate in any of the following three states:
1. Constantly locked: The selected sectors are protected and can not be reprogrammed unless PPB lock bit is cleared via hardware reset, or power cycle.
2. Dynamically locked: The selected sectors are protected and can be altered via software commands.
3. Unlocked: The sectors are unprotected and can be erased and/or programmed.

Persistent Protection Bits

The Persistent Protection Bits are unique and nonvolatile. For top boot sector device, Sector 0~123 are 1 PPB per 4 sectors and Sector 124~134 have PPB for each boot sector. For bottom boot sector device, Sector 0~10 have PPB for each boot sector and Sector 11~134 are 1 PPB per 4 sectors(refer to Figure 8a, 8b and Table 3a, 3b). The PPB has the same endurances as the Flash memory. Preprogramming and verification prior to erasure are handled by the device, and therefore do not require system monitoring.

Notes
1. Each PPB is individually programmed and all are erased in parallel.
2. While programming PPB for the four sectors and Data polling on programming PPB address, array data can not be read from any sectors.
3. Entry command disables reads and writes for all sectors selected.
4. Reads within that sector return the PPB status for that sector.
5. All Reads must be performed using the read mode.
6. The specific sector address are written at the same time as the program command.
7. If the PPB Lock Bit is set, the PPB Program or erase command does not execute and times-out without programming or erasing the PPB.
8. There are no means for individually erasing a specific PPB and no specific sector address is required for this operation.
9. Exit command must be issued after the execution which resets the device to read mode and re-enables reads and writes for all sectors.
10. The programming state of the PPB for given sectors can be verified by writing a PPB Status Read Command to the device as described by the flow chart shown in Figure 9. User only can use DQ6 and RY/BY# pin to detect programming status.

Figure 9. PPB Program Algorithm



Note: BA = base address

Dynamic Protection Bits

Dynamic Protection Bits are volatile and unique for each sector and can be individually modified. DYBs only control the protection scheme for unprotected sectors that have their PPBs cleared (erased to “1”). By issuing the DYB Set or Clear command sequences, the DYBs are set (programmed to “0”) or cleared (erased to “1”), thus placing each sector in the protected or unprotected state respectively. This feature allows software to easily protect sectors against inadvertent changes yet does not prevent the easy removal of protection when changes are needed.

Notes

1. The DYBs can be set (programmed to “0”) or cleared (erased to “1”) as often as needed. When the parts are first shipped, the PPBs are cleared (erased to “1”) and upon power up or reset, the DYBs can be set or cleared depending upon the ordering option chosen.
2. If the option to clear the DYBs after power up is chosen, (erased to “1”), then the sectorsmay be modified depending upon the PPB state of that sector (see Table 7).
3. The sectors would be in the protected state If the option to set the DYBs after power up is chosen (programmed to “0”).
4. It is possible to have sectors that are persistently locked with sectors that are left in the dynamic state.
5. The DYB Set or Clear commands for the dynamic sectors signify protected or unprotectedstate of the sectors respectively. However, if there is a need to change the status of the persistently locked sectors, a few more steps are required. First, the PPB Lock Bit must be cleared by either putting the device through a power-cycle, or hardware reset. The PPBs can then be changed to reflect the desired settings. Setting the PPB Lock Bit once again locks the PPBs, and the device operates normally again.
6. To achieve the best protection, it is recommended to execute the PPB Lock Bit Set command early in the boot code and protect the boot code by holding WP#/ACC = VIL. Note that the PPB and DYB bits have the same function when WP#/ACC = VHH as they do when ACC =VIH.

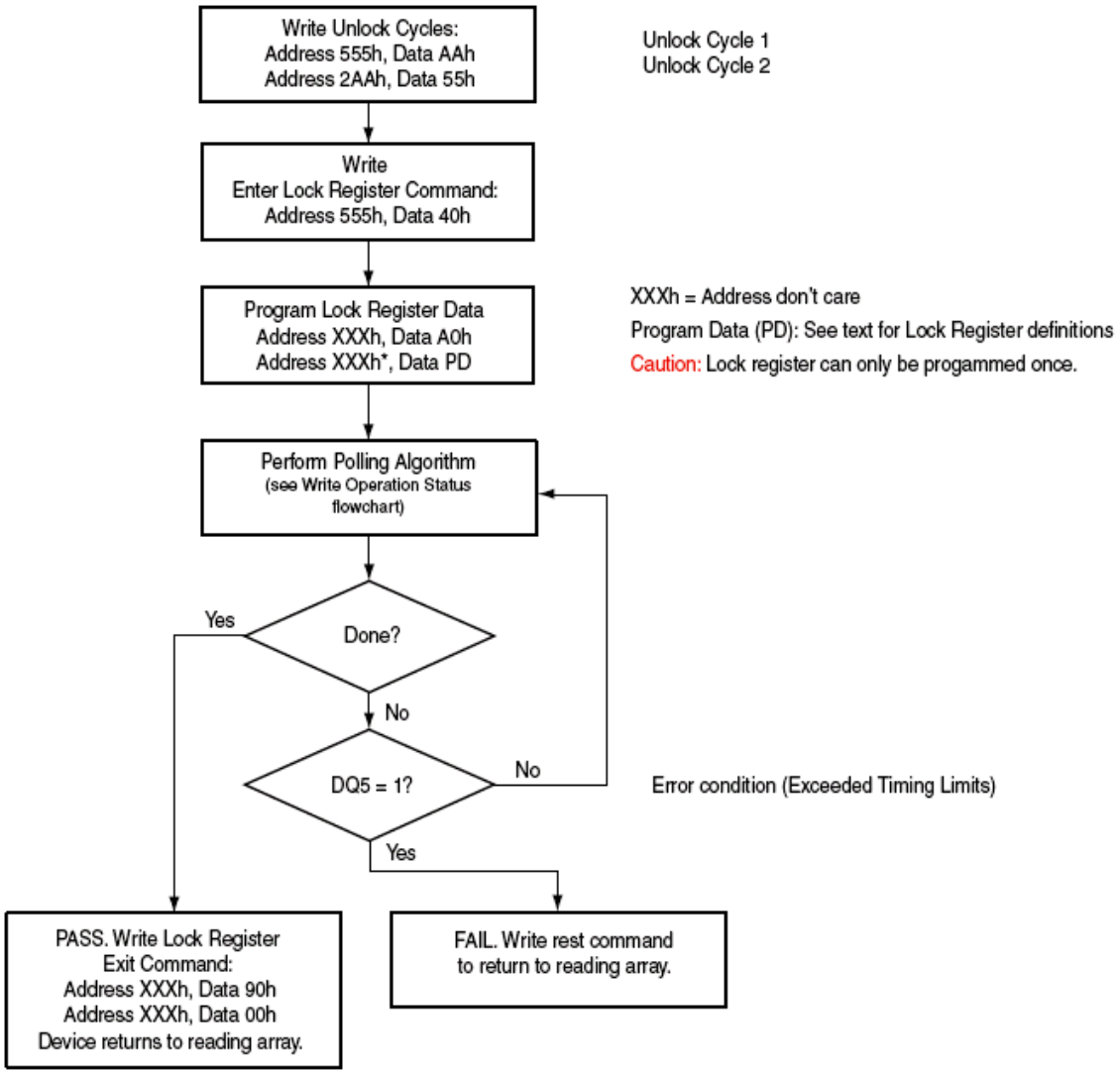
Persistent Protection Bit Lock Bit

The Persistent Protection Bit Lock Bit is a global volatile bit for all sectors. When set (programmed to “0”), it locks all PPBs and when cleared (erased to “1”), allows the PPBs to be changed. There is only one PPB Lock Bit per device.

Notes

1. No software command sequence unlocks this bit, but only a hardware reset or a power-up clears this bit.
2. The PPB Lock Bit must be set (programmed to “0”) only after all PPBs are configured to the desired settings.

Figure 10. Lock Register Program Algorithm



Advanced Sector Protection Software Examples

Table 7. Sector Protection Schemes: DYB, PPB and PPB Lock Bit Combinations

Unique Device PPB Lock Bit 0 = locked 1 = unlocked		Sector PPB 0 = protected 1 = unprotected	Sector DYB 0 = protected 1 = unprotected	Sector Protection Status
Any Sector	0	0	x	Protected through PPB
Any Sector	0	0	x	Protected through PPB
Any Sector	0	1	1	Unprotected
Any Sector	0	1	0	Protected through DYB
Any Sector	1	0	x	Protected through PPB
Any Sector	1	0	x	Protected through PPB
Any Sector	1	1	0	Protected through DYB
Any Sector	1	1	1	Unprotected

Table 7 contains all possible combinations of the DYB, PPB, and PPB Lock Bit relating to the status of the sector. In summary, if the PPB Lock Bit is locked (set to “0”), no changes to the PPBs are allowed. The PPB Lock Bit can only be unlocked (reset to “1”) through a hardware reset or power cycle. See also Figure 9 for an overview of the Advanced Sector Protection feature.

Hardware Data Protection Methods

The device offers two main types of data protection at the sector level via hardware control:

- When WP#/ACC is at VIL, the either the highest or lowest sector is locked (device specific).

There are additional methods by which intended or accidental erasure of any sectors can be prevented via hardware means. The following subsections describes these methods:

WP#/ACC Method

The Write Protect feature provides a hardware method of protecting one outermost sector. This function is provided by the WP#/ACC pin and overrides the previously discussed Sector Protection/Unprotection method.

If the system asserts VIL on the WP#/ACC pin, the device disables program and erase functions in the highest or lowest sector independently of whether the sector was protected or unprotected using the method described in Advanced Sector Protection/Unprotection.

If the system asserts VIH on the WP#/ACC pin, the device reverts to whether the boot sectors were last set to be protected or unprotected. That is, sector protection or unprotection for these sectors depends on whether they were last protected or unprotected.

The WP#/ACC pin must be held stable during a command sequence execution. WP# has an internal pull-up; when unconnected, WP# is set at VIH.

Note
If WP#/ACC is at VIL when the device is in the standby mode, the maximum input load current is increased.

Low V_{CC} Write Inhibit

When VCC is less than VLKO, the device does not accept any write cycles. This protects data during VCC power-up and power-down.

The command register and all internal program/erase circuits are disabled, and the device resets to reading array data. Subsequent writes are ignored until VCC is greater than VLKO. The system must provide the proper signals to the control inputs to prevent unintentional writes when VCC is greater than VLKO.

Write Pulse “Glitch Protection”

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

Power-Up Write Inhibit

If WE# = CE# = RESET# = VIL and OE# = VIH during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.

Power Conservation Modes

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input. The device enters the CMOS standby mode when the CE# and RESET# inputs are both held at V_{CC} ± 0.3 V. The device requires standard access time (tCE) for read access, before it is ready to read data. If the device is deselected during erasure or programming, the device draws active current until the operation is completed. ICC4 in “DC Characteristics” represents the standby current specification

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for tACC + 30 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system.

Hardware RESET# Input Operation

The RESET# input provides a hardware method of resetting the device to reading array data. When RESET# is driven low for at least a period of tRP, the device immediately terminates any operation in progress, tristates all outputs, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence to ensure data integrity.

When RESET# is held at VSS ± 0.3 V, the device draws ICC reset current (ICC5). If RESET# is held at VIL but not within VSS ± 0.3 V, the standby current is greater.

RESET# may be tied to the system reset circuitry and thus, a system reset would also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

Output Disable (OE#)

When the OE# input is at VIH, output from the device is disabled. The outputs are placed in the high impedance state. (With the exception of RY/BY#.)

Secured Silicon Sector Flash Memory Region

The Secured Silicon Sector provides an extra Flash memory region. The Secured Silicon Sector is 128 words in length and all Secured Silicon reads outside of the 128-word address range returns invalid data. The Secured Silicon Sector Indicator Bit, DQ7, (at Autoselect address 03h) is used to indicate whether or not the Secured Silicon Sector is locked when shipped from the factory.
Please note the following general conditions:

- On power-up, or following a hardware reset, the device reverts to sending commands to the normal address space.
- Reads outside of sector SA0 return memory array data.
- Sector SA0 is remapped from memory array to Secured Silicon Sector array.
- Once the Secured Silicon Sector Entry Command is issued, the Secured Silicon Sector Exit command must be issued to exit Secured Silicon Sector Mode.
- The Secured Silicon Sector is not accessible when the device is executing an Embedded Program or Embedded Erase algorithm.
- When sector SA0 is suspended, if system enters Secured Silicon Sector mode, the Secured Silicon Sector Region cannot be read. If the system suspends the flash in other sectors except SA0, Secured Silicon Sector Region can be read normally.
- The ACC function is not available when the Secured Silicon Sector is enabled.

Table 8. Secured Silicon Sector Addresses

Secured Silicon Sector Address Range	
000000h-000007h	Reserve for Factory
000008h-00007Fh	Determined by customer

Customer Lockable Secured Silicon Sector

The Customer Lockable Secured Silicon Sector is always shipped unprotected (DQ0 set to "1"), allowing customers to utilize that sector in any manner they choose. If the security feature is not required, the Secured Silicon Sector can be treated as an additional Flash memory space.
Please note the following:

- Once the Secured Silicon Sector area is protected, the Secured Silicon Sector Indicator Bit (DQ0) is permanently set to "0."
- The Secured Silicon Sector can be read any number of times, but can be programmed and locked only once. The Secured Silicon Sector lock must be used with caution as once locked, there is no procedure available for unlocking the Secured Silicon Sector area and none of the bits in the Secured Silicon Sector memory space can be modified in any way.
- The accelerated programming (ACC) is not available when the Secured Silicon Sector is enabled.
- Once the Secured Silicon Sector is locked and verified, the system must write the Exit Secured Silicon Sector Region command sequence which return the device to the memory array at sector 0.
- The address 0h~7h in Secured Silicon Sector is reserved for Factory.

Secured Silicon Sector Entry/Exit Command Sequences

The system can access the Secured Silicon Sector region by issuing the three-cycle Enter Secured Silicon Sector command sequence. The device continues to access the Secured Silicon Sector region until the system issues the four-cycle Exit Secured Silicon Sector command sequence.

The Secured Silicon Sector Entry Command allows the following commands to be executed

- Read customer and factory Secured Silicon areas
- Program the customer Secured Silicon Sector

After the system has written the Enter Secured Silicon Sector command sequence, it may read the Secured Silicon Sector by using the addresses normally occupied by sector SA0 within the memory array. This mode of operation continues until the system issues the Exit Secured Silicon Sector command sequence, or until power is removed from the device.

COMMON FLASH INTERFACE (CFI)

The common flash interface (CFI) specification outlines device and host systems software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h in word mode (or address AAh in byte mode), any time the device is ready to read array data.

The system can read CFI information at the addresses given in Tables 9~11.In word mode, the upper address bits (A7–MSB) must be all zeros. To terminate reading CFI data, the system must write the reset command.
The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode and the system can read CFI data at the addresses given in Tables 9~11. The system must write the reset command to return the device to the autoselect mode.

Table 9. CFI Query Identification String

Addresses (Word Mode)	Data	Description
10h 11h 12h	0051h 0052h 0059h	Query Unique ASCII string “QRY”
13h 14h	0002h 0000h	Primary OEM Command Set
15h 16h	0040h 0000h	Address for Primary Extended Table
17h 18h	0000h 0000h	Alternate OEM Command set (00h = none exists)
19h 1Ah	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

Table 10. System Interface String

Addresses (Word Mode)	Data	Description
1Bh	0027h	Vcc Min (write/erase) DQ7-DQ4: volt, DQ3-DQ0: 100mV
1Ch	0036h	Vcc Max (write/erase) DQ7-DQ4: volt, DQ3-DQ0: 100mV
1Dh	0000h	Vpp Min voltage (00h = no Vpp pin present)
1Eh	0000h	Vpp Max voltage (00h = no Vpp pin present)
1Fh	0003h	Typical timeout per single byte/word write 2^N µs
20h	0004h	Typical timeout for min size buffer write 2^N µs (00h = not supported)
21h	0009h	Typical timeout per individual block erase 2^N ms
22h	0000h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	0005h	Max timeout for byte/word write 2^N times typical
24h	0005h	Max timeout for buffer write 2^N times typical
25h	0004h	Max timeout per individual block erase 2^N times typical
26h	0000h	Max timeout for full chip erase 2^N times typical (00h = not supported)

Table 11. Device Geometry Definition

Addresses (Word mode)	Data	Description
27h	0017h	Device Size = 2^N bytes. 2**23=8MB=64Mb
28h 29h	0002h 0000h	Flash Device Interface Description (refer to CFI publication 100); 01h = X16 only; 02h = x8/x16
2Ah 2Bh	0005h 0000h	Max number of byte in multi-byte write = 2^N (00h = not supported)
2Ch	0002h	Number of Erase Block Regions within device (01h = uniform device, 02h = boot device)
2Dh 2Eh 2Fh 30h	0007h 0000h 0020h 0000h	Erase Block Region 1 Information (refer to the CFI specification of CFI publication 100) EN29GL064A B and T : 0007h, 0000h, 0020h, 0000h
31h 32h 33h 34h	007Eh 0000h 0000h 0001h	Erase Block Region 2 Information (refer to the CFI specification of CFI publication 100) EN29GL064A B and T : 007Eh, 0000h, 0000h, 0001h
35h 36h 37h 38h	0000h 0000h 0000h 0000h	Erase Block Region 3 Information (refer to the CFI specification of CFI publication 100)
39h 3Ah 3Bh 3Ch	0000h 0000h 0000h 0000h	Erase Block Region 4 Information (refer to the CFI specification of CFI publication 100)

Table 12. Primary Vendor-specific Extended Query

Addresses (Word Mode)	Data	Description
40h	0050h	Query Unique ASCII string "PRI"
41h	0052h	
42h	0049h	
43h	0031h	Major version number, ASCII
44h	0034h	Minor version number, ASCII
45h	000Ch	Address Sensitive Unlock (Bits 1-0) 00 = Required, 01 = Not Required Technology (Bits 5-2) 0001 = 0.18um, 0010 = 0.13um, 0011 = 90nm
46h	0002h	Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	0001h	Sector Protect 0 = Not Supported, X = Minimum number of sectors per group
48h	0000h	Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	0003h	Sector Protect/Unprotect Scheme 00h = High Voltage Sector Protection 01h = High Voltage + In-System Sector Protection 02h = HV + In-System + Software Command Sector Protection 03h = Software Command Sector Protection
4Ah	0000h	Simultaneous Operation 00 = Not supported, X = Number of Sectors
4Bh	0000h	Burst Mode Type 00 = Not Supported, 01 = Supported

4Ch	0002h	Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page
4Dh	0085h	Minimum WP#/ACC (Acceleration) Supply Voltage 00 = Not Supported, DQ7-DQ4: Volts, DQ3=DQ0: 100mV
4Eh	0095h	Maximum WP#/ACC (Acceleration) Supply Voltage 00 = Not Supported, DQ7-DQ4: Volts, DQ3=DQ0: 100mV
4Fh	000xh	Top/Bottom Boot Sector Flag 02 = Bottom Boot Device, 03 = Top Boot Device
50h	0001h	Program Suspend 00 = Not Supported, 01 = Supported
52h	0008h	Secured Silicon Sector (Customer OTP Area) Size 2^N bytes
53h	000Fh	Hardware Reset Low Time-out during an embedded algorithm to read mode Maximum 2^N ns
54h	0009h	Hardware Reset Low Time-out not during an embedded algorithm to read mode Maximum 2^N ns
55h	0005h	Erase Suspend Latency Maximum 2^N µs
56h	0005h	Program Suspend Latency Maximum 2^N µs
57h	0000h	Bank Organization 00 = Data at 4Ah is zero, X = Number of Banks

Table 13. EN29GL064AT/B Command Definitions

Command Sequence			Cycles	Bus Cycles											
				1st Cycle		2nd Cycle		3rd Cycle		4th Cycle		5th Cycle		6th Cycle	
				Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read			1	RA	RD										
Reset			1	XXX	F0										
Autoselect	Manufacturer ID	Word	4	555	AA	2AA	55	555	90	000	7F				
										100	1C				
		Byte		AAA		555		AAA		000	7F				
										200	1C				
	Device ID Top Boot	Word	4	555	AA	2AA	55	555	90	X01	227E	X0E	2210	X0F	2201
		Byte		AAA		555		AAA		X02	7E	X1C	10	X1E	01
	Device ID Bottom Boot	Word	4	555	AA	2AA	55	555	90	X01	227E	X0E	2210	X0F	2200
		Byte		AAA		555		AAA		X02	7E	X1C	10	X1E	00
	Sector Protect Verify (note)	Word	4	555	AA	2AA	55	555	90	(SA) X02	00				
											01				
		Byte		AAA		555		AAA		(SA) X04	00				
											01				
Program		Word	4	555	AA	2AA	55	555	A0	PA	PD				
		Byte		AAA		555		AAA							
Write to Buffer		Word	6	555	AA	2AA	55	SA	25	SA	WC	PA	PD	WBL	PD
		Byte		AAA		555									
Program Buffer to Flash		Word	1	PA	29										
		Byte													
Write to Buffer Abort Reset		Word	3	555	AA	2AA	55	555	F0						
		Byte		AAA		555		555							
Chip Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
		Byte		AAA		555		AAA		AAA		555		AAA	
Sector Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
		Byte		AAA		555		AAA		AAA		555			
Erase/Program Suspend			1	XXX	B0										
Erase/Program Resume			1	XXX	30										
Secured Silicon Sector Entry			3	555	AA	2AA	55	555	88						
Secured Silicon Sector Exit			4	555	AA	2AA	55	555	90	XX	00				
CFI Query		Word	1	55	98										
		Byte		AA											
Accelerated Program			2	XX	A0	PA	PD								

Legend
X = Don't care
RA = Address of the memory to be read.
RD = Data read from location RA during read operation.
PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.
PD = Data to be programmed at location PA. Data latches on the rising edge of the WE# or CE# pulse, whichever happens first.
SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits Amax–A16 uniquely select any sector.
WBL = Write Buffer Location. The address must be within the same write buffer page as PA.
WC = Word Count is the number of write buffer locations to load minus 1 and maximum value is 31 for word and byte mode.

Note:
The data is 00h for an unprotected sector and 01h for a protected sector. This is same as PPB Status Read except that the protect and unprotect statuses are inverted here.

Table 14. EN29GL064AT/B Command Definitions

Command Sequence			Cycles	Bus Cycles											
				1st Cycle		2nd Cycle		3rd Cycle		4th Cycle		5th Cycle		6th Cycle	
				Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Lock Register	Command Set Entry	Word	3	555	AA	2AA	55	555	40						
		Byte	3	AAA	AA	55	55	AAA	40						
	Program		2	XXX	A0	XXX	Data								
	Read		1	00	RD										
	Command Set Exit		2	XXX	90	XXX	00								
Global Non-Volatile	PPB Command Set Entry	Word	3	555	AA	2AA	55	555	C0						
		Byte	3	AAA	AA	55	55	AAA	C0						
	PPB Program		2	XXX	A0	SA	00								
	All PPB Erase		2	XXX	80	00	30								
	PPB Status Read		1	SA	RD										
	PPB Command Set Exit		2	XXX	90	XXX	00								
Global Volatile Freeze	PPB Lock Command Set Entry	Word	3	555	AA	2AA	55	555	50						
		Byte	3	AAA	AA	555	55	AAA	50						
	PPB Lock Set (note)		2	XXX	A0	XXX	00								
	PPB Lock Status Read (note)		1	XXX	RD										
	PPB Lock Command Set Exit		2	XXX	90	XXX	00								
Volatile	DYB Command Set Entry	Word	3	555	AA	2AA	55	555	E0						
		Byte	3	AAA	AA	555	55	AAA	E0						
	DYB Set		2	XXX	A0	SA	00								
	DYB Clear		2	XXX	A0	SA	01								
	DYB Status Read		1	SA	RD										
	DYB Command Set Exit		2	XXX	90	XXX	00								

Legend
X = Don't care
RD(0) = Read data.
SA = Sector Address. Address bits Amax–A16 uniquely select any sector.
PWD = Password
PWDx = Password word0, word1, word2, and word3.
Data = Lock Register Contents: PD(0) = Secured Silicon Sector Protection Bit,
PD(1) = Persistent Protection Mode Lock Bit, PD(2) = Password Protection Mode Lock Bit.

Note:
Protected State = "00h," Unprotected State = "01h."

Table 15. DC Characteristics

(T_a = - 40°C to 85°C; V_{CC} = 2.7-3.6V)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	0V≤ V_{IN} ≤ Vcc				±5	µA
I_{LO}	Output Leakage Current	0V≤ V_{OUT} ≤ Vcc				±1	µA
I_{CC1}	V_{CC} Active Read Current	CE# = V_{IL}; OE# = V_{IH} ; V_{CC} = V_{CC} max	5MHz		15	30	mA
			10MHz		25	45	mA
I_{CC2}	V_{CC} Intra-Page Read Current	CE# = V_{IL} , OE# = V_{IH} , V_{CC} = V_{CC}max, f = 10 MHz			1	10	mA
		CE# = V_{IL} , OE# = V_{IH} , V_{CC} = V_{CC}max, f = 33 MHz			5	15	
I_{CC3}	V_{CC} Active Erase/ Program Current	CE# = V_{IL} , OE# = V_{IH} , V_{CC} = V_{CC}max			20	40	mA
I_{CC4}	V_{CC} Standby Current	CE#, RESET# = VCC ± 0.3 V, OE# = V_{IH} , V_{CC} = V_{CC} max V_{IL} = Vss + 0.3 V/-0.1V,			2.0	20	µA
I_{CC5}	V_{CC} Reset Current	RESET# = Vss ± 0.3V			2.0	20	µA
I_{CC6}	Automatic Sleep Mode	V_{IH} = Vcc ± 0.3V V_{IL} = Vss ± 0.3V			2.0	20	µA
I_{ACC}	ACC Accelerated Program Current	CE# = V_{IL}, OE# = V_{IH}, V_{CC} = V_{CC}max, WP#/ACC = V_{HH}	WP#/ACC pin		3	10	mA
			V_{CC} pin		15	30	
V_{IL}	Input Low Voltage			-0.5		0.3 x V_{CC}	V
V_{IH}	Input High Voltage			0.7 x V_{CC}		V_{CC} + 0.3	V
V_{HH}	Acceleration Program Voltage			8.5		9.5	V
V_{OL}	Output Low Voltage	I_{OL} = 100µA				0.15 x V_{CC}	V
V_{OH}	Output High Voltage CMOS	I_{OH} = -100µA		0.85 x V_{CC}			V
V_{LKO}	Supply voltage (Erase and Program lock-out)			2.3		2.5	V

Notes:
1. BYTE# pin can also be GND ± 0.3V. BYTE# and RESET# pin input buffers are always enabled so that they draw power if not at full CMOS supply voltages.
2. Maximum I_{CC} specifications are tested with Vcc = Vcc max.
3. Not 100% tested.

Figure 11. Test Conditions

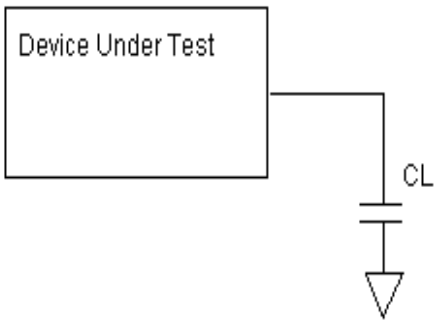


Table 16. Test Specifications

Test Conditions	-70	Unit
Output Load Capacitance, C_L	30	pF
Input Rise and Fall times	5	ns
Input Pulse Levels	0.0- VCC	V
Input timing measurement reference levels	0.5 VCC	V
Output timing measurement reference levels	0.5 VCC	V

AC CHARACTERISTICS

Table 17. Read-only Operations Characteristics

Parameter Symbols		Description		Test Setup		Speed	Unit
JEDEC	Standard					-70	
t_{AVAV}	t_{RC}	Read Cycle Time			Min	70	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		CE# = V_{IL} OE#= V_{IL}	Max	70	ns
t_{ELQV}	t_{CE}	Chip Enable To Output Delay		OE#= V_{IL}	Max	70	ns
	t_{PACC}	Page Access Time			Max	25	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	25	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z			Max	20	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z			Max	20	ns
t_{AXQX}	t_{OH}	Output Hold Time from Addresses, CE# or OE#, whichever occurs first			Min	0	ns
	t_{OEH}	Output Enable Hold Time	Read		Min	0	ns
			Toggle and DATA# Polling		Min	10	ns

Notes: High Z is Not 100% tested.

Figure 12. AC Waveforms for READ Operations

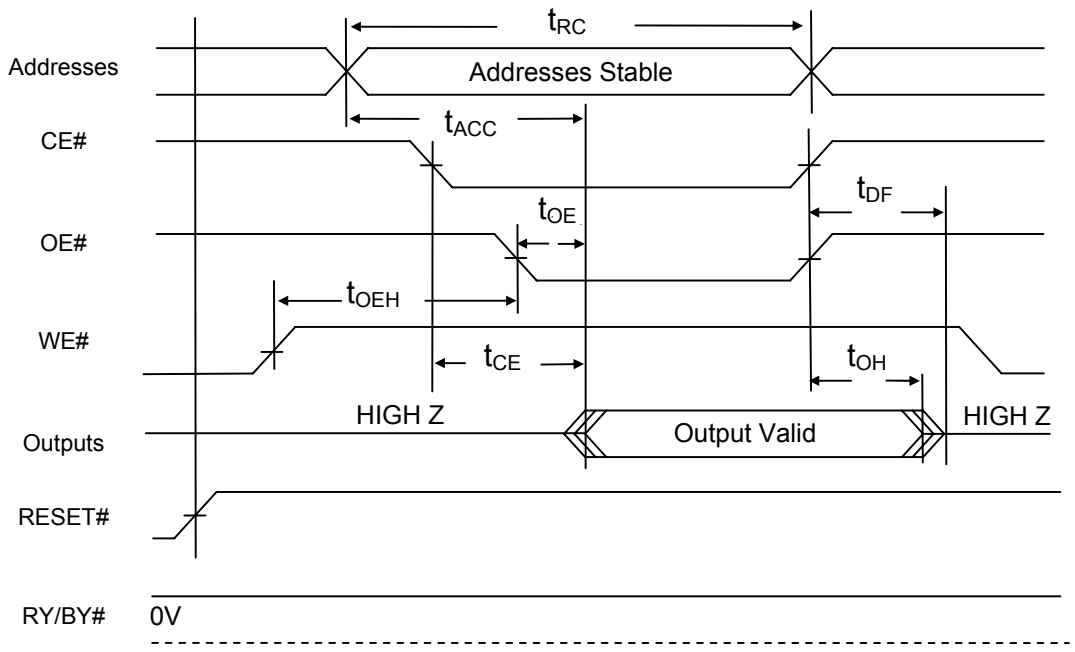
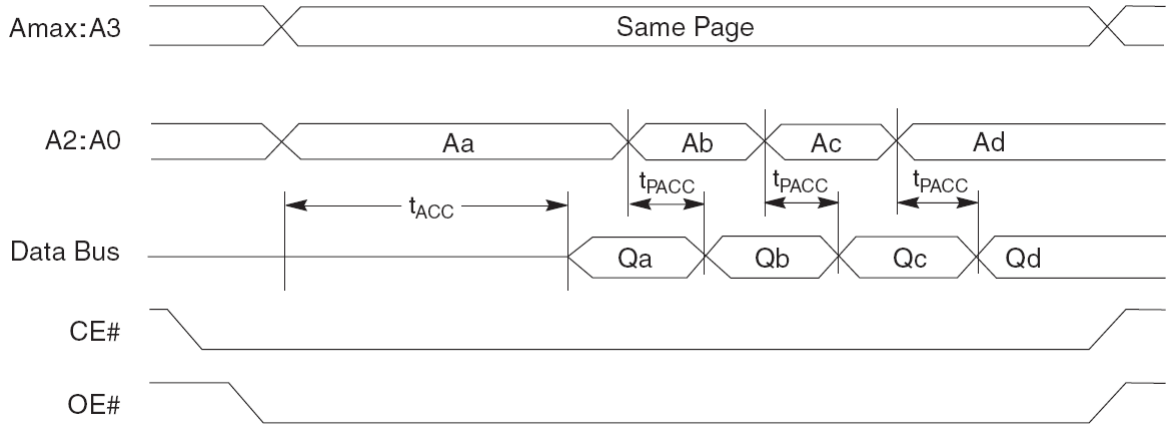


Figure 13. Page Read Operation Timings



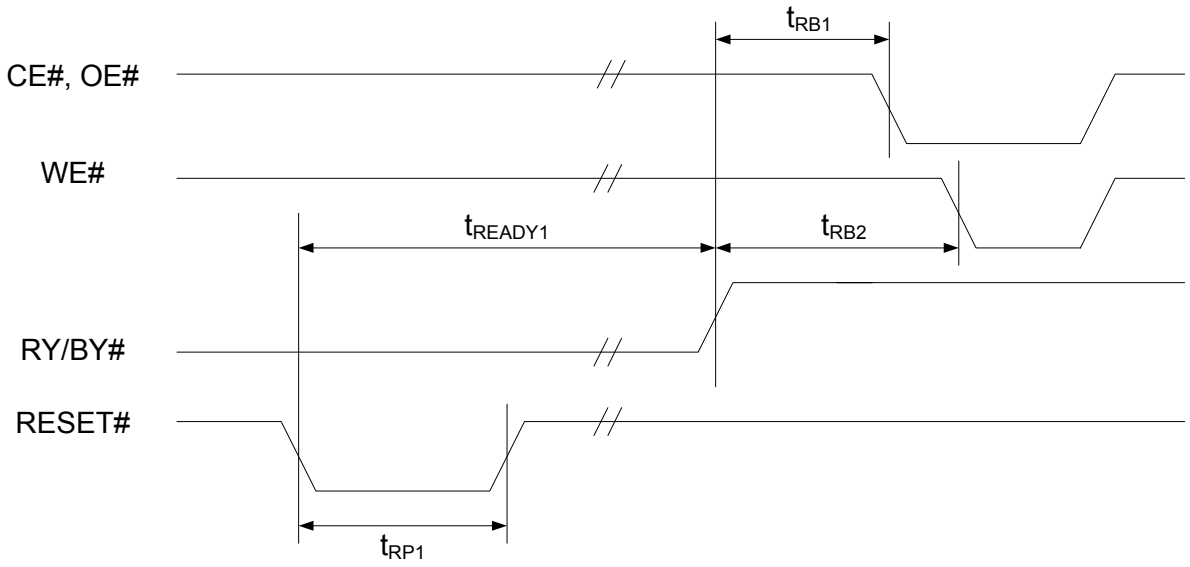
Note: Addresses are A2:A-1 for byte mode.

AC CHARACTERISTICS

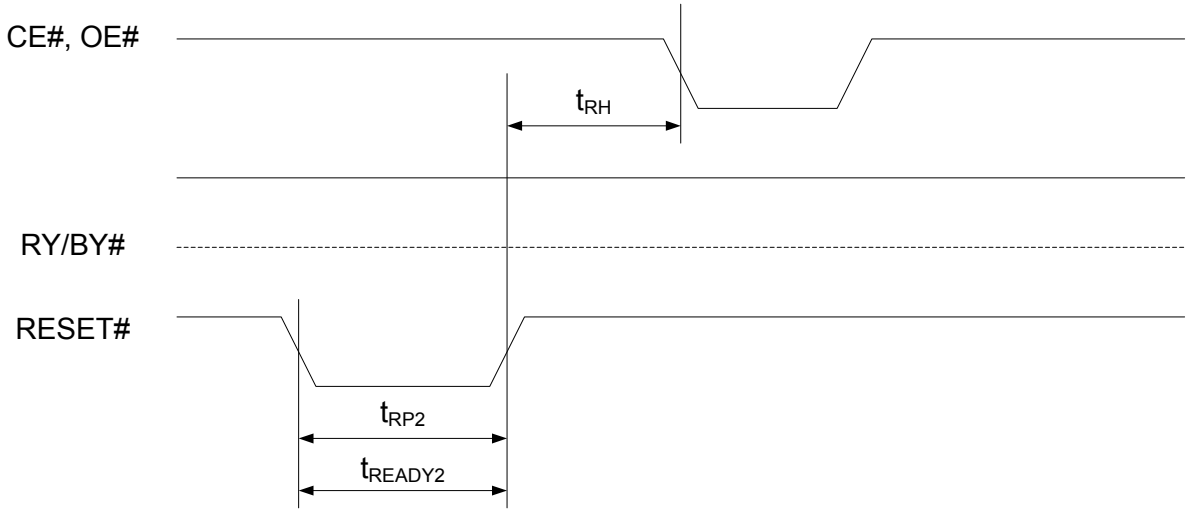
Table 18. Hardware Reset (RESET#)

Parameter Std	Description	Test Setup	Speed	Unit
			-70	
t_{RP1}	RESET# Pulse Width (During Embedded Algorithms)	Min	10	us
t_{RP2}	RESET# Pulse Width (NOT During Embedded Algorithms)	Min	500	ns
t_{RH}	Reset# High Time Before Read	Min	50	ns
t_{RB1}	RY/BY# Recovery Time (to CE#, OE# go low)	Min	0	ns
t_{RB2}	RY/BY# Recovery Time (to WE# go low)	Min	50	ns
t_{READY1}	Reset# Pin Low (During Embedded Algorithms) to Read or Write	Max	20	us
t_{READY2}	Reset# Pin Low (NOT During Embedded Algorithms) to Read or Write	Max	500	ns

Figure 14. AC Waveforms for RESET#
Reset# Timings



Reset Timing during Embedded Algorithms



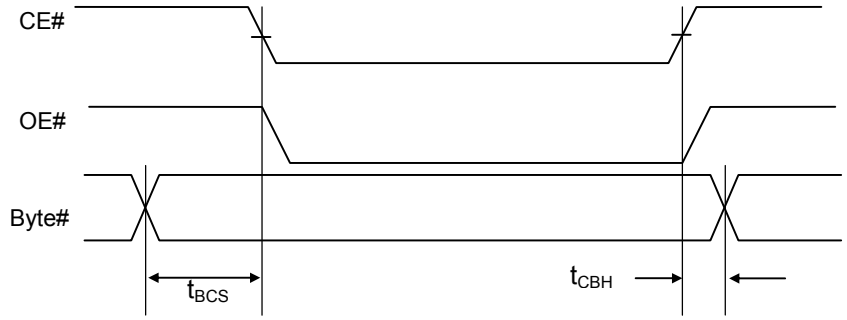
Reset Timing NOT during Embedded Algorithms

AC CHARACTERISTICS

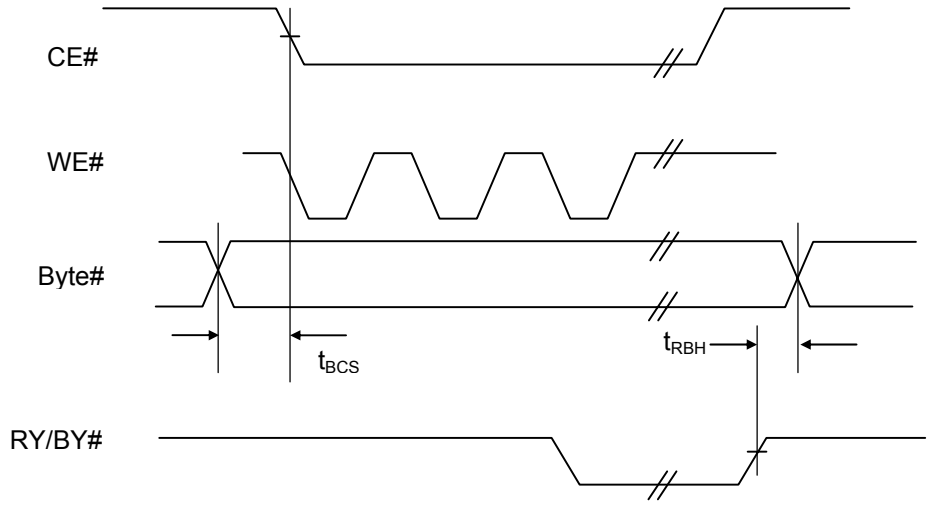
Table 19. Word / Byte Configuration (BYTE#)

Std Parameter	Description	Test Setup	Speed	Unit
			-70	
t_{BCS}	Byte# to CE# switching setup time	Min	0	ns
t_{CBH}	CE# to Byte# switching hold time	Min	0	ns
t_{RBH}	RY/BY# to Byte# switching hold time	Min	0	ns

Figure 15. AC Waveforms for BYTE#



Byte# timings for Read Operations



Byte #timings for Write Operations

Note: Switching BYTE# pin not allowed during embedded operations

AC CHARACTERISTICS

Table 20. Write (Erase/Program) Operations

Parameter Symbols		Description			Speed	Unit
JEDEC	Standard				-70	
t_{AVAV}	t_{WC}	Write Cycle Time		Min	70	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0	ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	45	ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	30	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0	ns
	t_{OEH}	Output Enable Hold Time	Read	MIn	0	ns
			Toggle and DATA# Polling	Min	10	ns
t_{GHWL}	t_{GHWL}	Read Recovery Time before Write (OE# High to WE# Low)		Min	0	ns
t_{ELWL}	t_{CS}	CE# SetupTime		Min	0	ns
t_{WHEH}	t_{CH}	CE# Hold Time		Min	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	35	ns
t_{WHDL}	t_{WPH}	Write Pulse Width High		Min	20	ns
t_{WHWH1}	t_{WHWH1}	Write Buffer Program Operation (Note 2, 3)		Typ	100	µs
		Programming Operation (Word AND Byte Mode)		Typ	8	µs
				Max	200	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation		Typ	0.1	s
				Max	2	s
		Chip Erase Operation		Typ	16	s
	t_{VHH}	V_{HH} Rise and Fall Time		Min	250	ns
	t_{VCS}	Vcc Setup Time		Min	50	µs
	t_{BUSY}	WE# High to RY/BY# Low		Max	70	ns
	t_{RB}	Recovery Time from RY/BY#		Min	0	ns

Notes: 1. Not 100% tested.
2. See table.22 Erase and Programming Performance for more information.
3. For 1~16 words bytes programmed.

AC CHARACTERISTICS

Table 21. Write (Erase/Program) Operations

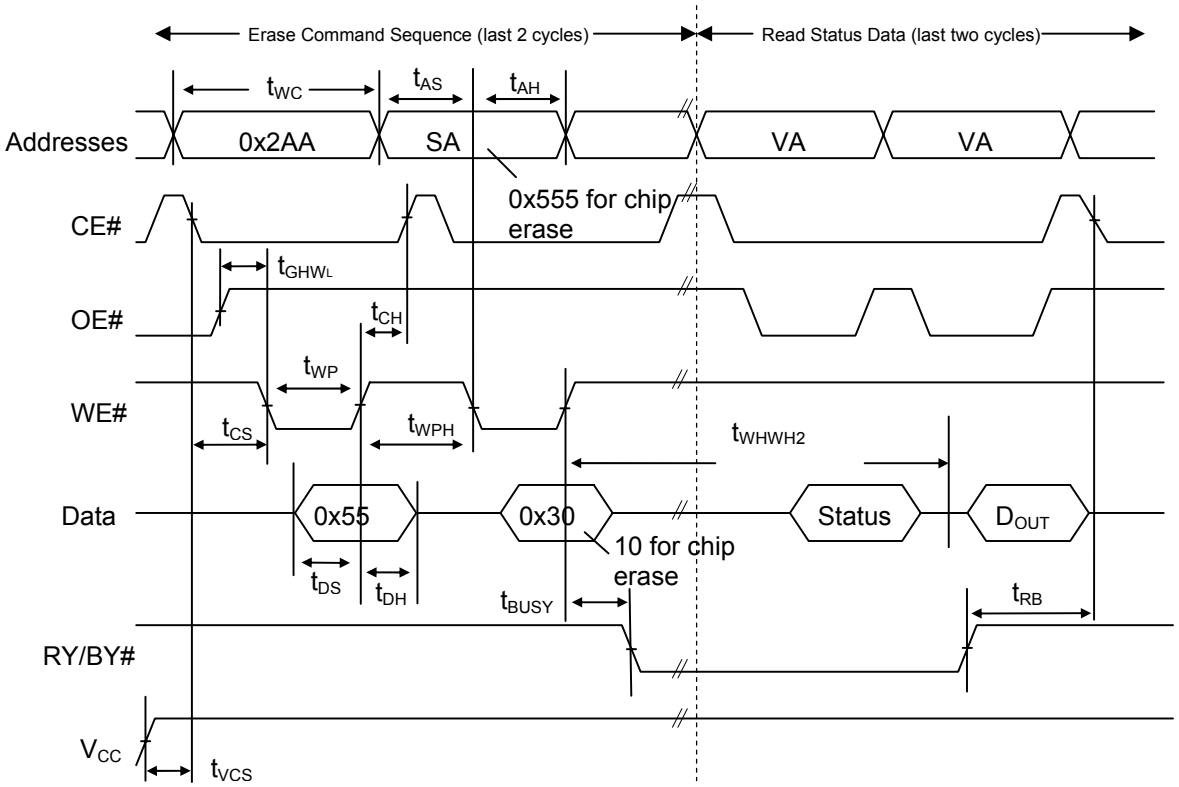
Alternate CE# Controlled Writes

Parameter Symbols		Description		Speed	Unit
JEDEC	Standard			-70	
t_{AVAV}	t_{WC}	Write Cycle Time	Min	70	ns
t_{AVEL}	t_{AS}	Address Setup Time	Min	0	ns
t_{ELAX}	t_{AH}	Address Hold Time	Min	45	ns
t_{DVEH}	t_{DS}	Data Setup Time	Min	30	ns
t_{EHDX}	t_{DH}	Data Hold Time	Min	0	ns
t_{GHEL}	t_{GHEL}	Read Recovery Time before Write (OE# High to CE# Low)	Min	0	ns
t_{WLEL}	t_{WS}	WE# SetupTime	Min	0	ns
t_{EHWH}	t_{WH}	WE# Hold Time	Min	0	ns
t_{ELEH}	t_{CP}	Write Pulse Width	Min	35	ns
t_{EHEL}	t_{CPH}	Write Pulse Width High	Min	20	ns
t_{WHWH1}	t_{WHWH1}	Write Buffer Program Operation (Note 2, 3)	Typ	100	µs
		Programming Operation (Byte AND word mode)	Typ	8	µs
			Max	200	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation	Typ	0.1	s
			Max	2	s

Notes: 1. Not 100% tested.
2. See table.22 Erase and Programming Performance for more information.
3. For 1~16 words bytes programmed.

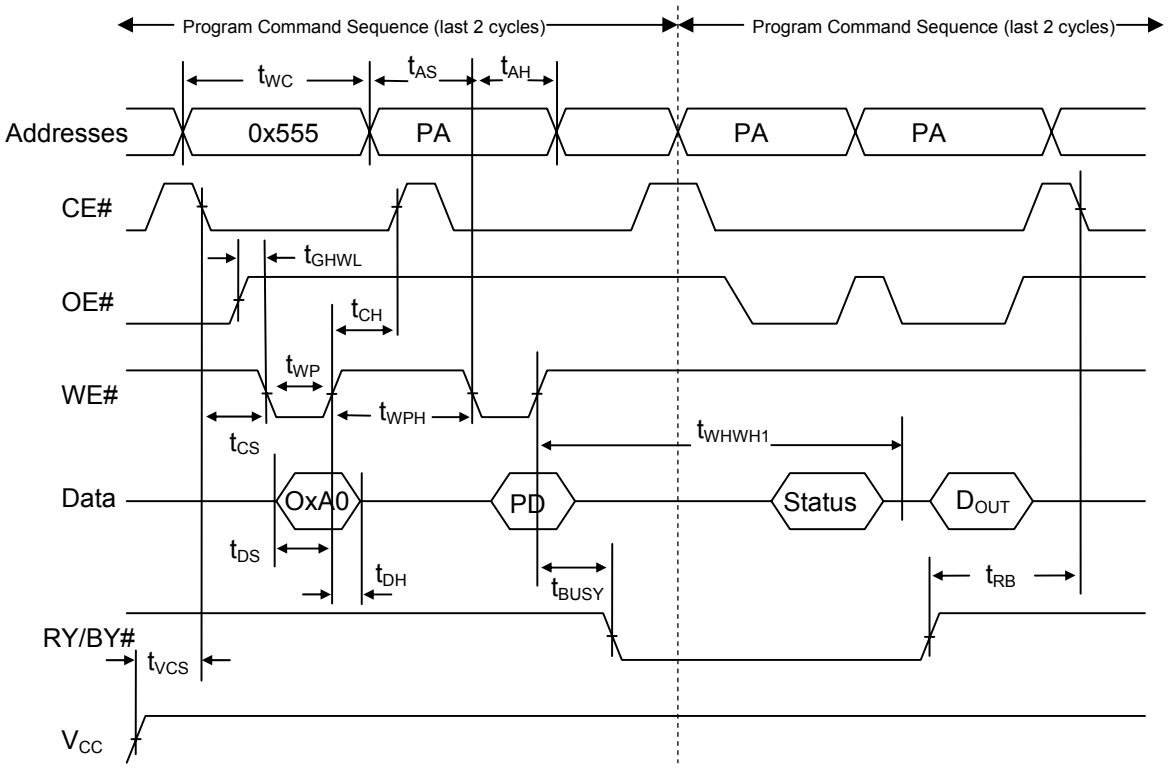
AC CHARACTERISTICS

Figure 16. AC Waveforms for Chip/Sector Erase Operations Timings



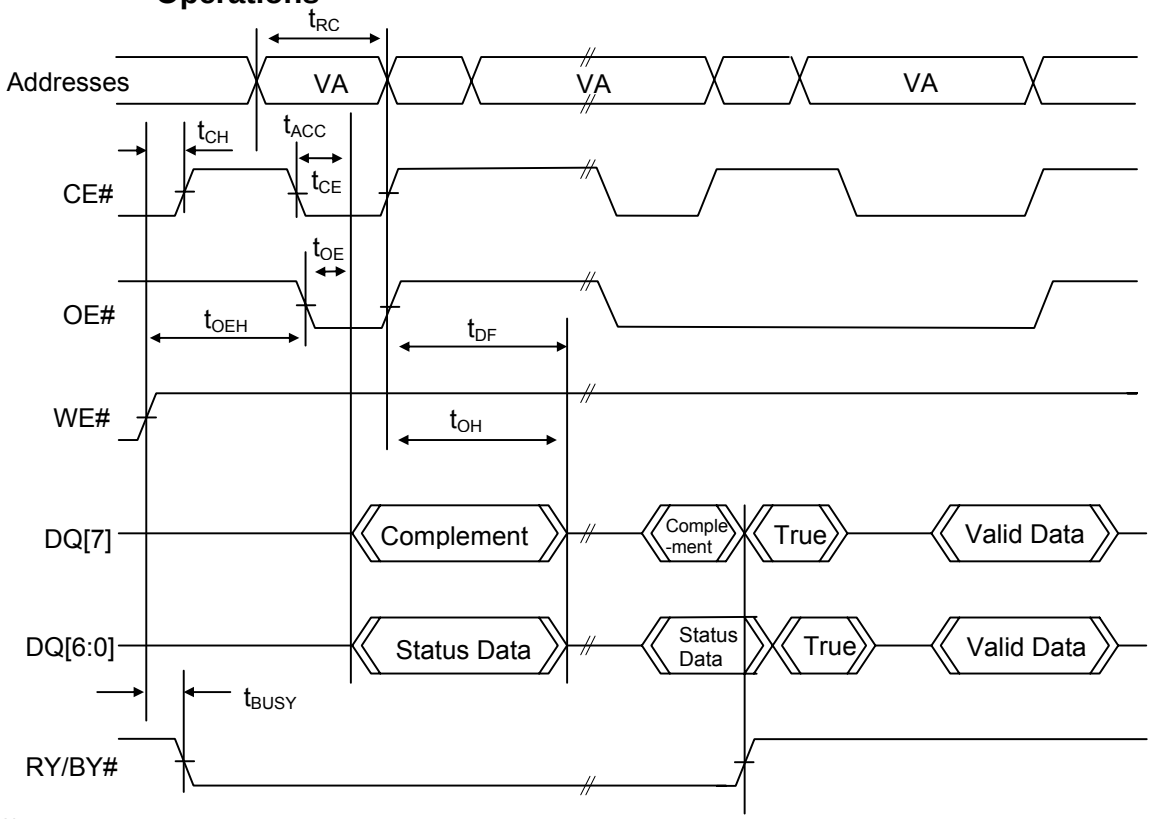
Notes:
1. SA=Sector Address (for sector erase), VA=Valid Address for reading status, D_{out}=true data at read address.
2. V_{cc} shown only to illustrate t_{vcs} measurement references. It cannot occur as shown during a valid command sequence.

Figure 17. Program Operation Timings



Notes:
1. PA=Program Address, PD=Program Data, D_{OUT} is the true data at the program address.
2. V_{CC} shown in order to illustrate t_{VCS} measurement references. It cannot occur as shown during a valid command sequence.

Figure 18. AC Waveforms for /DATA Polling During Embedded Algorithm Operations



Notes:
1. VA=Valid Address for reading Data# Polling status data
2. This diagram shows the first status cycle after the command sequence, the last status read cycle and the array data read cycle.

Figure 19. AC Waveforms for Toggle Bit During Embedded Algorithm Operations

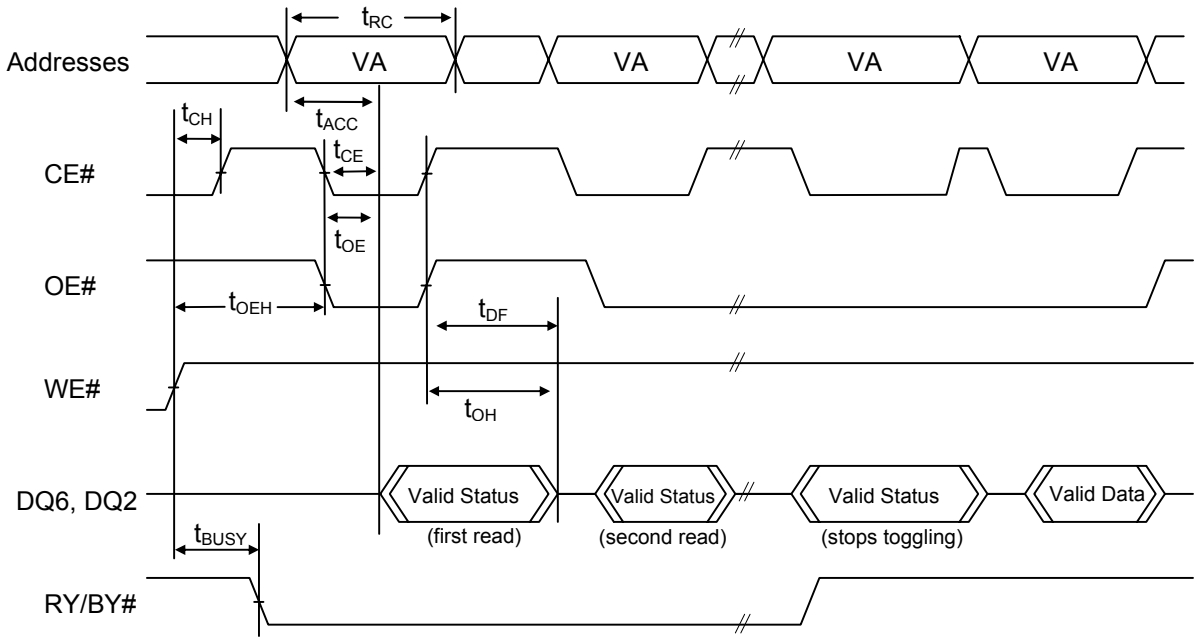
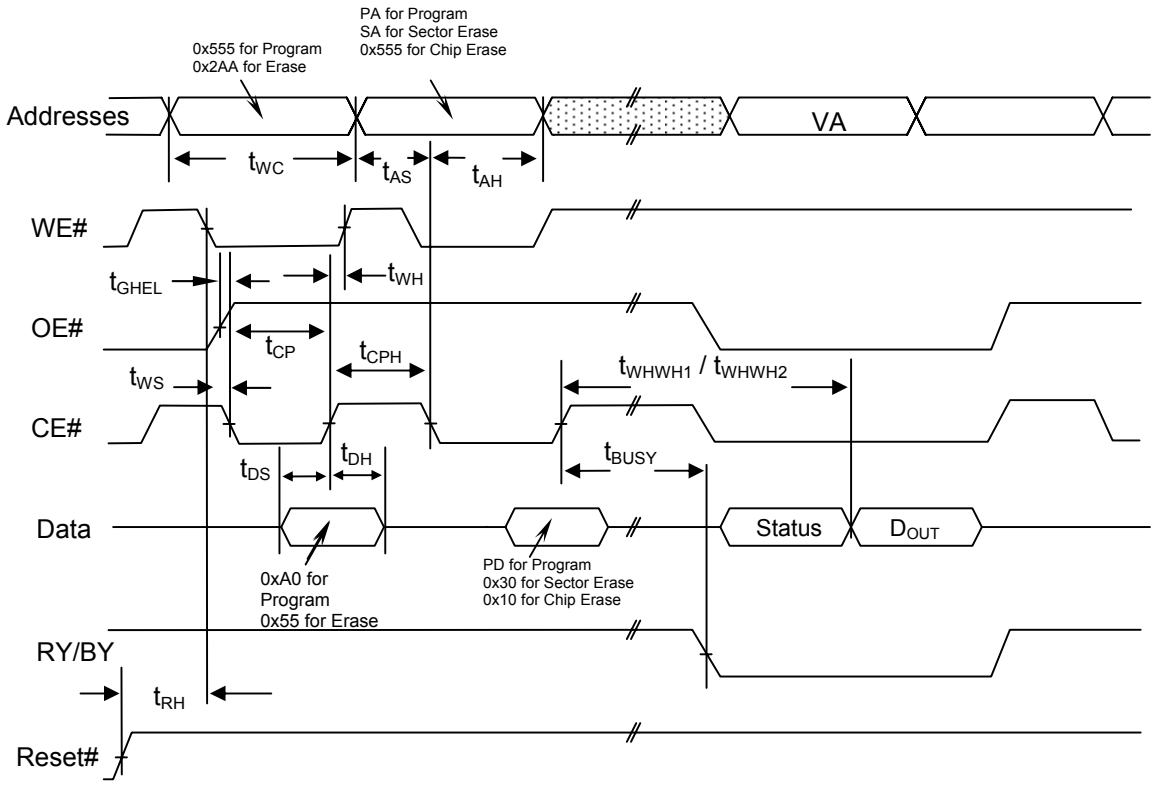


Figure 20. Alternate CE# Controlled Write Operation Timings



Notes:

PA = address of the memory location to be programmed.
PD = data to be programmed at byte address.
VA = Valid Address for reading program or erase status
D_{out} = array data read at VA
Shown above are the last two cycles of the program or erase command sequence and the last status read cycle
Reset# shown to illustrate t_{RH} measurement references. It cannot occur as shown during a valid command sequence.

Figure 21. DQ2 vs. DQ6

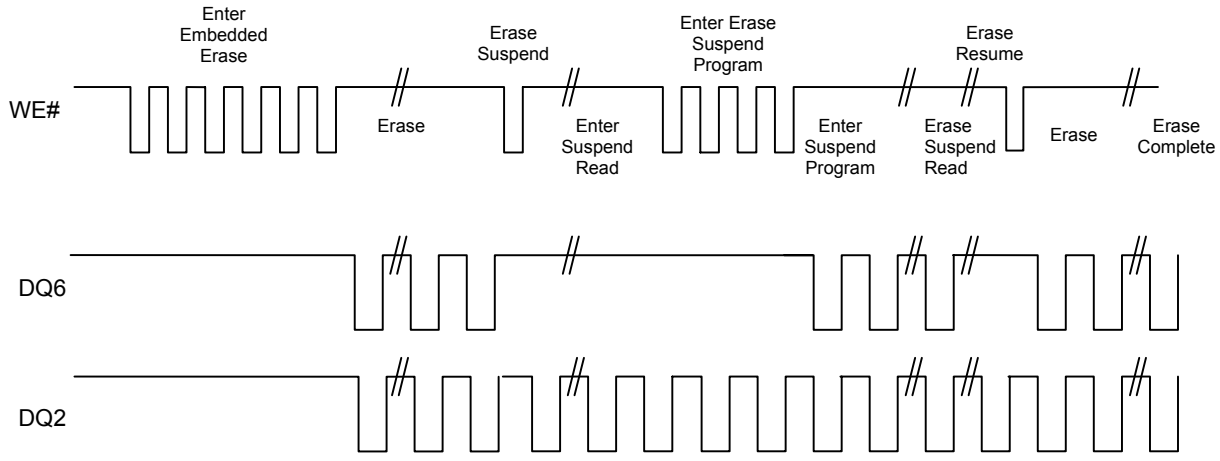


TABLE 22. ERASE AND PROGRAMMING PERFORMANCE

Parameter		Limits			Comments
		Typ	Max	Unit	
Sector Erase Time		0.1	2	sec	Excludes 00h programming prior to erasure
Chip Erase Time		16	60	sec	
Byte Programming Time		8	200	µs	Excludes system level overhead
Word Programming Time		8	200	µs	
Chip Programming Time	Byte	67.2	201.6	sec	
	Word	33.6	100.8		
Total Write Buffer time		100		µs	
ACC Total Write Buffer time		60			
Erase/Program Endurance		100K		cycles	Minimum 100K cycles

Notes:
1. Typical program and erase times assume the following conditions: room temperature, 3V and check board pattern programmed.
2. Maximum program and erase times assume the following conditions: worst case Vcc, 90°C and 100,000 cycles.

Table 23. 48-PIN TSOP AND BGA PACKAGE CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Package	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	TSOP	6	7.5	pF
			BGA	1.2	1.2	
C_{OUT}	Output Capacitance	V_{OUT} = 0	TSOP	8.5	12	pF
			BGA	1.1	1.2	
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	TSOP	7.5	9	pF
			BGA	1.0	1.3	

Note: Test conditions are Temperature = 25°C and f = 1.0 MHz.

Table 24. DATA RETENTION

Parameter Description	Test Conditions	Min	Unit
Data Retention Time	150°C	10	Years
	125°C	20	Years

ABSOLUTE MAXIMUM RATINGS

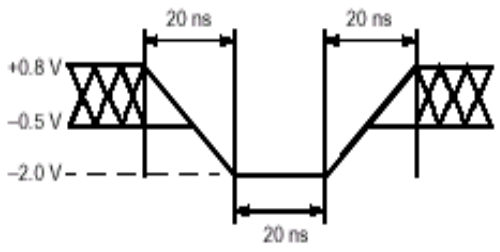
Parameter		Value	Unit
Storage Temperature		-65 to +150	°C
Plastic Packages		-65 to +125	°C
Ambient Temperature With Power Applied		-55 to +125	°C
Output Short Circuit Current[1]		200	mA
Voltage with Respect to Ground	OE#, RESET# and WP#/ACC[2]	-0.5 to + 9.5	V
	All other pins [3]	-0.5 to Vcc+0.5	V
	Vcc	-0.5 to + 4.0	V

Notes:
1. No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.
2. Minimum DC input voltage on OE#, RESET# and WP#/ACC pins is –0.5V. During voltage transitions, OE#, RESET# and WP#/ACC pins may undershoot V_{ss} to –1.0V for periods of up to 50ns and to –2.0V for periods of up to 20ns. See figure below. Maximum DC input voltage on OE#, and RESET# is 8.5V which may overshoot to 9.5V for periods up to 20ns.
3. Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may undershoot V_{ss} to –1.0V for periods of up to 50ns and to –2.0 V for periods of up to 20ns. See figure below. Maximum DC voltage on output and I/O pins is V_{cc} + 0.5 V. During voltage transitions, outputs may overshoot to V_{cc} + 1.5 V for periods up to 20ns. See figure below.
4. Stresses above the values so mentioned above may cause permanent damage to the device. These values are for a stress rating only and do not imply that the device should be operated at conditions up to or above these values. Exposure of the device to the maximum rating values for extended periods of time may adversely affect the device reliability.

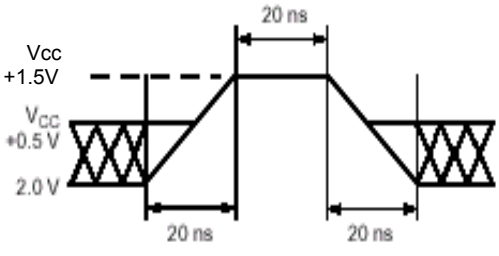
RECOMMENDED OPERATING RANGES[1]

Parameter	Value	Unit
Ambient Operating Temperature Industrial Devices	-40 to 85	°C
Operating Supply Voltage Vcc	Full Voltage Range: 2.7 to 3.6V	V

1. Recommended Operating Ranges define those limits between which the functionality of the device is guaranteed.

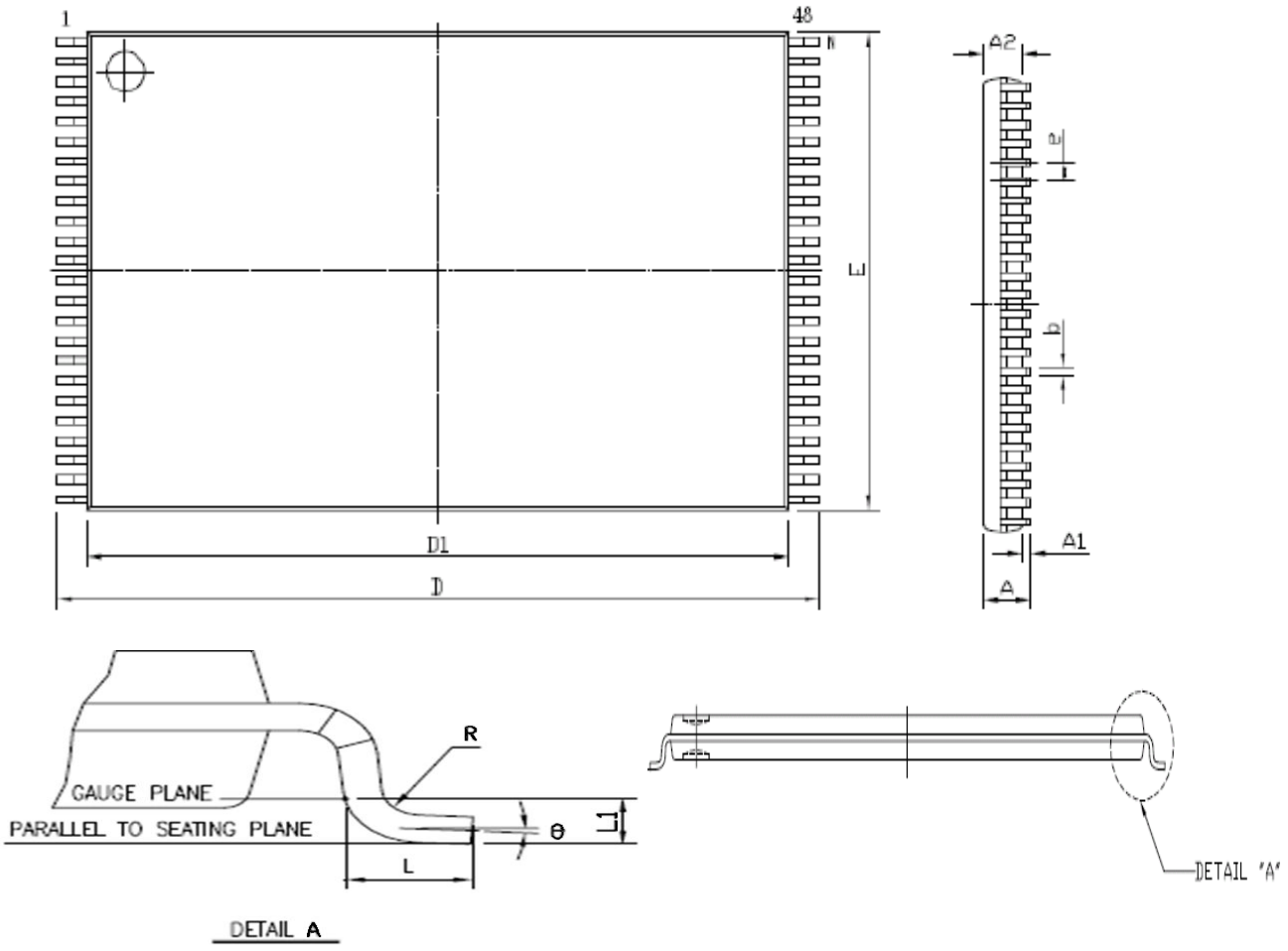


Maximum Negative Overshoot Waveform



Maximum Positive Overshoot Waveform

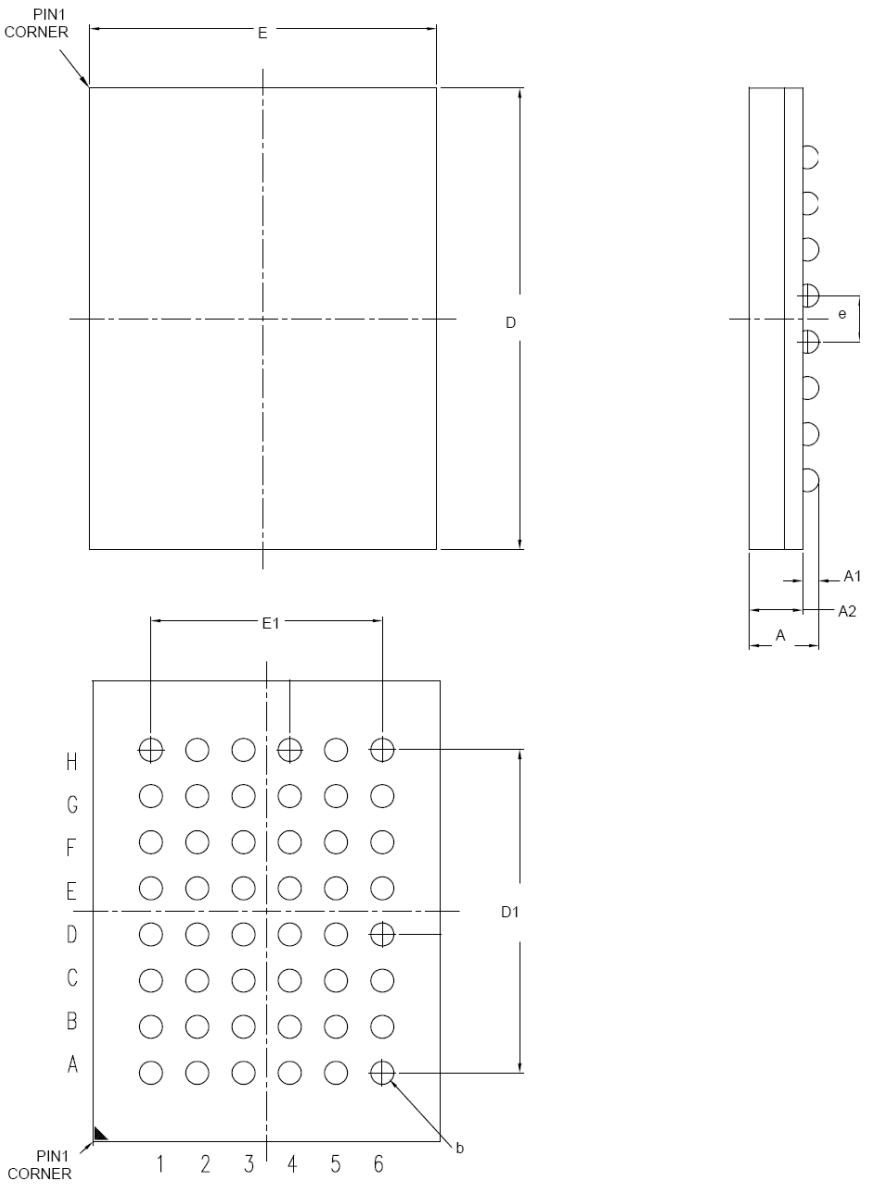
FIGURE 22. 48L TSOP 12mm x 20mm package outline



SYMBOL	DIMENSION IN MM		
	MIN.	NOR	MAX
A	- - -	- - -	1.20
A1	0.05	- - -	0.15
A2	0.95	1.00	1.05
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	11.9	12.00	12.10
e	- - -	0.50	- - -
b	0.17	0.22	0.27
L	0.5	0.60	0.70
L1	- - -	0.25	- - -
R	0.08	- - -	0.20
θ	0^0	3^0	5^0

Note : 1. Coplanarity: 0.1 mm
2. Max. allowable mold flash is 0.15 mm at the pkg ends, 0.25 mm between leads.

FIGURE 23. 48L TFBGA 6mm x 8mm package outline



SYMBOL	DIMENSION IN MM		
	MIN.	NOR	MAX
A	- - -	- - -	1.30
A1	0.23	0.29	- - -
A2	0.84	0.91	- - -
D	7.90	8.00	8.10
E	5.90	6.00	6.10
D1	- - -	5.60	- - -
E1	- - -	4.00	- - -
e	- - -	0.80	- - -
b	0.35	0.40	0.45

Note : 1. Coplanarity: 0.1 mm

Purpose

Eon Silicon Solution Inc. (hereinafter called “Eon”) is going to provide its products’ top marking on ICs with < cFeon > from January 1st, 2009, and without any change of the part number and the compositions of the ICs. Eon is still keeping the promise of quality for all the products with the same as that of Eon delivered before. Please be advised with the change and appreciate your kindly cooperation and fully support Eon’s product family.

Eon products’ Top Marking

cFeon

cFeon Top Marking Example:

cFeon

Part Number: XXXX-XXX
Lot Number: XXXXX
Date Code: XXXXX

For More Information

Please contact your local sales office for additional information about Eon memory solutions.

ORDERING INFORMATION

EN29GL064A T - 70 T I P

PACKAGING CONTENT
P = RoHS compliant

TEMPERATURE RANGE
I = Industrial (-40°C to +85°C)

PACKAGE
T = 48-pin TSOP
B = 48-Ball Thin Profile Fine Pitch Ball Grid Array (TFBGA) 0.80mm pitch, 6mm x 8mm package

SPEED
70 = 70ns

BOOT CODE SECTOR ARCHITECTURE
T = Top boot Sector
B = Bottom boot Sector

BASE PART NUMBER
EN = Eon Silicon Solution Inc.
29GL = FLASH, 3V Page Mode Flash Memory
064 = 64 Megabit (8M x 8 / 4M x 16)
A = version identifier

Revisions List

Revision No	Description	Date
A	Initial Release	2010/12/24
B	Remove V_{IO} function.	2011/04/12
C	1. Add Table 6 “Note 3. If user needs the product of DQ3 = 0, please chose the EN29GA064AT/B. For the detail information of EN29GA064AT/B please contact with Eon directly” on page 27. 2. Update Table 23. 48-PIN TSOP AND BGA PACKAGE CAPACITANCE on page 52.	2011/12/01