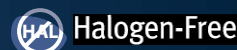


EPC2019 – Enhancement Mode Power Transistor

 V_{DS} , 200 V $R_{DS(on)}$, 50 m Ω I_D , 8.5 A

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR} . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Maximum Ratings			
PARAMETER		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	200	V
I_D	Continuous ($T_A = 25^\circ\text{C}$, $R_{\theta JA} = 18^\circ\text{C/W}$)	8.5	A
	Pulsed (25°C , $T_{PULSE} = 300 \mu\text{s}$)	42	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	$^\circ\text{C}$
T_{STG}	Storage Temperature	-40 to 150	

Thermal Characteristics			
PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	2.7	$^\circ\text{C/W}$
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	7.5	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	72	

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

Static Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	$V_{GS} = 0 \text{ V}$, $I_D = 125 \mu\text{A}$	200			V
I_{DSS}	Drain-Source Leakage	$V_{GS} = 0 \text{ V}$, $V_{DS} = 160 \text{ V}$		20	100	μA
I_{GSS}	Gate-to-Source Forward Leakage	$V_{GS} = 5 \text{ V}$		0.8	2.5	mA
	Gate-to-Source Reverse Leakage	$V_{GS} = -4 \text{ V}$		20	100	μA
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 1.5 \text{ mA}$	0.8	1.4	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	$V_{GS} = 5 \text{ V}$, $I_D = 7 \text{ A}$		36	50	m Ω
V_{SD}	Source-Drain Forward Voltage	$I_S = 0.5 \text{ A}$, $V_{GS} = 0 \text{ V}$		1.8		V

All measurements were done with substrate connected to source.



EPC2019 eGaN® FETs are supplied only in passivated die form with solder bars

Applications

- High Speed DC-DC conversion
- Class-D Audio
- High Frequency Hard-Switching and Soft-Switching Circuits

Benefits

- Ultra High Efficiency
- Ultra Low $R_{DS(on)}$
- Ultra Low Q_G
- Ultra Small Footprint



Dynamic Characteristics ($T_j = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	$V_{GS} = 100\text{ V}, V_{DS} = 0\text{ V}$		200	270	pF
C_{OSS}	Output Capacitance			110	150	
C_{RSS}	Reverse Transfer Capacitance			0.7	1	
R_G	Gate Resistance			0.4		Ω
Q_G	Total Gate Charge	$V_{DS} = 100\text{ V}, V_{GS} = 5\text{ V}, I_D = 7\text{ A}$		1.8	2.5	nC
Q_{GS}	Gate-to-Source Charge	$V_{DS} = 100\text{ V}, I_D = 7\text{ A}$		0.6		
Q_{GD}	Gate-to-Drain Charge			0.35	0.6	
$Q_{G(TH)}$	Gate Charge at Threshold			0.4		
Q_{OSS}	Output Charge	$V_{DS} = 100\text{ V}, V_{DS} = 0\text{ V}$		18	23	
Q_{RR}	Source-Drain Recovery Charge			0		

All measurements were done with substrate connected to source.

Figure 1: Typical Output Characteristics at 25°C

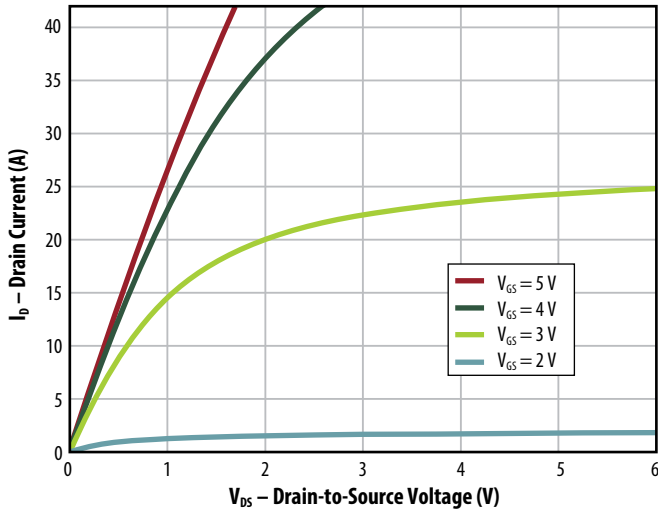


Figure 2: Transfer Characteristics

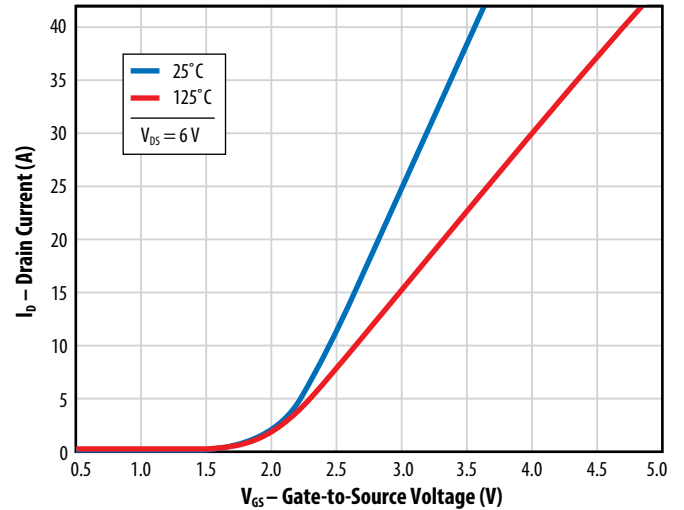


Figure 3: $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

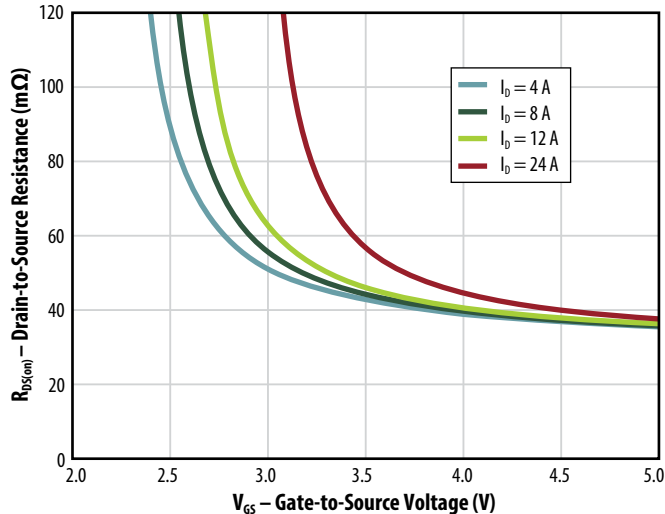


Figure 4: $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

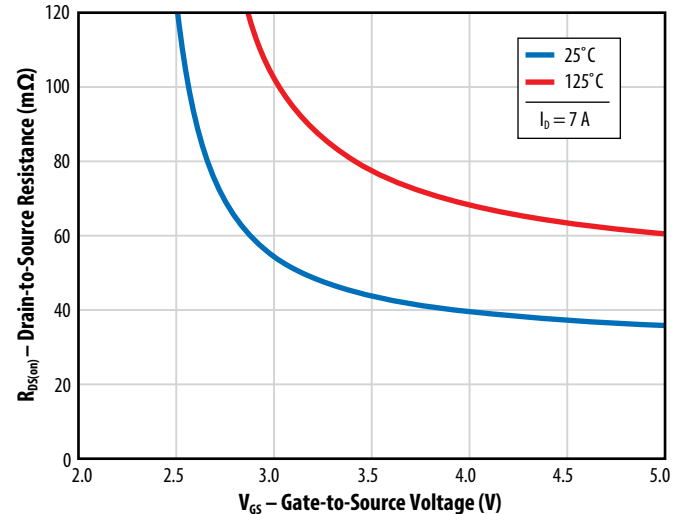


Figure 5a: Capacitance (Linear Scale)

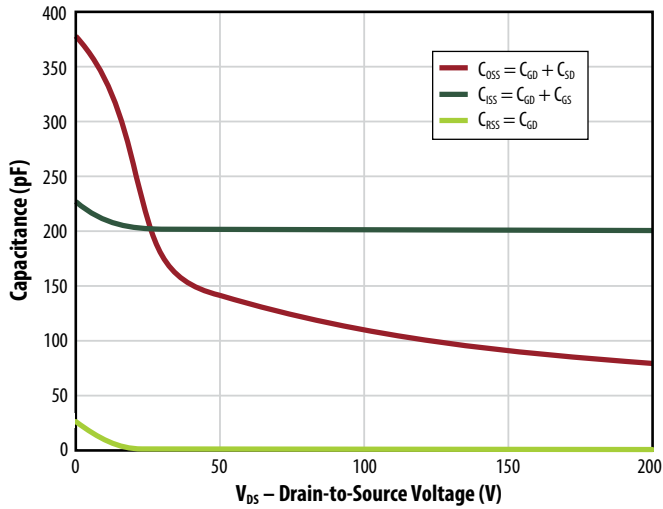


Figure 5b: Capacitance (Log Scale)

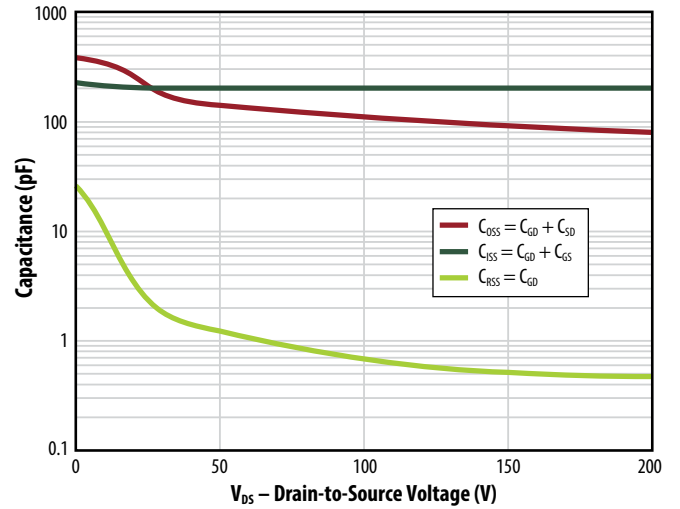


Figure 6: Gate Charge

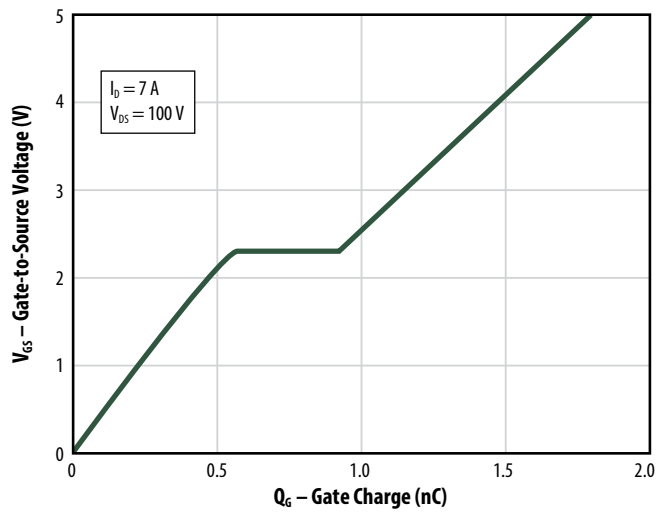


Figure 7: Reverse Drain-Source Characteristics

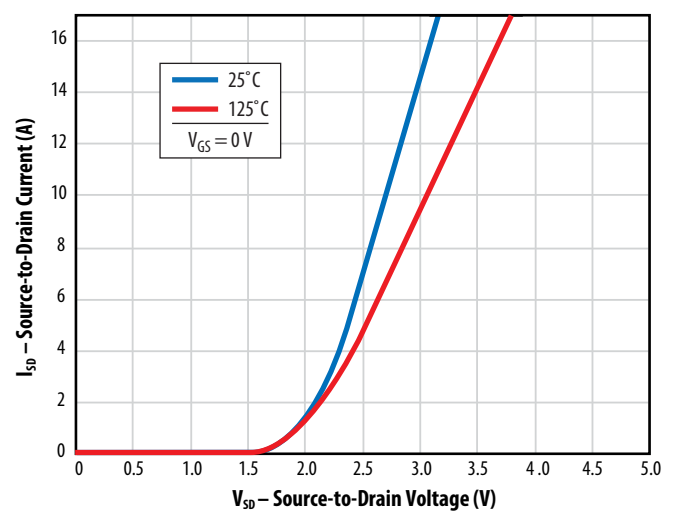


Figure 8: Normalized On-State Resistance vs. Temperature

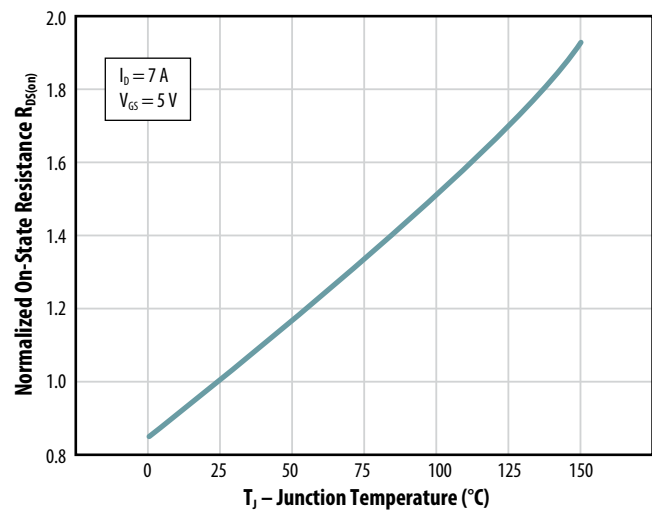
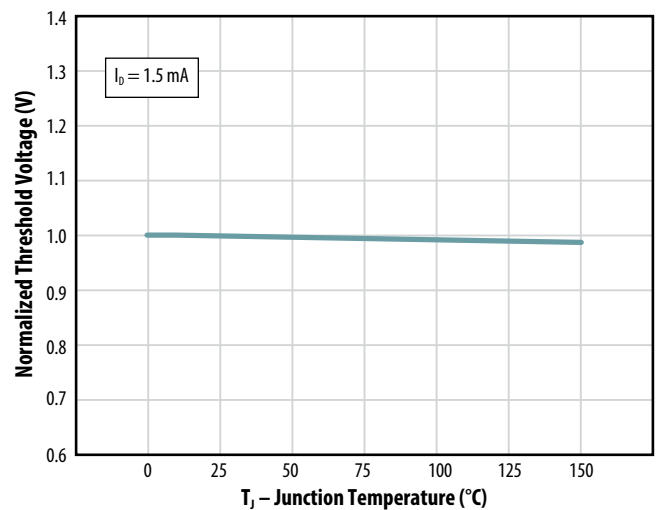


Figure 9: Normalized Threshold Voltage vs. Temperature



All measurements were done with substrate shorted to source.

Figure 10: Gate Leakage Current

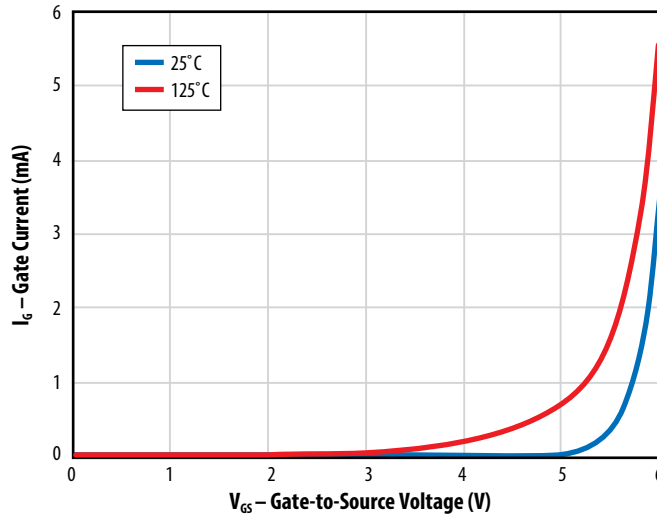


Figure 11: Transient Thermal Response Curves

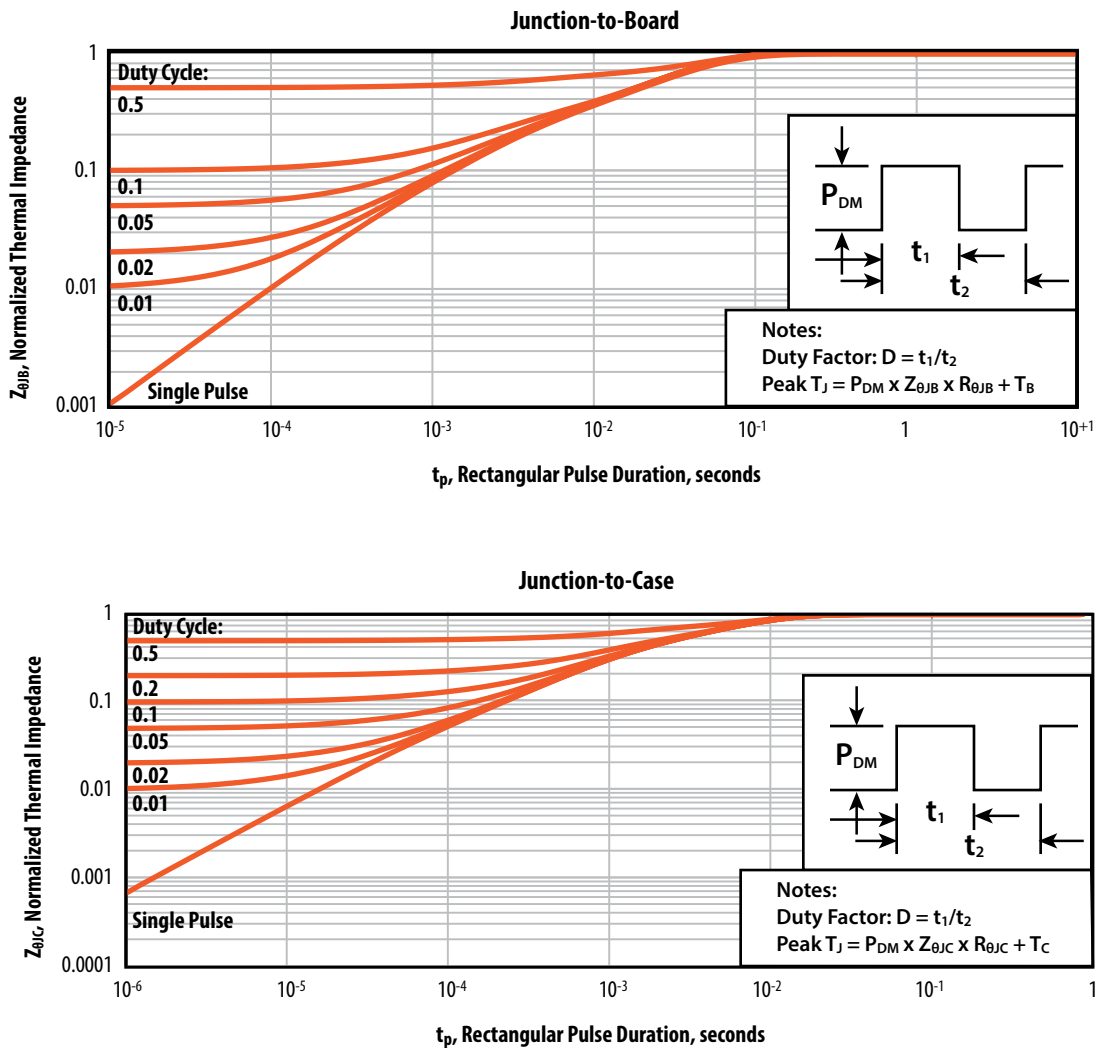
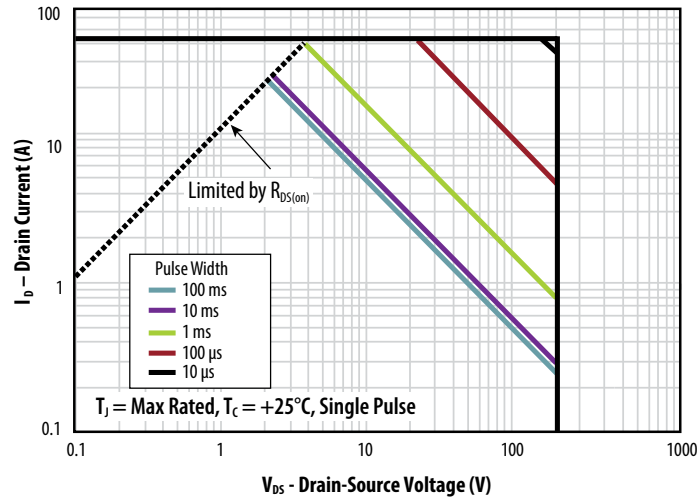
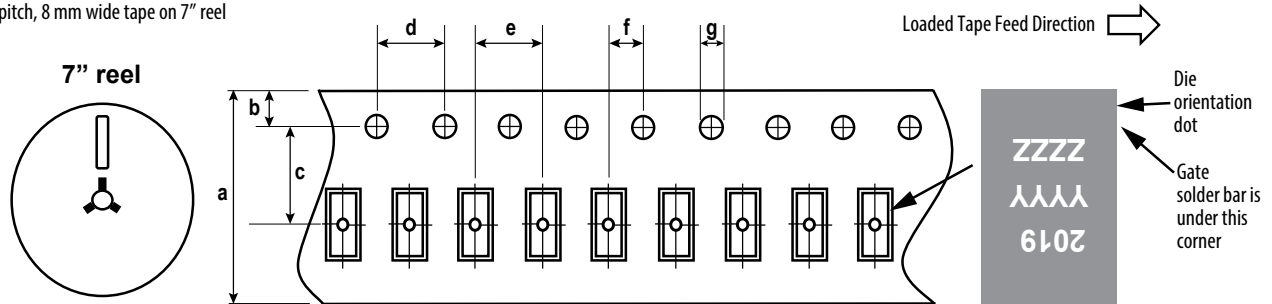


Figure 12: Safe Operating Area



TAPE AND REEL CONFIGURATION

4 mm pitch, 8 mm wide tape on 7" reel

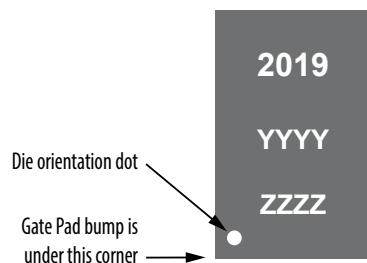


Die is placed into pocket solder bar side down (face side down)

EPC2019 (note 1)			
Dimension (mm)	target	min	max
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (see note)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (see note)	2.00	1.95	2.05
g	1.5	1.5	1.6

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.
 Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

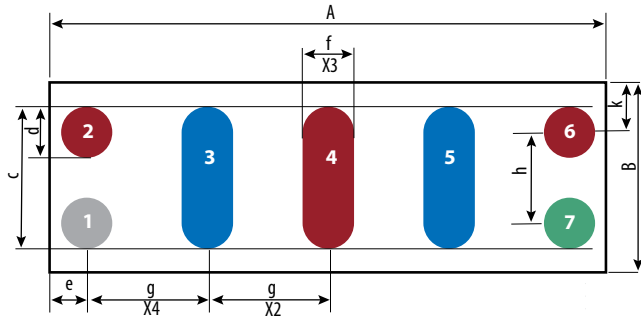
DIE MARKINGS



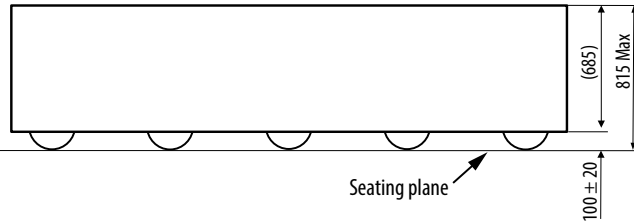
Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking line 2	Lot_Date Code Marking Line 3
EPC2019	2019	YYYY	ZZZZ

DIE OUTLINE

Solder Bar View



Side View



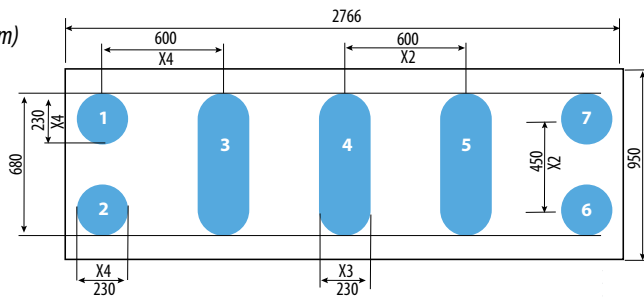
DIM	MICROMETERS		
	MIN	Nominal	MAX
A	2736	2766	2796
B	920	950	980
c	697	700	703
d	247	250	253
e	168	183	198
f	245	250	255
g	600	600	600
h	450	450	450
i	235	250	265

Pad no.1 is Gate;
 Pad no. 3, 5 are Drain;
 Pad no. 2, 4, 6 are Source;
 Pad no. 7 is Substrate.*

*Substrate pin should be connected to Source

RECOMMENDED LAND PATTERN

(measurements in μm)



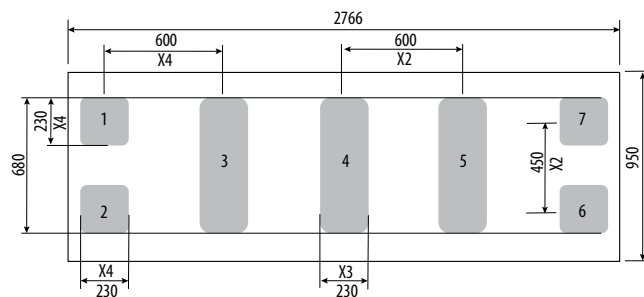
The land pattern is solder mask defined.
 Copper is larger than the solder mask opening.
 Solder mask is 10 μm smaller per side than bump.

Pad no. 1 is Gate
 Pad no. 3, 5 are Drain
 Pad no. 2, 4, 6 are Source
 Pad no. 7 is Substrate*

*Substrate pin should be connected to Source

RECOMMENDED STENCIL DRAWING

(units in μm)



Recommended stencil should be 4 mil (100 μm) thick, must be laser cut, opening per drawing. The corner has a radius of R60.

Intended for use with SAC305 Type 3 solder, reference 88.5% metals content

Additional assembly resources available at <https://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx>

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